

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for CDMA base station applications with frequencies from 2110 to 2170 MHz. Can be used in Class AB and Class C for all typical cellular base station modulations.

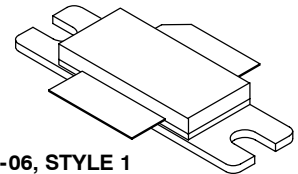
- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 1400$ mA, $P_{out} = 63$ Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
 Power Gain — 18.5 dB
 Drain Efficiency — 29%
 Device Output Signal PAR — 5.9 dB @ 0.01% Probability on CCDF
 ACPR @ 5 MHz Offset — -33 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 2140 MHz, 190 Watts CW Output Power
- Typical P_{out} @ 1 dB Compression Point = 190 Watts CW

Features

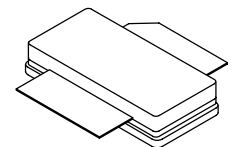
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF7S21210HR3
MRF7S21210HSR3

2110-2170 MHz, 63 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF7S21210HR3



CASE 465A-06, STYLE 1
NI-780S
MRF7S21210HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	CW	253 1.5	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 190 W CW Case Temperature 72°C, 63 W CW	$R_{\theta JC}$	0.33 0.37	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 513\ \mu\text{Adc}$)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 1400\text{ mAdc}$)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) ($V_{DD} = 28\text{ Vdc}$, $I_D = 1400\text{ mAdc}$, Measured in Functional Test)	$V_{GG(Q)}$	4	5.4	7	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 5.13\text{ Adc}$)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

Dynamic Characteristics (2)

Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	2.02	—	pF
Output Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	257	—	pF
Input Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz)	C_{iss}	—	516	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1400\text{ mA}$, $P_{out} = 63\text{ W Avg.}$, $f = 2112.5\text{ MHz}$ and $f = 2167.5\text{ MHz}$, Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.

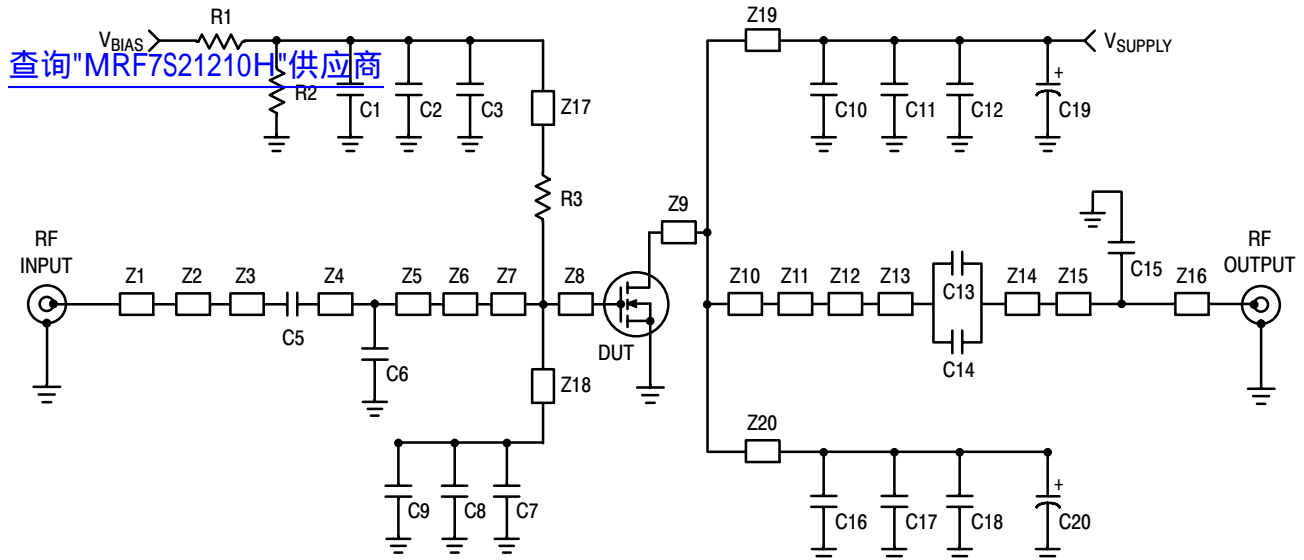
Power Gain	G_{ps}	17	18.5	20.5	dB
Drain Efficiency	η_D	26	29	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.5	5.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33	-31	dBc
Input Return Loss	IRL	—	-15	-8	dB

- $V_{GG} = 2 \times V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
- Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1400\text{ mA}$, 2110-2170 MHz Bandwidth					
IMD Symmetry @ 130 W PEP, P_{out} where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands $> 2\text{ dB}$)	IMD_{sym}	—	15	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	60	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 63\text{ W Avg.}$	G_F	—	1.2	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ $P_{out} = 190\text{ W CW}$	Φ	—	1.1	—	$^\circ$
Average Group Delay @ $P_{out} = 190\text{ W CW}$, $f = 2140\text{ MHz}$	Delay	—	2.5	—	ns
Part-to-Part Insertion Phase Variation @ $P_{out} = 190\text{ W CW}$, $f = 2140\text{ MHz}$, Six Sigma Window	$\Delta\Phi$	—	26	—	$^\circ$
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.019	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔP_{1dB}	—	0.011	—	dBm/ $^\circ\text{C}$



Z1	0.402" x 0.066" Microstrip	Z11	0.044" x 0.613" Microstrip
Z2	0.840" x 0.076" Microstrip	Z12	0.398" x 0.102" Microstrip
Z3	0.059" x 0.118" Microstrip	Z13	0.071" x 0.220" Microstrip
Z4	0.059" x 0.118" Microstrip	Z14	0.071" x 0.220" Microstrip
Z5	0.029" x 0.076" Microstrip	Z15	0.439" x 0.066" Microstrip
Z6	0.194" x 0.076" Microstrip	Z16	0.764" x 0.066" Microstrip
Z7	0.051" x 0.533" Microstrip	Z17	0.353" x 0.090" Microstrip
Z8	0.114" x 0.533" Microstrip	Z18	0.797" x 0.090" Microstrip
Z9	0.139" x 1.268" Microstrip	Z19, Z20	0.660" x 0.120" Microstrip
Z10	0.304" x 1.201" Microstrip	PCB	Taconic RF35, 0.030", $\epsilon_r = 3.5$

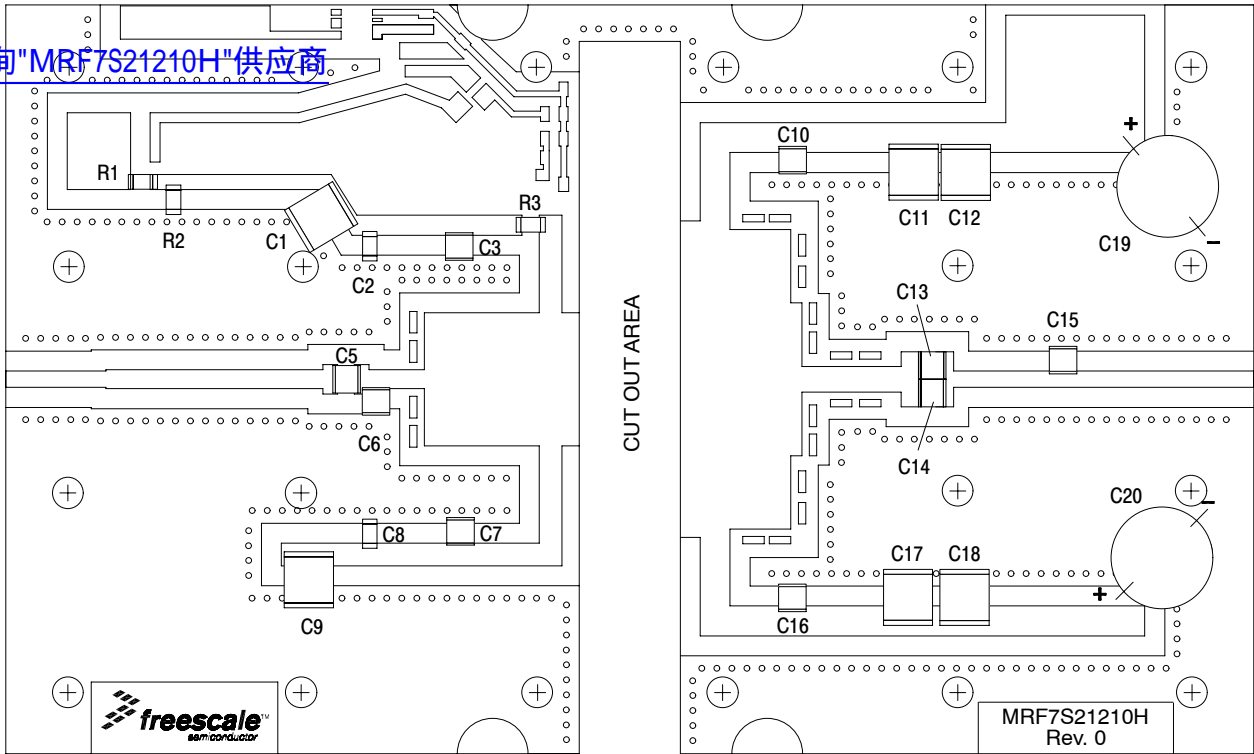
Figure 1. Test Circuit Schematic — MRF7S21210HR3

Table 5. Test Circuit Component Designations and Values — MRF7S21210HR3

Part	Description	Part Number	Manufacturer
C1, C9, C11, C12, C17, C18	10 μ F, 50 V Chip Capacitors	C5750X5R1H106MT	TDK
C2, C8	100 nF Chip Capacitors	12065C104KAT	AVX
C3, C7, C10, C13, C14, C16	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C5	5.6 pF Chip Capacitor	ATC100B5R6BT500XT	ATC
C6	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C15	0.6 pF Chip Capacitor	ATC100B0R6BT500XT	ATC
C19, C20	470 μ F Electrolytic Capacitors	2222 12018471	BC Components
R1, R2	10 K Ω , 1/4 W Chip Resistors	WCR120610KL	Welwyn
R3	10 Ω , 1/4 W Chip Resistor	232272461009	Phycomp

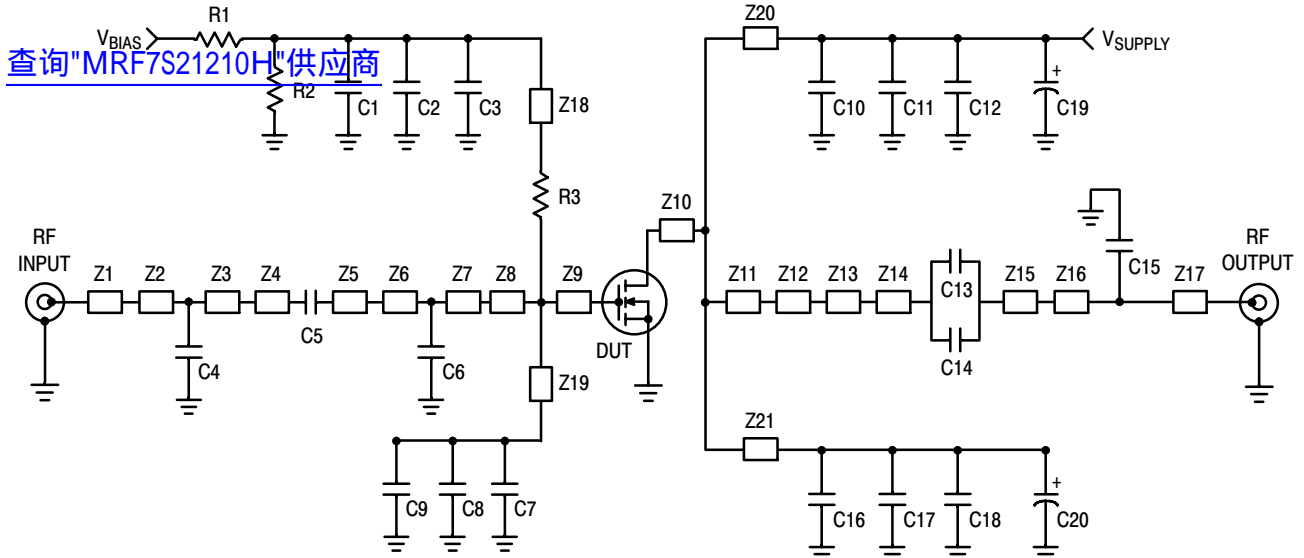
C4 not used in MRF7S21210HR3 part.

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C4 not used in MRF7S21210HR3 part.

Figure 2. Test Circuit Component Layout — MRF7S21210HR3



Z1	0.402" x 0.066" Microstrip	Z12	0.044" x 0.613" Microstrip
Z2	0.840" x 0.076" Microstrip	Z13	0.398" x 0.102" Microstrip
Z3	0.029" x 0.076" Microstrip	Z14	0.071" x 0.220" Microstrip
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Z6	0.029" x 0.076" Microstrip	Z17	0.764" x 0.066" Microstrip
Z7	0.194" x 0.076" Microstrip	Z18	0.353" x 0.090" Microstrip
Z8	0.510" x 0.533" Microstrip	Z19	0.797" x 0.090" Microstrip
Z9	0.114" x 0.533" Microstrip	Z20, Z21	0.660" x 0.120" Microstrip
Z10	0.139" x 1.268" Microstrip	PCB	Taconic RF35, 0.030", $\epsilon_r = 3.5$
Z11	0.304" x 1.201" Microstrip		

Figure 3. Test Circuit Schematic — MRF7S21210HSR3

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C2, C8	100 nF Chip Capacitors	12065C104KAT	AVX
C3, C7, C10, C13, C14, C16	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C4	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C5	5.6 pF Chip Capacitor	ATC100B5R6BT500XT	ATC
C6	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C15	0.4 pF Chip Capacitor	ATC100B0R4BT500XT	ATC
C19, C20	470 μ F Electrolytic Capacitors	2222 12018471	BC Components
R1, R2	10 K Ω , 1/4 W Chip Resistors	WCR120610KL	Welwyn
R3	10 Ω , 1/4 W Chip Resistor	232272461009	Phycomp

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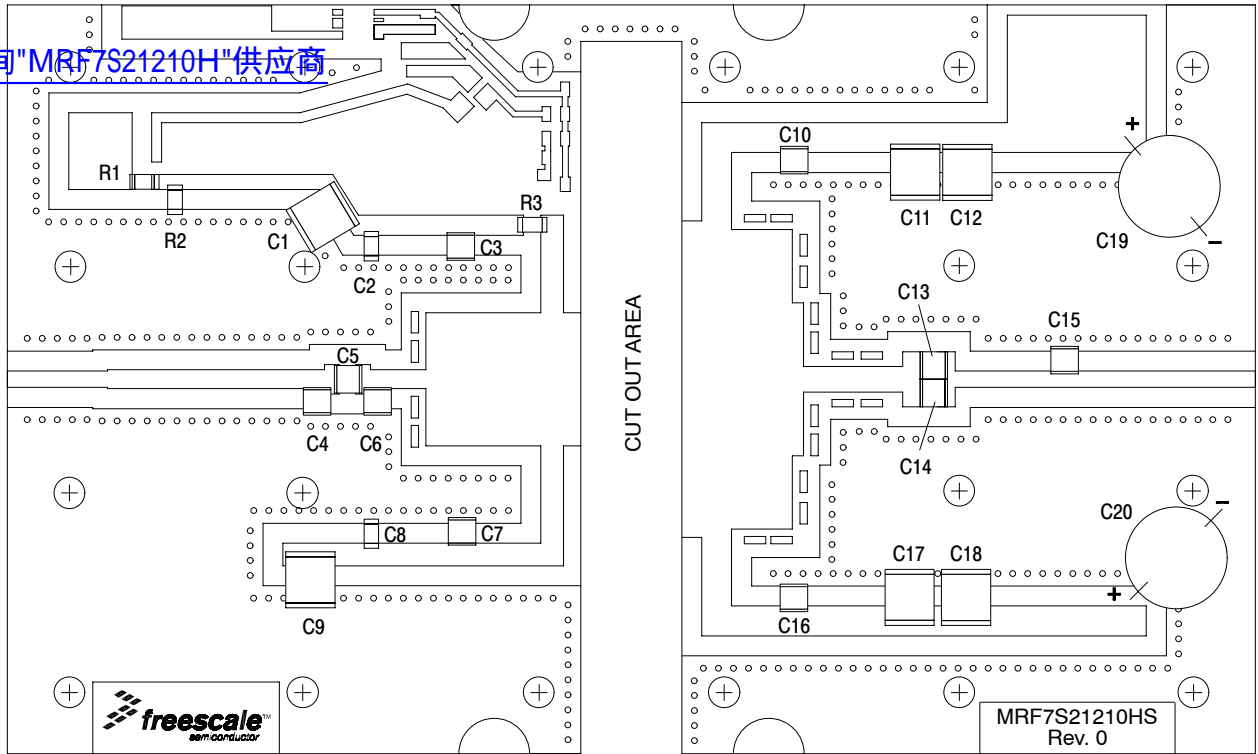
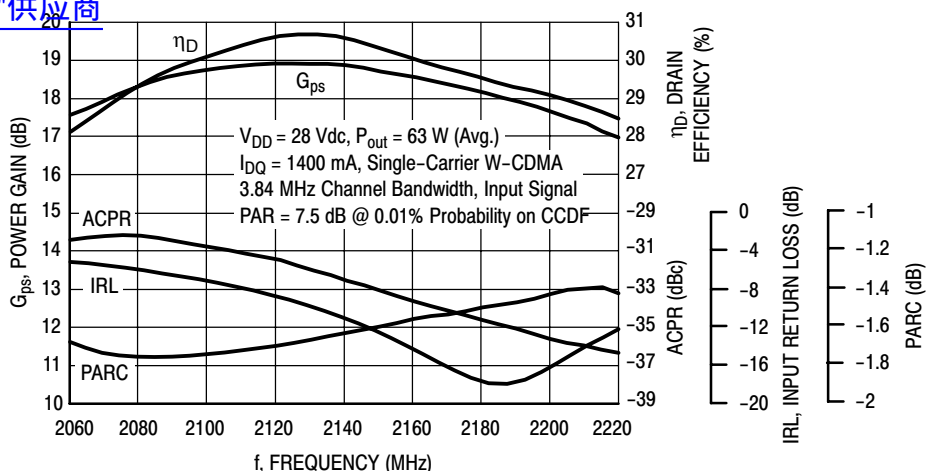


Figure 4. Test Circuit Component Layout — MRF7S21210HSR3

TYPICAL CHARACTERISTICS

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Note: Measurement conducted with device soldered on Freescale test fixture.

Figure 5. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 63$ Watts Avg.

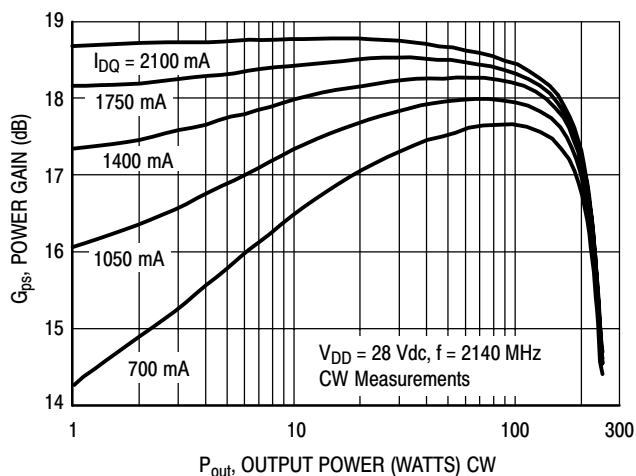


Figure 6. CW Power Gain versus Output Power

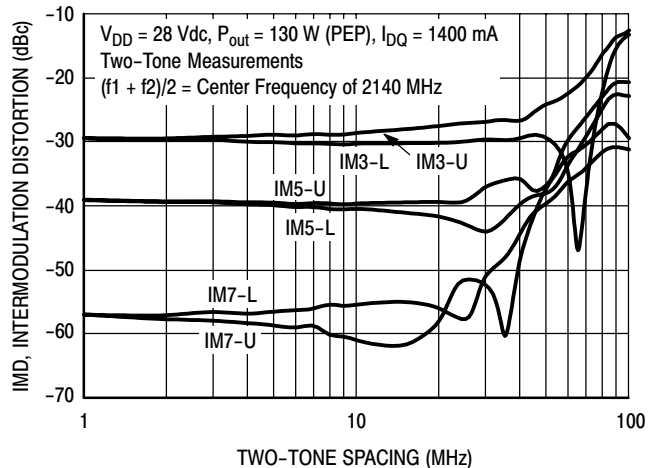


Figure 7. Intermodulation Distortion Products versus Tone Spacing

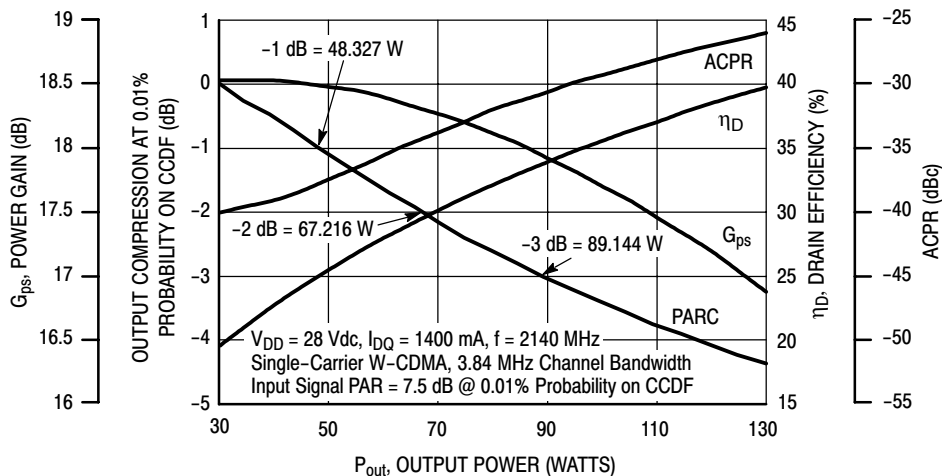


Figure 8. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

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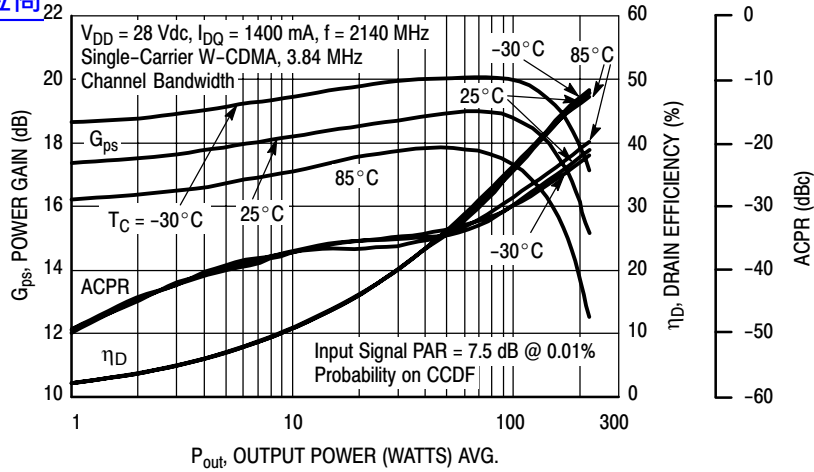


Figure 9. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

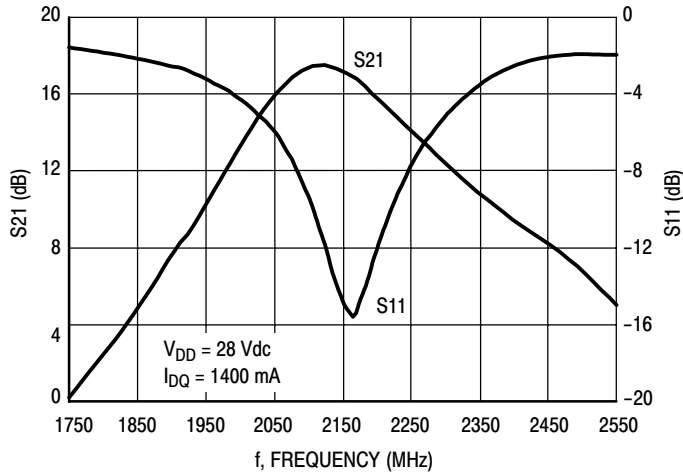
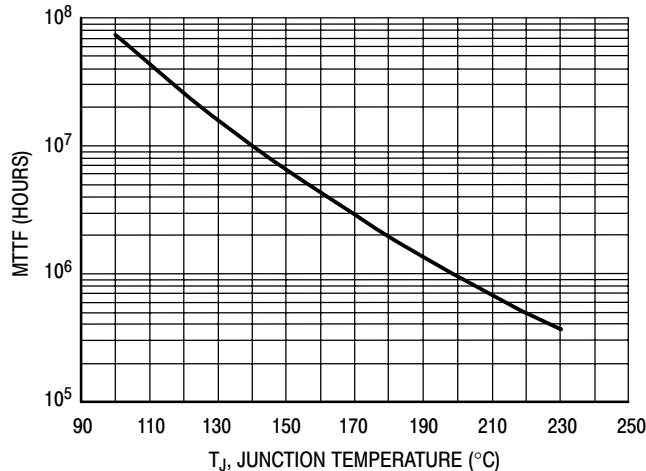


Figure 10. Broadband Frequency Response



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 28$ Vdc, $P_{out} = 63$ W Avg., and $\eta_D = 29\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 11. MTTF versus Junction Temperature

MRF7S21210HR3 MRF7S21210HSR3

W-CDMA TEST SIGNAL

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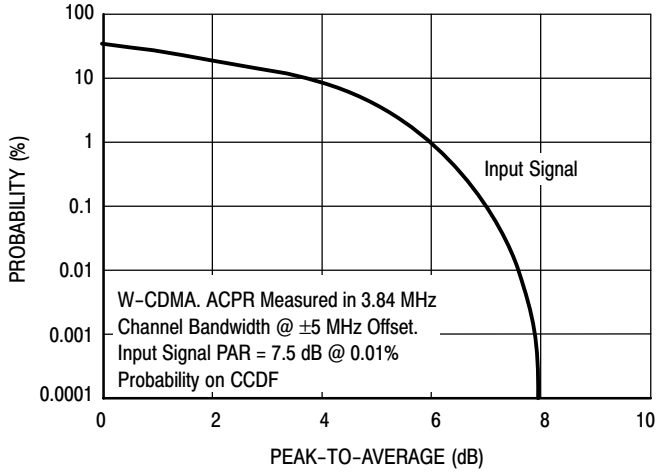


Figure 12. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

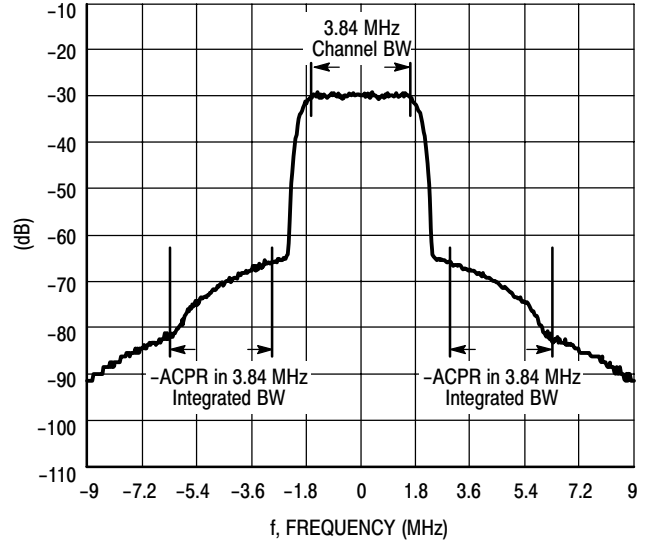
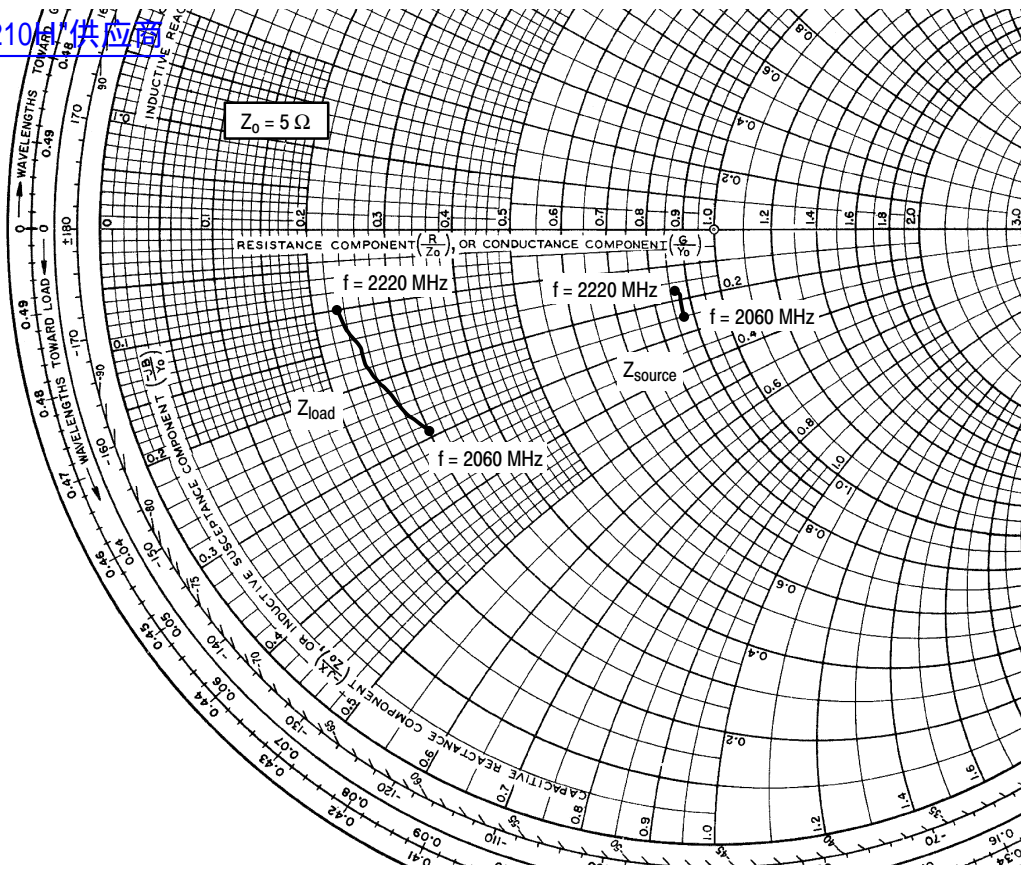


Figure 13. Single-Carrier W-CDMA Spectrum



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1400 \text{ mA}$, $P_{out} = 63 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
2060	$4.34 - j1.26$	$1.52 - j1.46$
2080	$4.34 - j1.20$	$1.47 - j1.35$
2100	$4.34 - j1.14$	$1.42 - j1.23$
2120	$4.33 - j1.09$	$1.37 - j1.11$
2140	$4.34 - j1.05$	$1.32 - j0.99$
2160	$4.33 - j0.96$	$1.27 - j0.87$
2180	$4.33 - j0.92$	$1.23 - j0.75$
2200	$4.33 - j0.92$	$1.19 - j0.64$
2220	$4.32 - j0.87$	$1.15 - j0.52$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

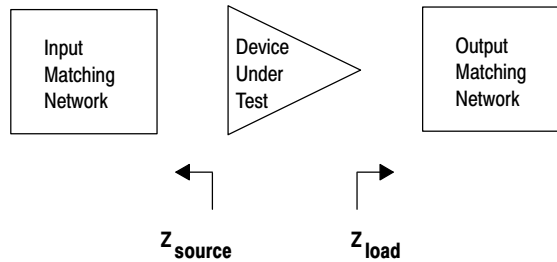
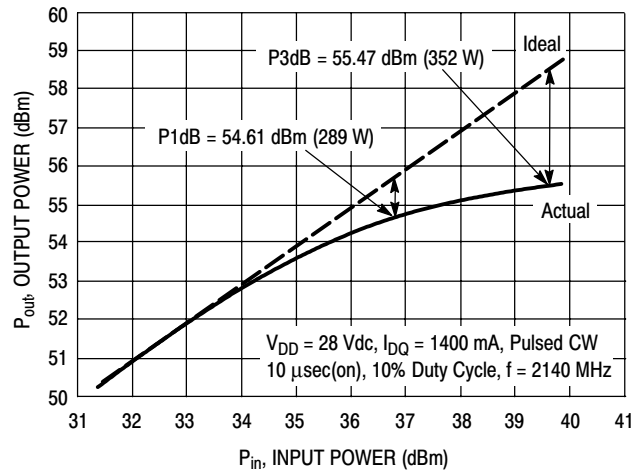


Figure 14. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

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NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

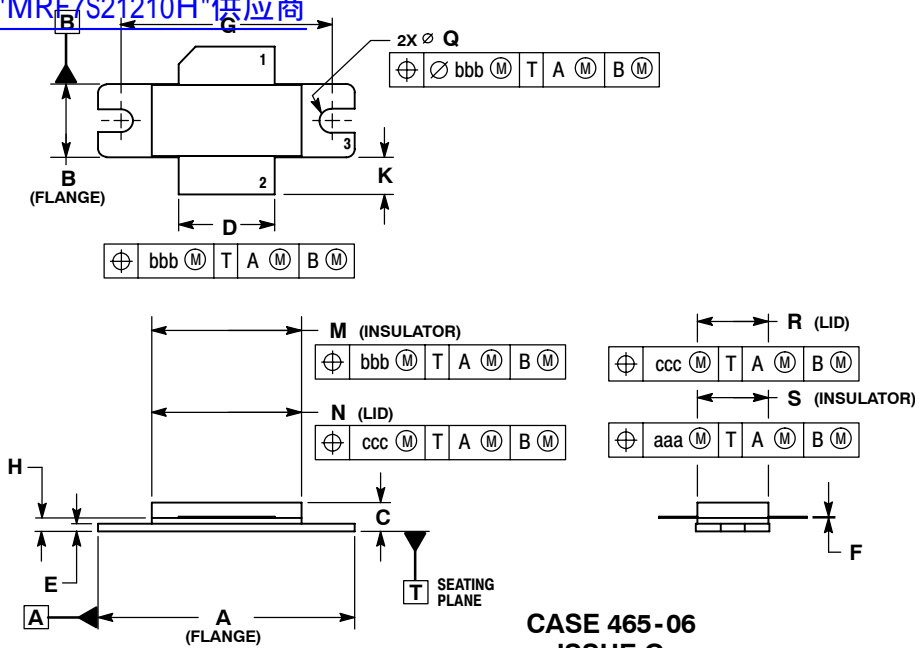
Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	5.21 - j0.31	1.23 - j1.06

Figure 15. Pulsed CW Output Power versus Input Power @ 28 V

PACKAGE DIMENSIONS

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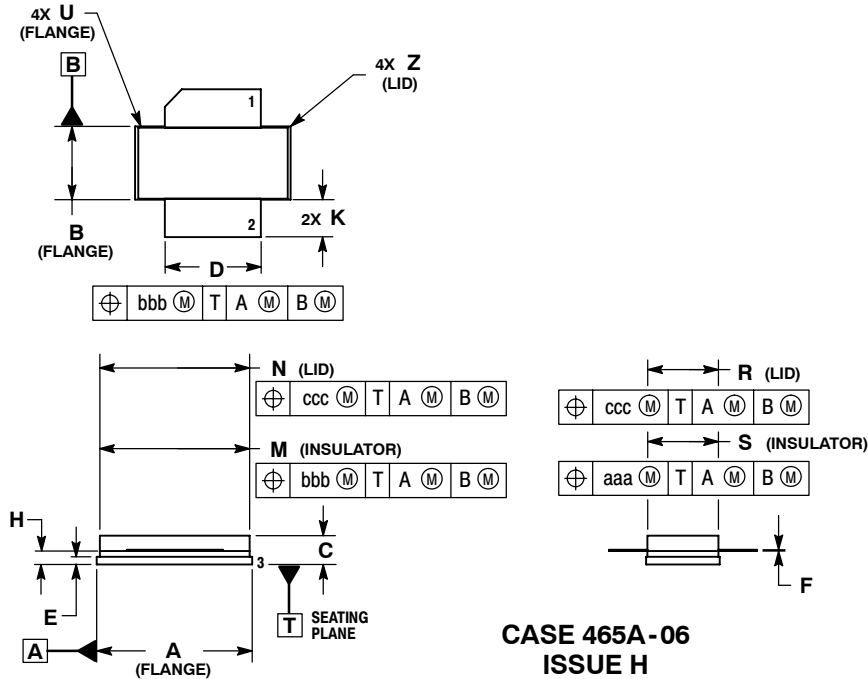


**CASE 465-06
ISSUE G
NI-780
MRF7S21210HR3**

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DELETED
 4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	Ø 0.118	Ø 0.138	Ø 3.00	Ø 3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE



**CASE 465A-06
ISSUE H
NI-780S
MRF7S21210HSR3**

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 2. CONTROLLING DIMENSION: INCH.
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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

MRF7S21210HR3 MRF7S21210HSR3

PRODUCT DOCUMENTATION

[查询"MRF7S21210H"供应商](#)
Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2008	<ul style="list-style-type: none">• Initial Release of Data Sheet
1	Jan. 2009	<ul style="list-style-type: none">• Added MRF7S21210HR3 part to data sheet, p. 1• Added Fig. 1, Test Circuit Schematic and Microstrip list for MRF7S21210HR3, p. 4• Added Fig. 2, Test Circuit Component Part Layout for MRF7S21210HR3, p. 5• Table 6, Test Circuit Component Designations and Values - MRF7S21210HR3, changed Part Number and Manufacturer for R1, R2 from CRCW12061002FKEA, Vishay to WCR120610KL, Welwyn and for R3 from CRCW12061000FKEA, Vishay to 232272461009, Phycomp, p. 6• Added Fig. 11, MTTF versus Junction Temperature, p. 9• Added 465-06 (NI-780) package isometric, p. 1, and Mechanical Outline, p. 12

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