

LOW INPUT VOLTAGE, DUAL LOAD SWITCH WITH CONTROLLED TURN-ON

FEATURES

- Integrated Dual Load Switch
- Input Voltage Range: 1.62 V to 5.5 V
- Low ON-State Resistance
 - $r_{ON} = 342\text{ m}\Omega$ at $V_{IN} = 5.5\text{ V}$
 - $r_{ON} = 435\text{ m}\Omega$ at $V_{IN} = 3.3\text{ V}$
 - $r_{ON} = 523\text{ m}\Omega$ at $V_{IN} = 2.6\text{ V}$
 - $r_{ON} = 714\text{ m}\Omega$ at $V_{IN} = 1.8\text{ V}$
- 500-mA Maximum Continuous Switch Current
- Low Quiescent Current and Shutdown Current
- Controlled Switch Output Rise Time: 75 μs or 660 μs
- Integrated Quick Output Discharge Transistor
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- 8-Pin SOT (DCN) Package: 3 mm × 3 mm
- 8-Pin μQFN (RSE) Package: 1.5 mm × 1.5 mm

DESCRIPTION

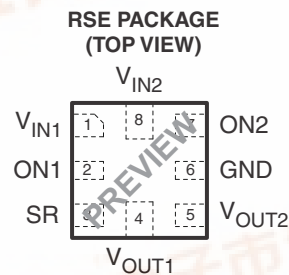
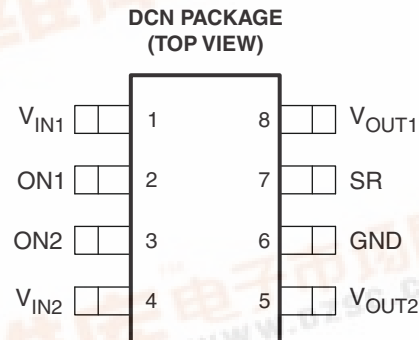
The TPS22960 is a small low- r_{ON} dual load switch with controlled turn on. The devices contain two P-channel MOSFETs that can operate over an input voltage range of 1.62 V to 5.5 V. Each switch is controlled by an on/off input (ON1 and ON2), which is capable of interfacing directly with low-voltage control signals. In TPS22960 a 85- Ω on-chip load resistor is added for output quick discharge when switch is turned off.

The rise time (slew-rate) of the device is internally controlled in order to avoid inrush current and can be slowed down if needed using the SR pin: TPS22960 feature a 75 μs rise time with the SR pin tied to ground and 660 μs with the SR pin tied to high.

The TPS22960 is available in a space-saving 8-pin μQFN package and in an 8-pin SOT package. It is characterized for operation over the free-air temperature range of -40°C to 85°C .

APPLICATIONS

- GPS Devices
- Cell Phones/PDAs
- MP3 Players
- Digital Cameras



DEVICE	r_{ON} AT 3.3 V (TYP)	SLEW RATE AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE ⁽¹⁾	MAX OUTPUT CURRENT	ENABLE
TPS22960	435 m Ω	75 μs with SR = low 660 μs with SR = high	Yes	500 mA	Active High

(1) This feature discharges the output of the switch to ground through a 85- Ω resistor, preventing the output from floating.



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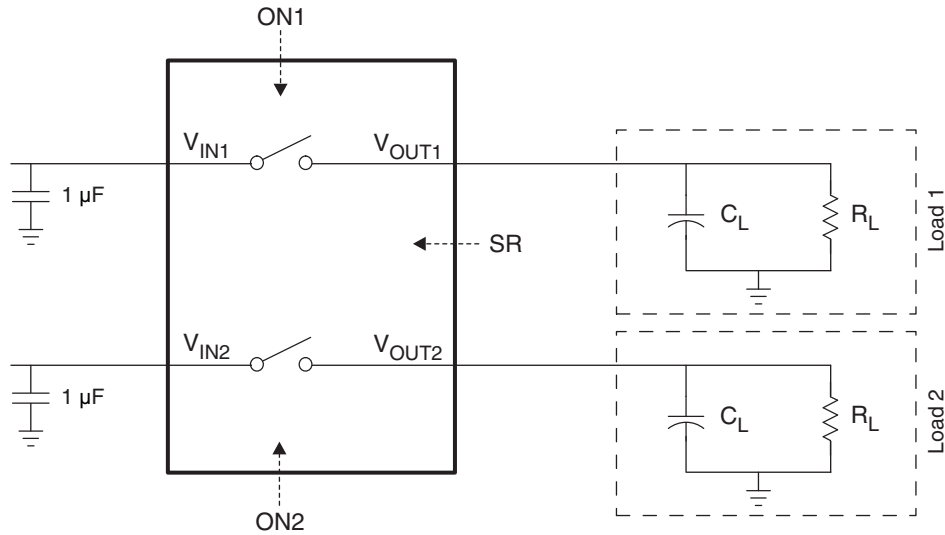


ORDERING INFORMATION

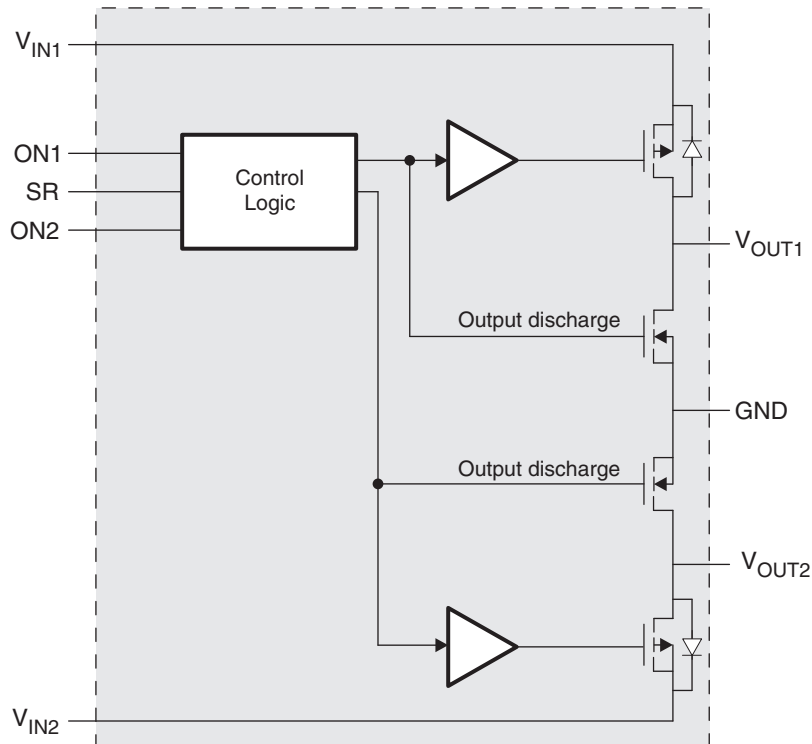
T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	μQFN – RSE	Tape and reel	TPS22960RSER	PREVIEW
	SOT – DCN	Tape and reel	TPS22960DCNR	NFR_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DCN: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

TYPICAL APPLICATION



APPLICATION BLOCK DIAGRAM



CONFIGURABLE LOGIC FUNCTION TABLE

ONx	V _{INx} TO V _{OUTx}	V _{OUTx} TO GND
L	OFF	ON
H	ON	GND

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
DCN PIN NO.	RSE PIN NO.	NAME	
1	1	V _{IN1}	Switch 1 input; bypass this input with a ceramic capacitor to GND
2	2	ON1	Switch 1 control input, active high. Do not leave floating.
3	7	ON2	Switch 2 control input, active high. Do not leave floating.
4	8	V _{IN2}	Switch 2 input; bypass this input with a ceramic capacitor to GND
5	5	V _{OUT2}	Switch 2 output
6	6	GND	Ground
7	3	SR	Slew rate control pin. SR = GND translates into a 75-μs rise time; SR = high translates into a 660-μs rise time
8	4	V _{OUT1}	Switch 1 output

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage range	-0.3	6	V
V _{OUT}	Output voltage range		V _{IN} + 0.3	V
V _{ON}	Input voltage range	-0.3	6	V
I _{MAX}	Maximum continuous switch current		0.5	A
T _A	Operating free-air temperature range	-40	85	°C
T _{stg}	Storage temperature range	-65	150	°C
T _{lead}	Maximum lead temperature (10-s soldering time)		300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)		V
		Charged-Device Model (CDM)		
			2000	
			1000	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

BOARD	PACKAGE	R _{θJC}	R _{θJA}	DERATING FACTOR ABOVE T _A = 25°C	T _A < 25°C	T _A = 70°C	T _A = 85°C
High-K ⁽¹⁾	DCN	123°C/W	220°C/W	-4.545 mW/°C	454.5 mW	250 mW	181.1 mW
High-K ⁽¹⁾	RSE	183°C/W	253°C/W	-3.952 mW/°C	395.2 mW	217.3 mW	158.1 mW

(1) The JEDEC High-K (2s2p) board used to derive this data was a 3 × 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V _{IN}	Input voltage range	1.62	5.5	V
V _{OUT}	Output voltage range		V _{IN}	V
V _{IH}	High-level input voltage: ON1, ON2, SR	V _{INx} = 3.0 V to 5.5 V		V
		V _{INx} = 1.62 V to 3.0 V		
V _{IL}	Low-level input voltage: ON1, ON2, SR	V _{INx} = 3.0 V to 5.5 V		V
		V _{INx} = 1.62 V to 3.0 V		
C _{IN}	Input capacitor	1 ⁽¹⁾		μF

(1) See [Application Information](#)

ELECTRICAL CHARACTERISTICS

 $V_{IN} = 1.62\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP ⁽¹⁾	MAX	UNIT
I_{IN} Quiescent current (each switch)	$I_{OUTx} = 0$, $V_{INx} = V_{ON}$	$V_{INx} = 5.5\text{ V}$	Full	0.64	2	μA
		$V_{INx} = 3.3\text{ V}$	Full	0.35	1.2	
		$V_{INx} = 2.5\text{ V}$	Full	0.24	0.8	
		$V_{INx} = 1.8\text{ V}$	Full	0.15	0.5	
$I_{IN(OFF)}$ OFF-state supply current (each switch)	$V_{ON} = \text{GND}$, $V_{OUTx} = \text{Open}$	$V_{INx} = 5.5\text{ V}$	Full	0.47	3.6	μA
		$V_{INx} = 3.3\text{ V}$	Full	0.25	1.8	
		$V_{INx} = 2.5\text{ V}$	Full	0.18	1.3	
		$V_{INx} = 1.8\text{ V}$	Full	0.11	0.9	
r_{ON} ON-state resistance (each switch)	$I_{OUT} = -200\text{ mA}$	$V_{INx} = 5.5\text{ V}$	25°C	342	400	$\text{m}\Omega$
			Full		465	
		$V_{INx} = 3.3\text{ V}$	25°C	435	500	
			Full		595	
		$V_{INx} = 2.5\text{ V}$	25°C	523	620	
			Full		720	
		$V_{INx} = 1.8\text{ V}$	25°C	714	855	
			Full		995	
		$V_{INx} = 1.62\text{ V}$	25°C	830	950	
			Full		1100	
r_{PD} Output pulldown resistance	$V_{IN} = 3.3\text{ V}$, $V_{ON} = 0$, $I_{OUT} = 30\text{ mA}$	25°C		85	120	Ω
I_{ON} ON-state input leakage current	$V_{ON} = 1.62\text{ V to }5.5\text{ V or GND}$	Full			0.25	μA

 (1) Typical values are at $T_A = 25^\circ\text{C}$.

SWITCHING CHARACTERISTICS

 $V_{IN} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_{L_CHIP} = 85\ \Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{ON} Turn-ON time	$R_L = 33\ \Omega$, $C_L = 0.1\ \mu\text{F}$	$SR = V_{IN}$		635	μs
		$SR = \text{GND}$		67	
t_{OFF} Turn-OFF time	$R_L = 33\ \Omega$, $C_L = 0.1\ \mu\text{F}$	$SR = V_{IN}$		4.5	μs
		$SR = \text{GND}$		4.2	
t_r V_{OUT} rise time	$R_L = 33\ \Omega$, $C_L = 0.1\ \mu\text{F}$	$SR = V_{IN}$		660	μs
		$SR = \text{GND}$		75	
t_f V_{OUT} fall time	$R_L = 33\ \Omega$, $C_L = 0.1\ \mu\text{F}$	$SR = V_{IN}$		4.5	μs
		$SR = \text{GND}$		4.5	

 (1) Typical values are at the specified $V_{IN} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$

TYPICAL CHARACTERISTICS

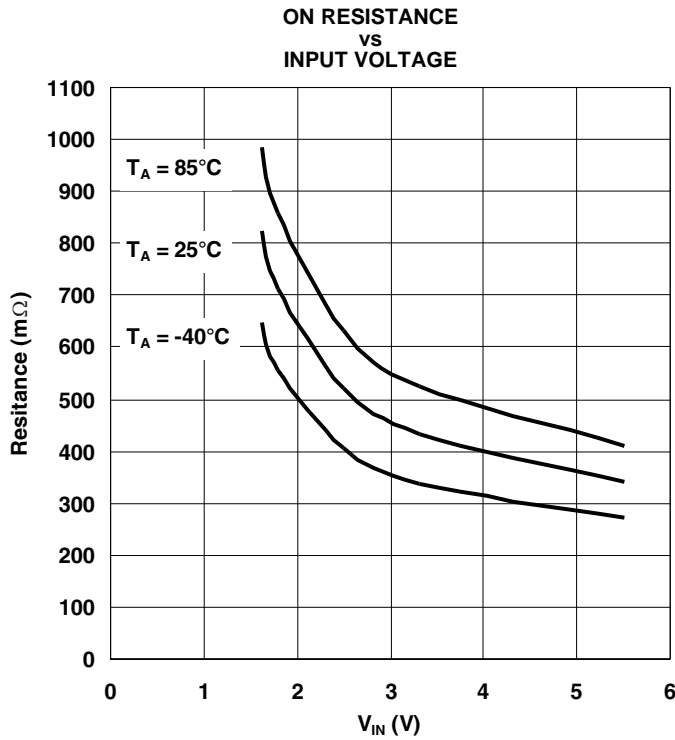


Figure 1.

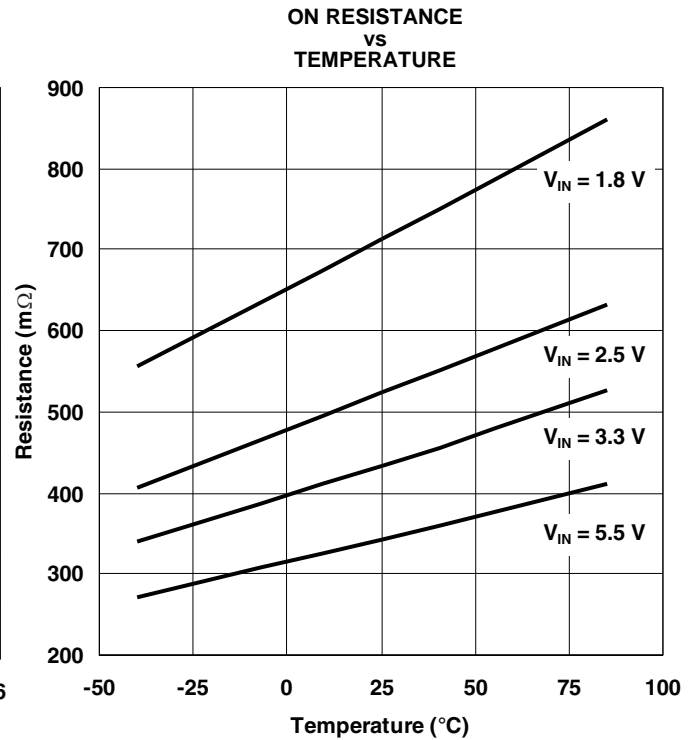


Figure 2.

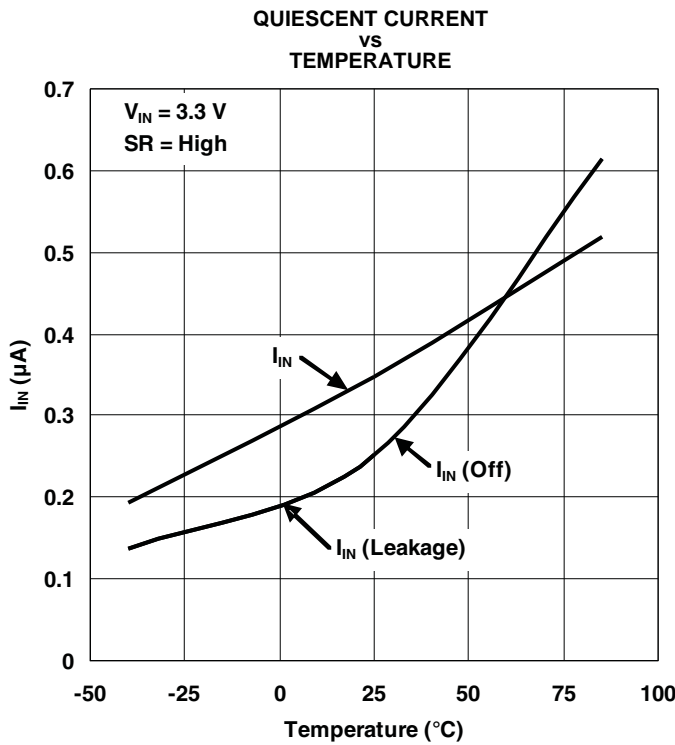


Figure 3.

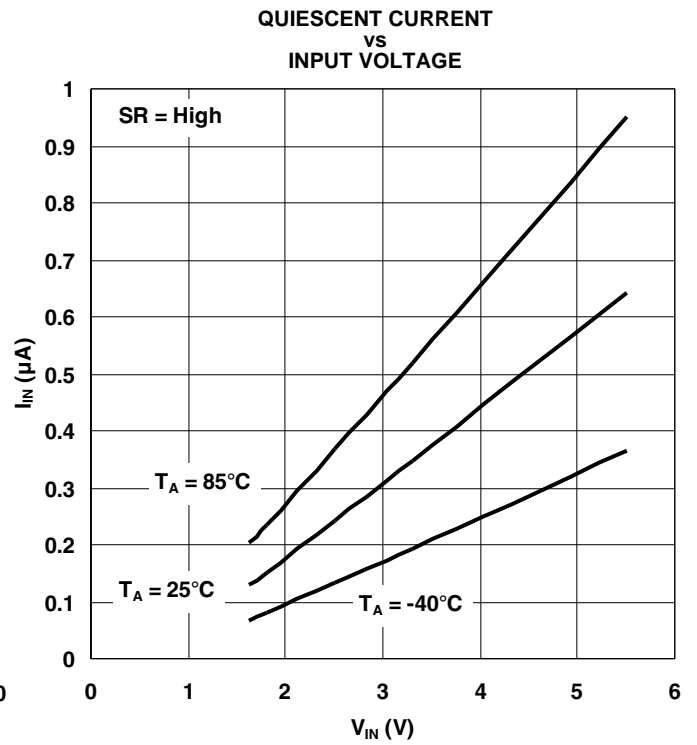
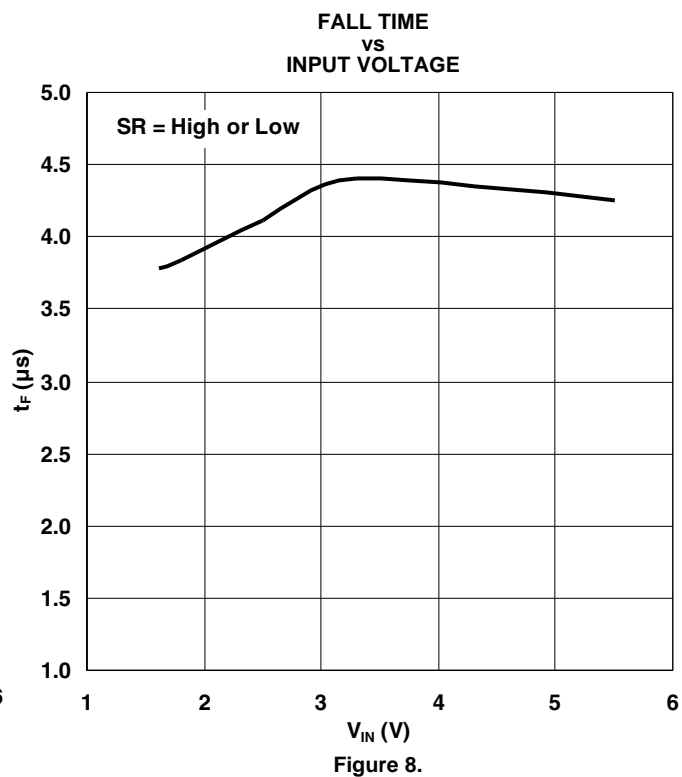
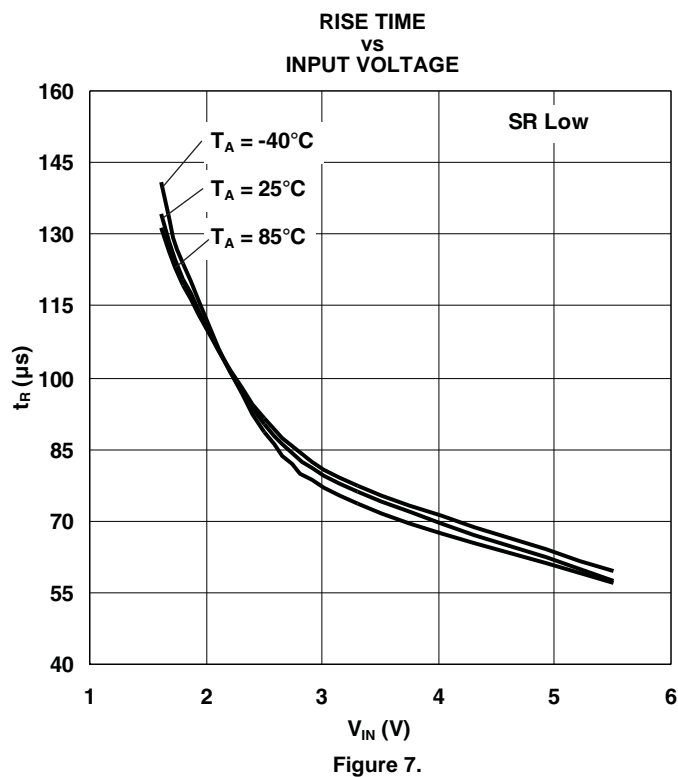
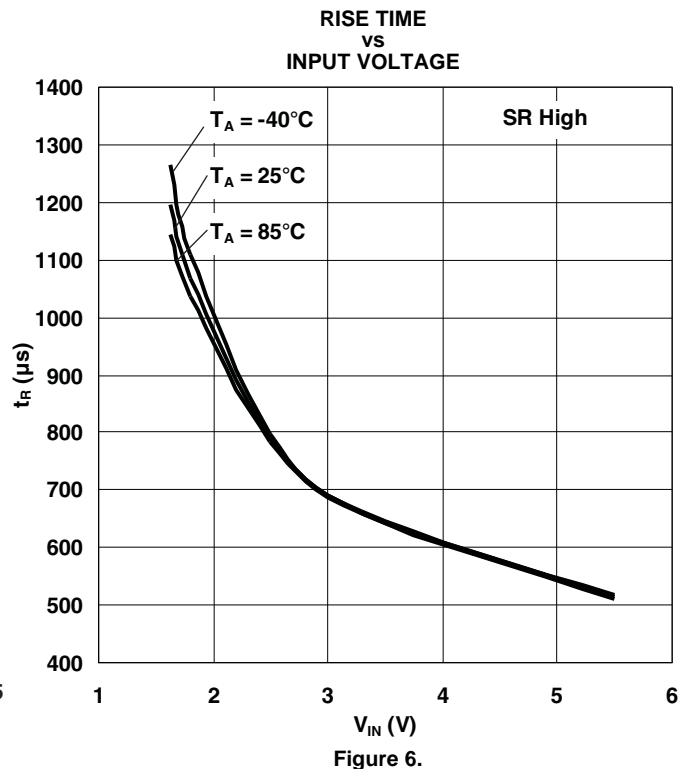
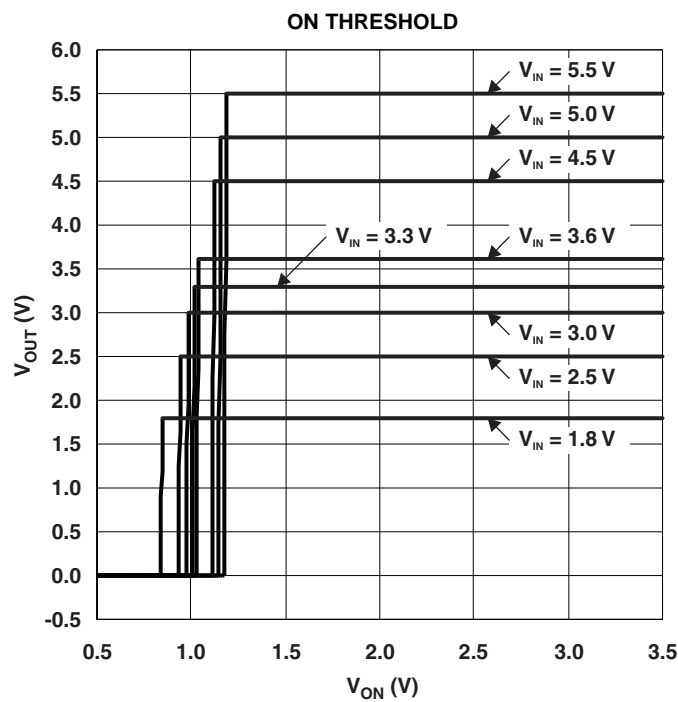


Figure 4.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

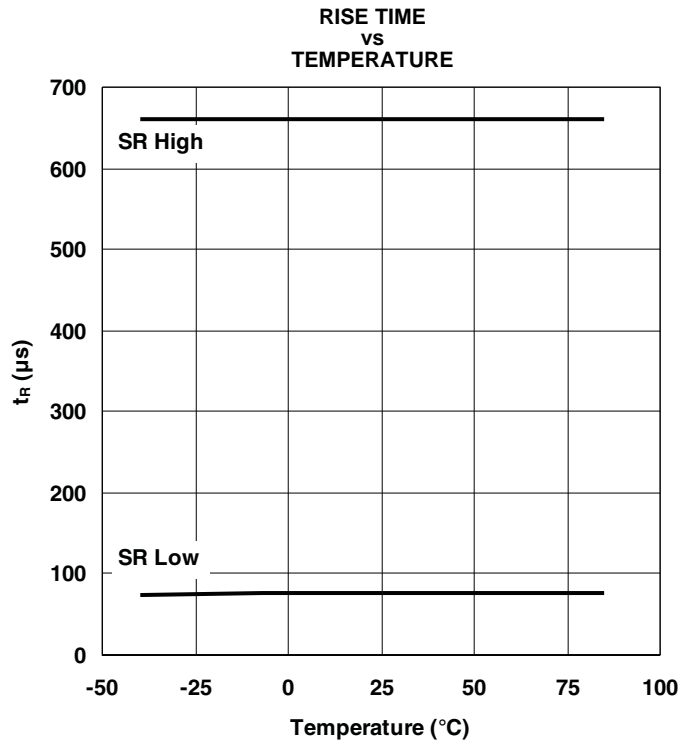


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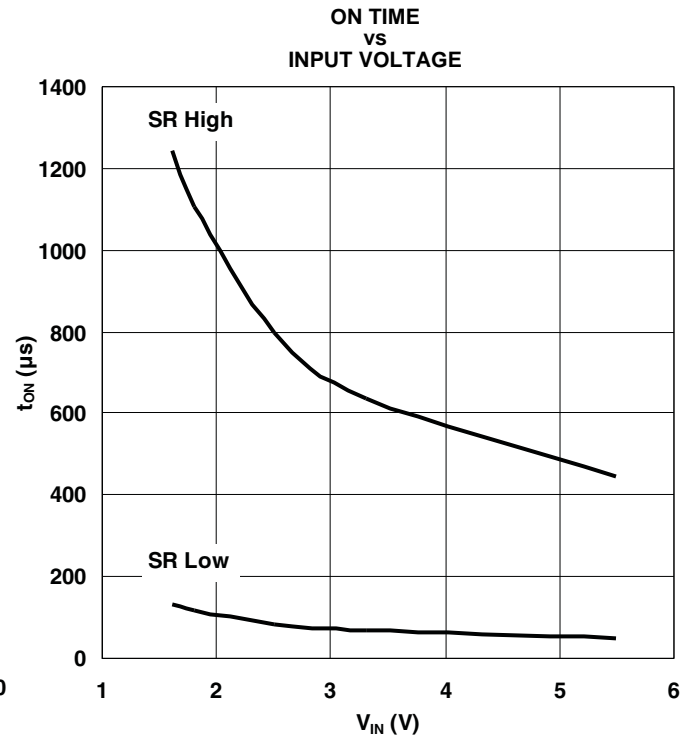


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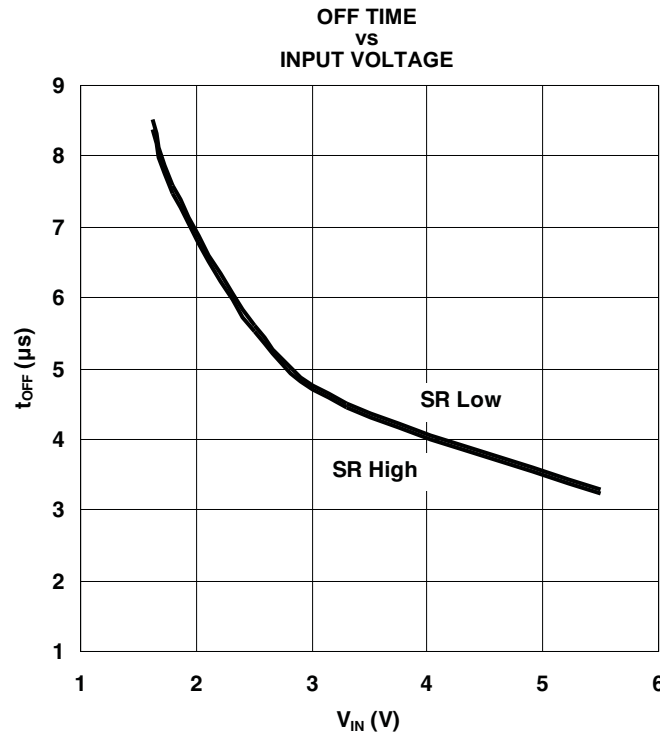


Figure 11.

TYPICAL CHARACTERISTICS (continued)

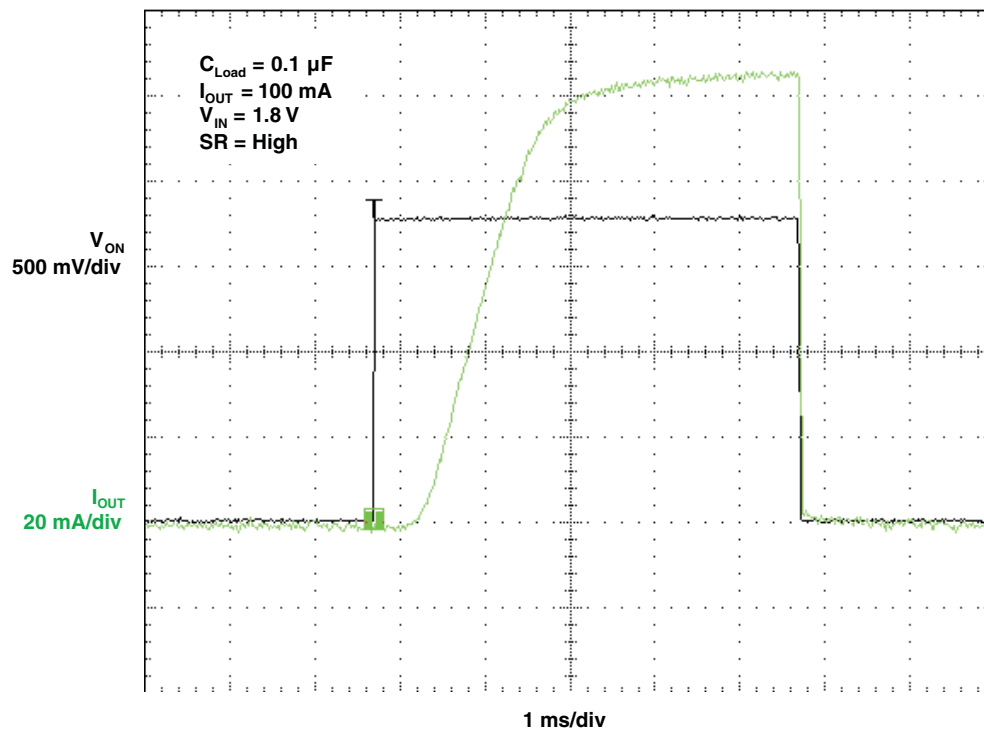


Figure 12. t_{ON} Response

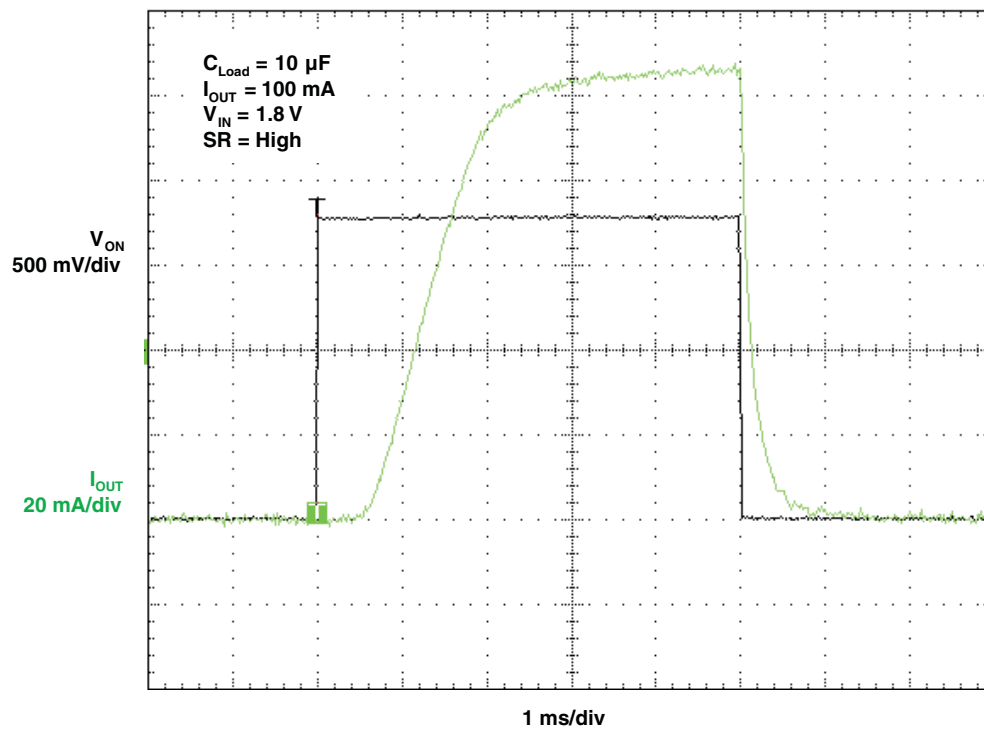


Figure 13. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

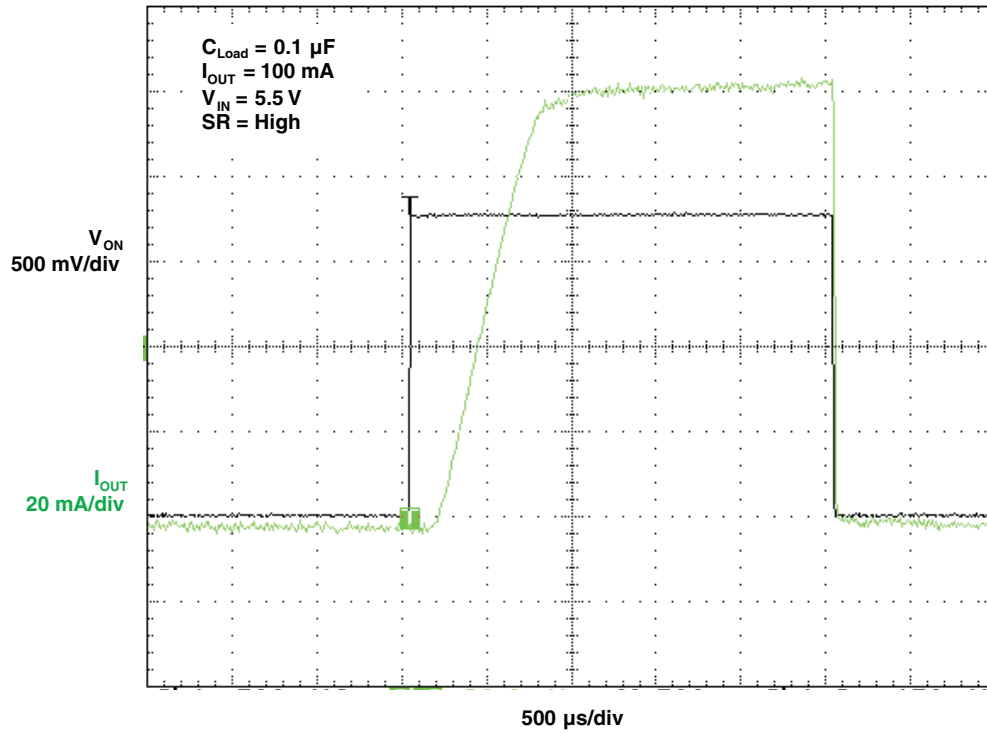


Figure 14. t_{ON} Response

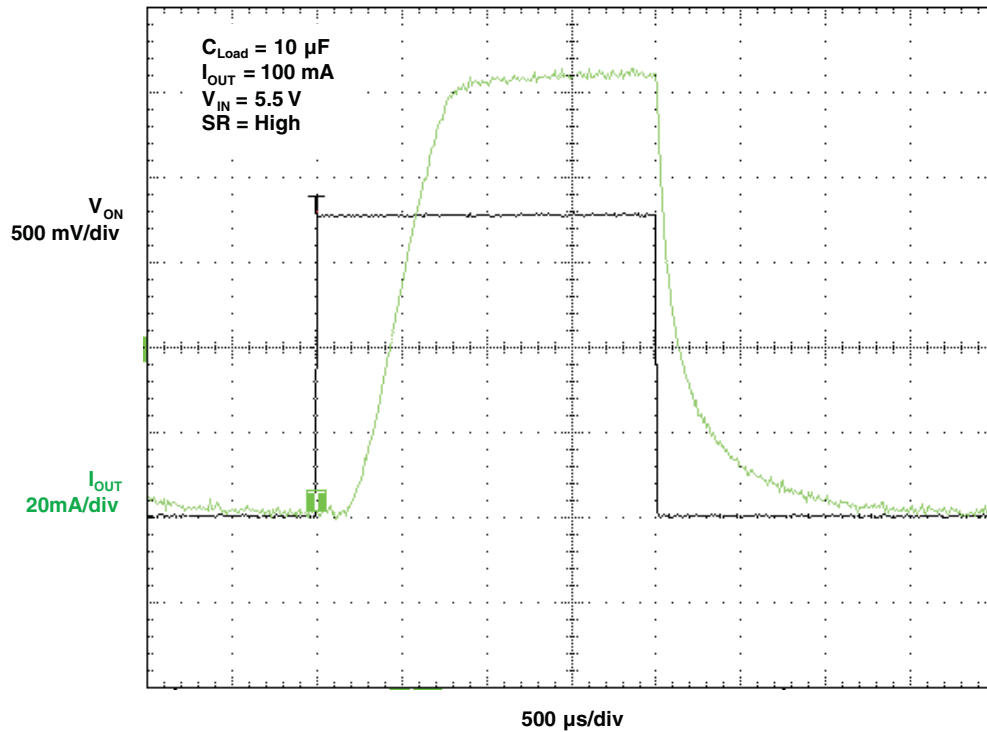


Figure 15. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

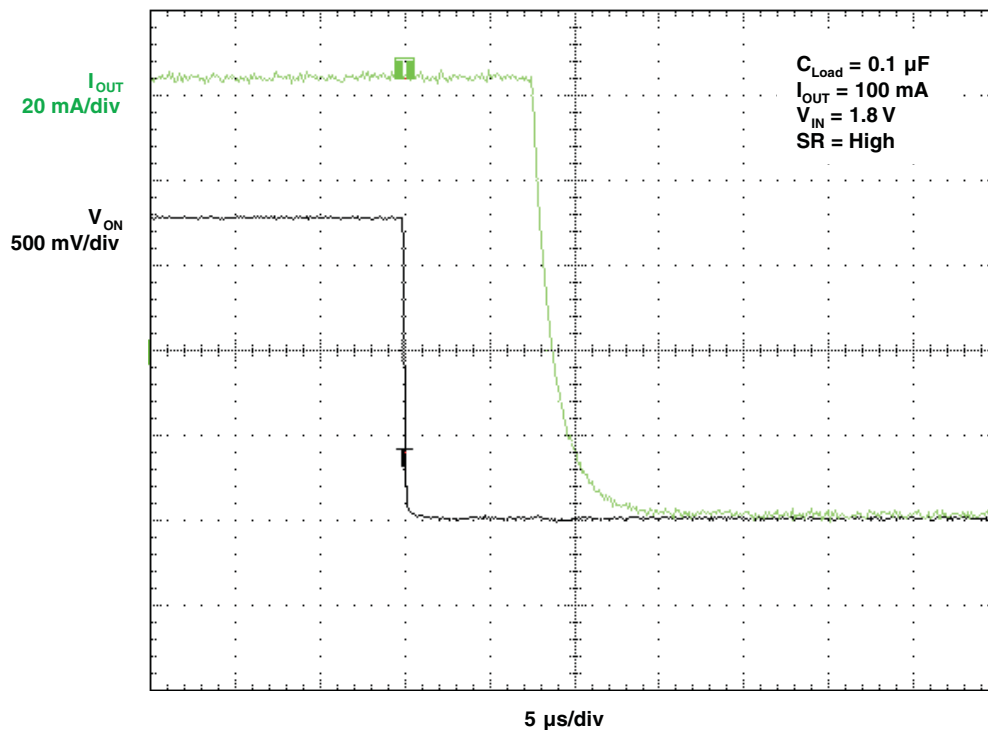


Figure 16. t_{OFF} Response

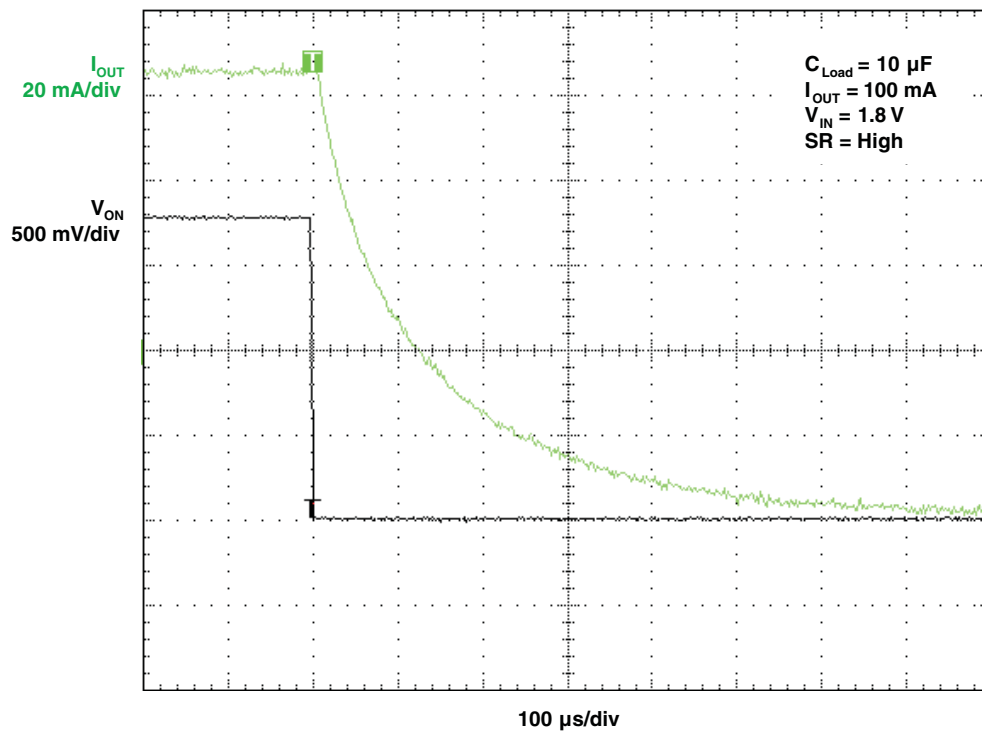


Figure 17. t_{OFF} Response

TYPICAL CHARACTERISTICS (continued)

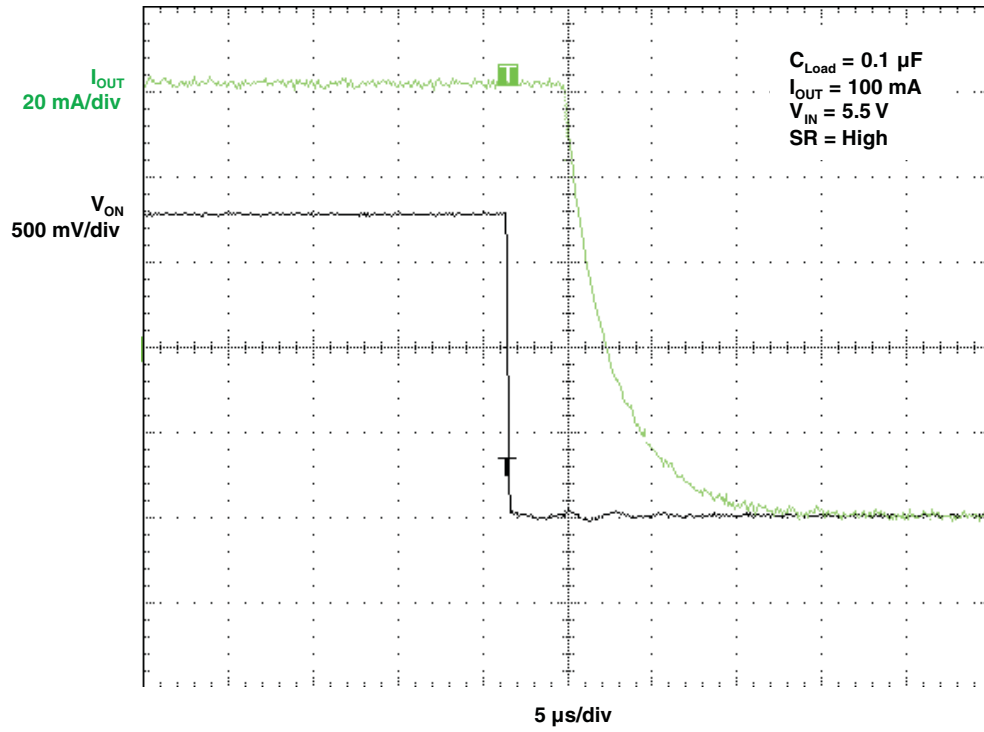


Figure 18. t_{OFF} Response

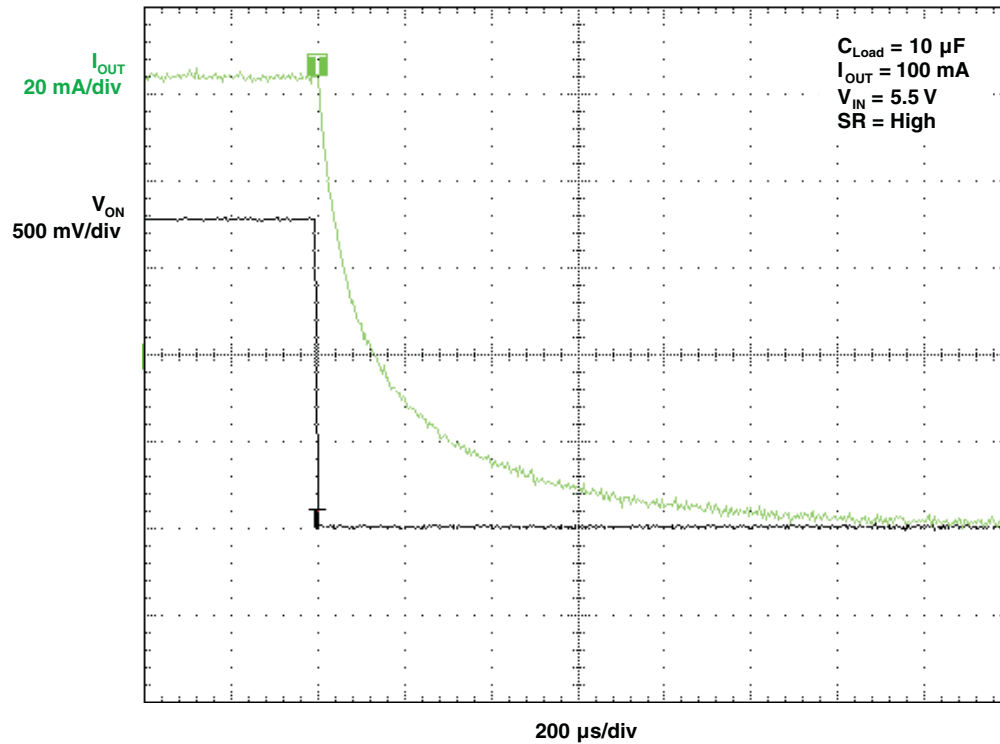


Figure 19. t_{OFF} Response

TYPICAL CHARACTERISTICS (continued)

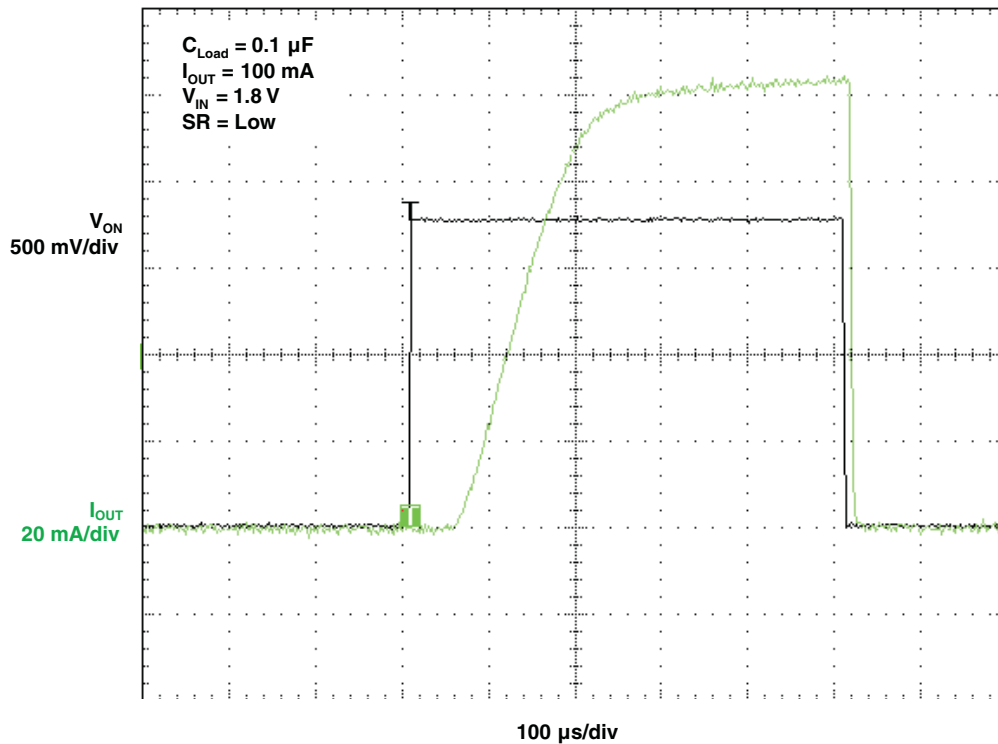


Figure 20. t_{ON} Response

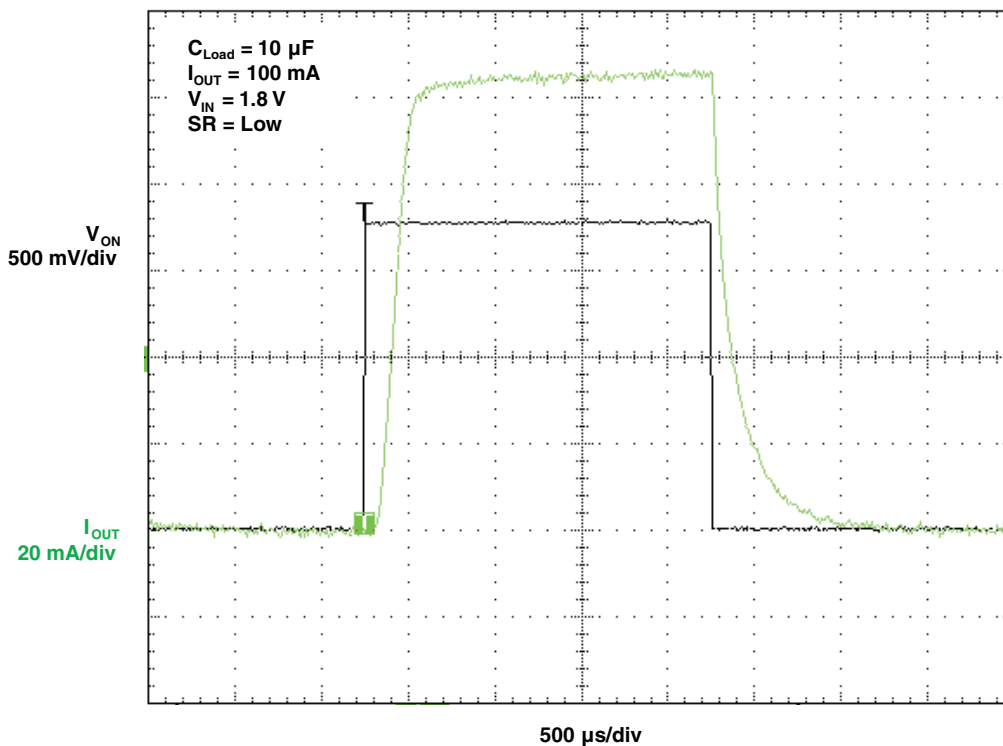


Figure 21. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

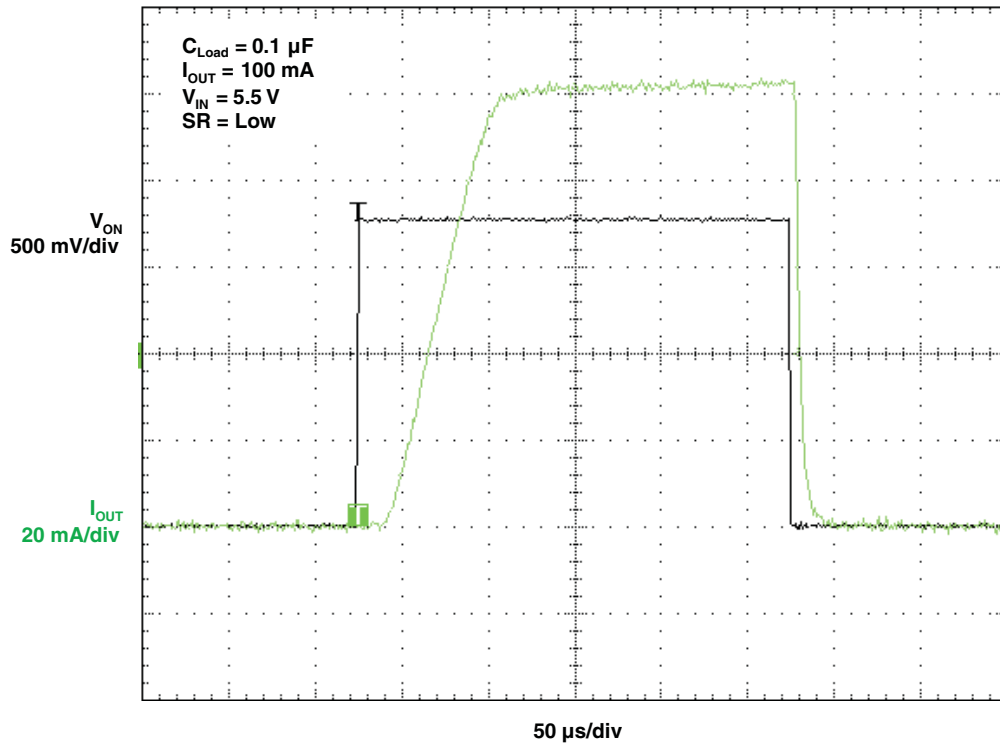


Figure 22. t_{ON} Response

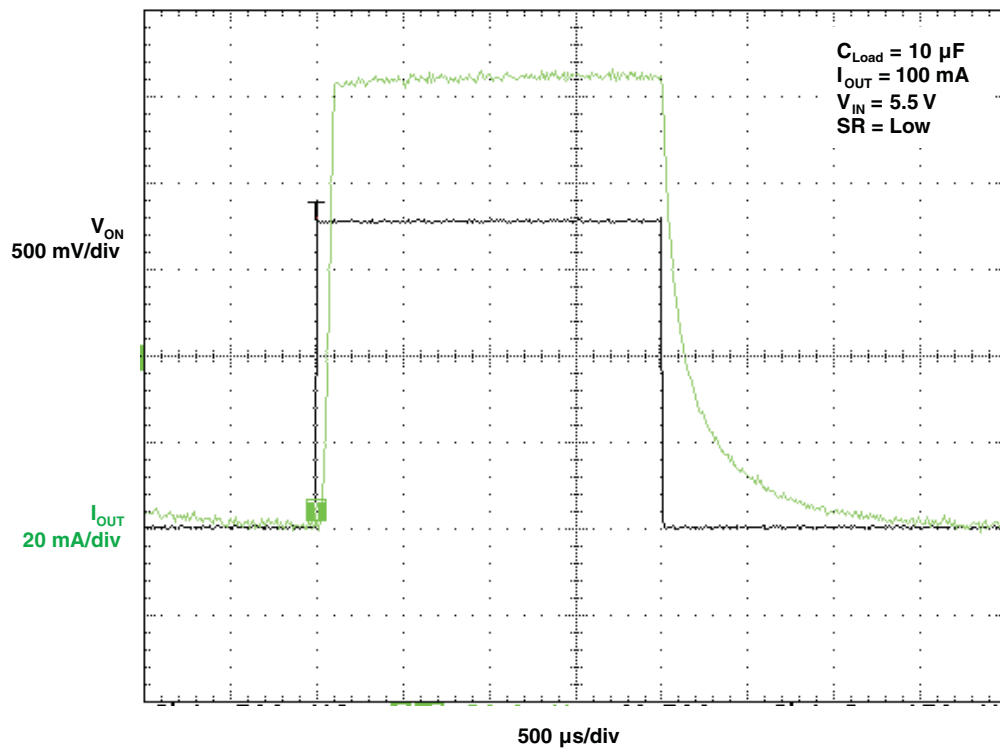


Figure 23. t_{ON} Response

TYPICAL CHARACTERISTICS (continued)

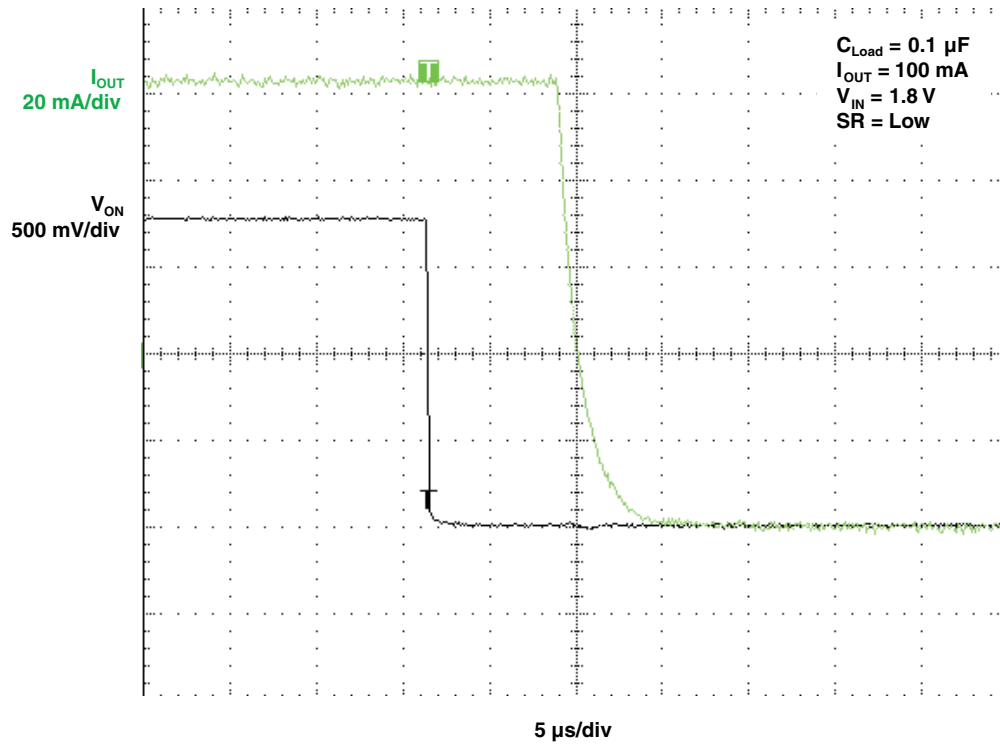


Figure 24. t_{OFF} Response

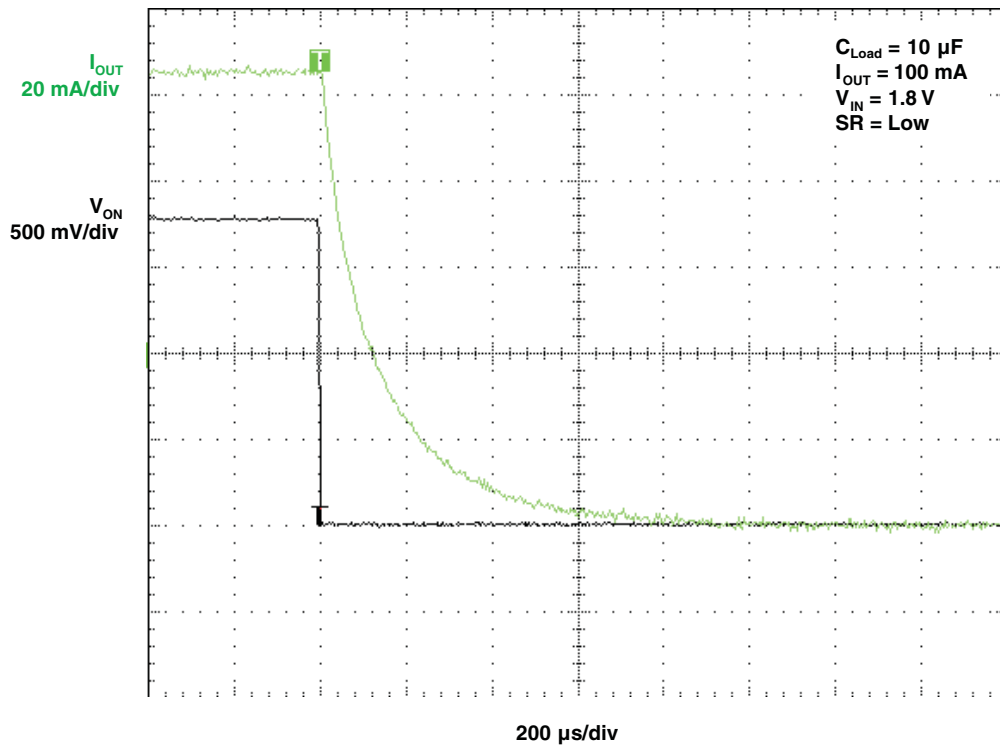


Figure 25. t_{OFF} Response

TYPICAL CHARACTERISTICS (continued)

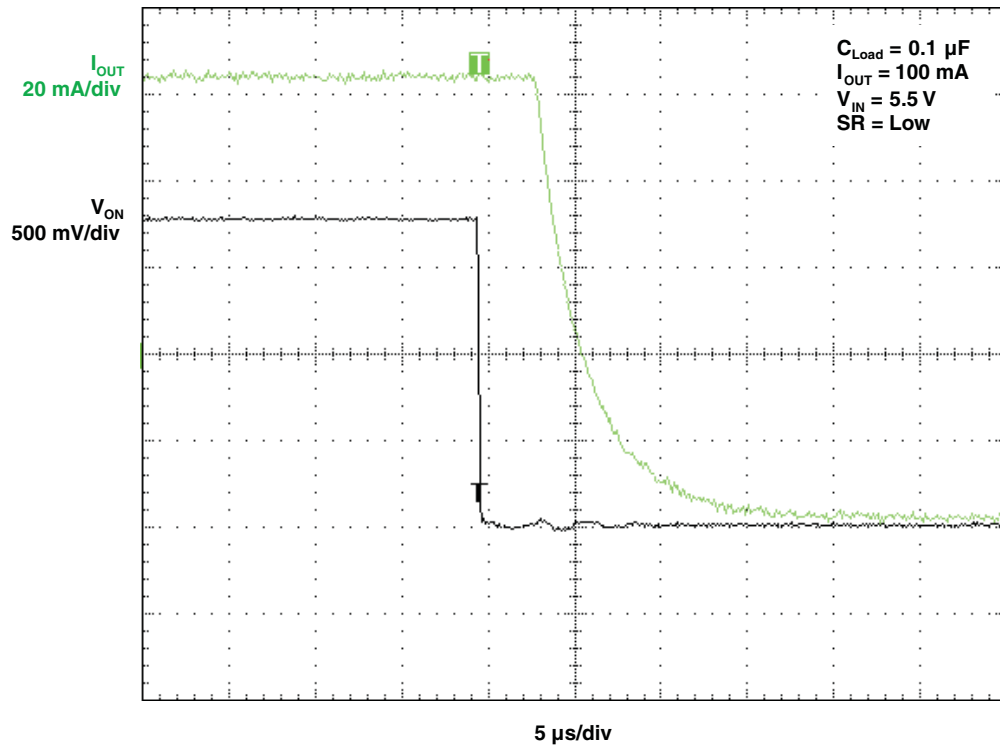


Figure 26. t_{OFF} Response

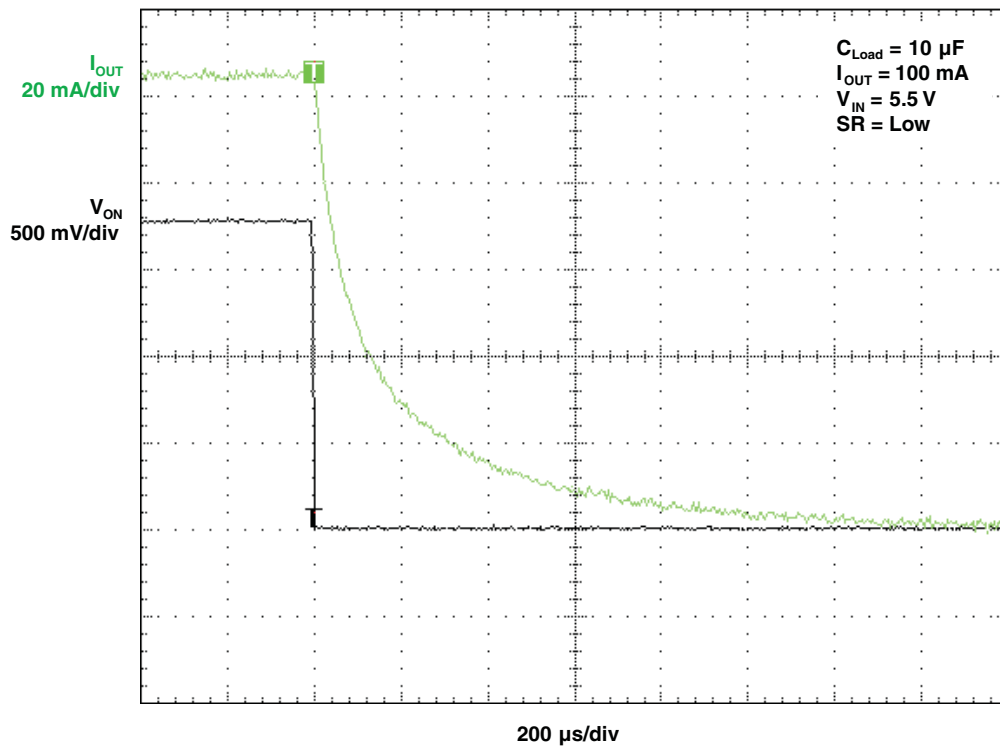
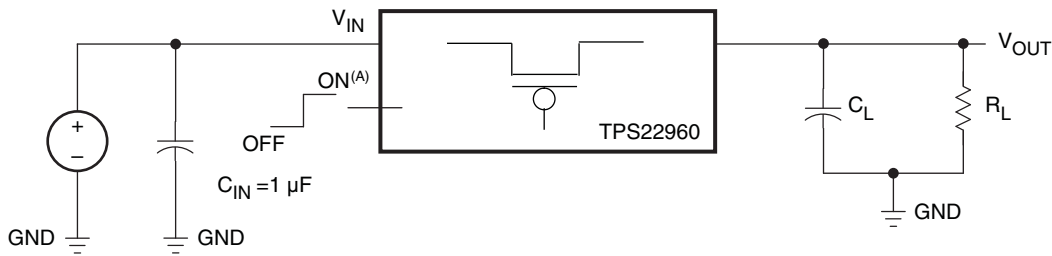
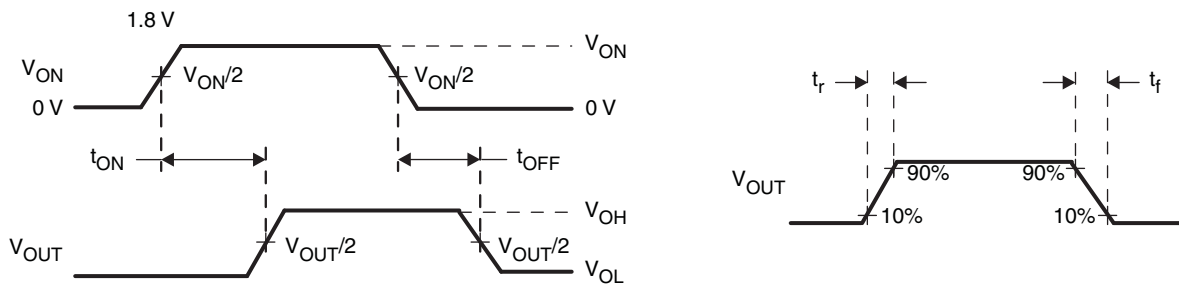


Figure 27. t_{OFF} Response

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

A. t_{rise} and t_{fall} of the control signal is 100 ns.

Figure 28. Test Circuit and t_{ON}/t_{OFF} Waveforms

APPLICATION INFORMATION

ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state so long as there is no fault. ON is active HI and has a low threshold making it capable of interfacing with low voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

Input Capacitor

To limit voltage drop or voltage transients, a capacitor needs to be placed between V_{IN} and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient, but higher values of C_{IN} can be used. When switching heavy loads, it is recommended to have an input capacitor about ten times higher than the output capacitor.

Output Capacitor

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} .

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN} , V_{OUT} , and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS22960DCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22960DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

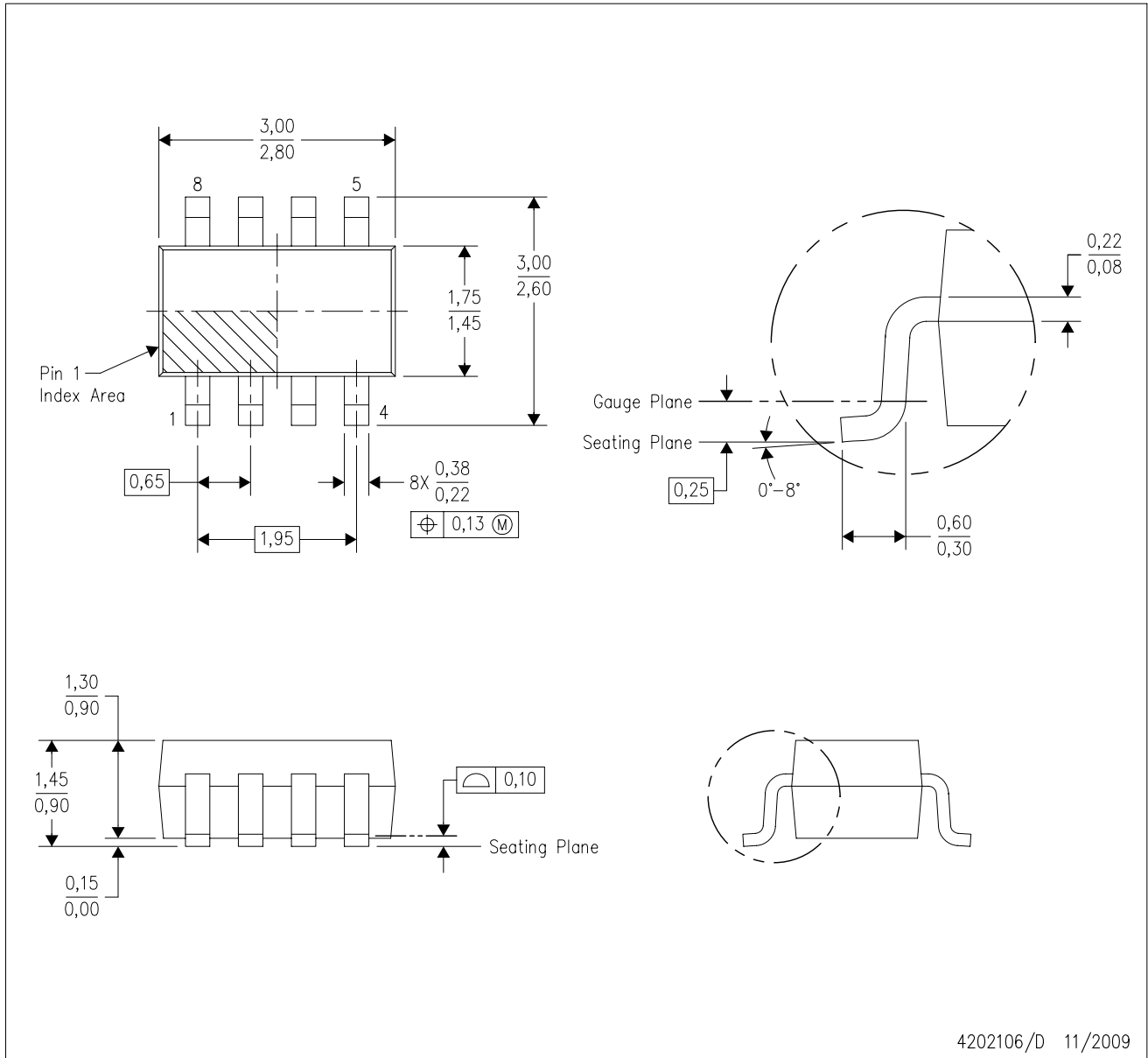


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22960DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0

DCN (R-PDSO-G8)

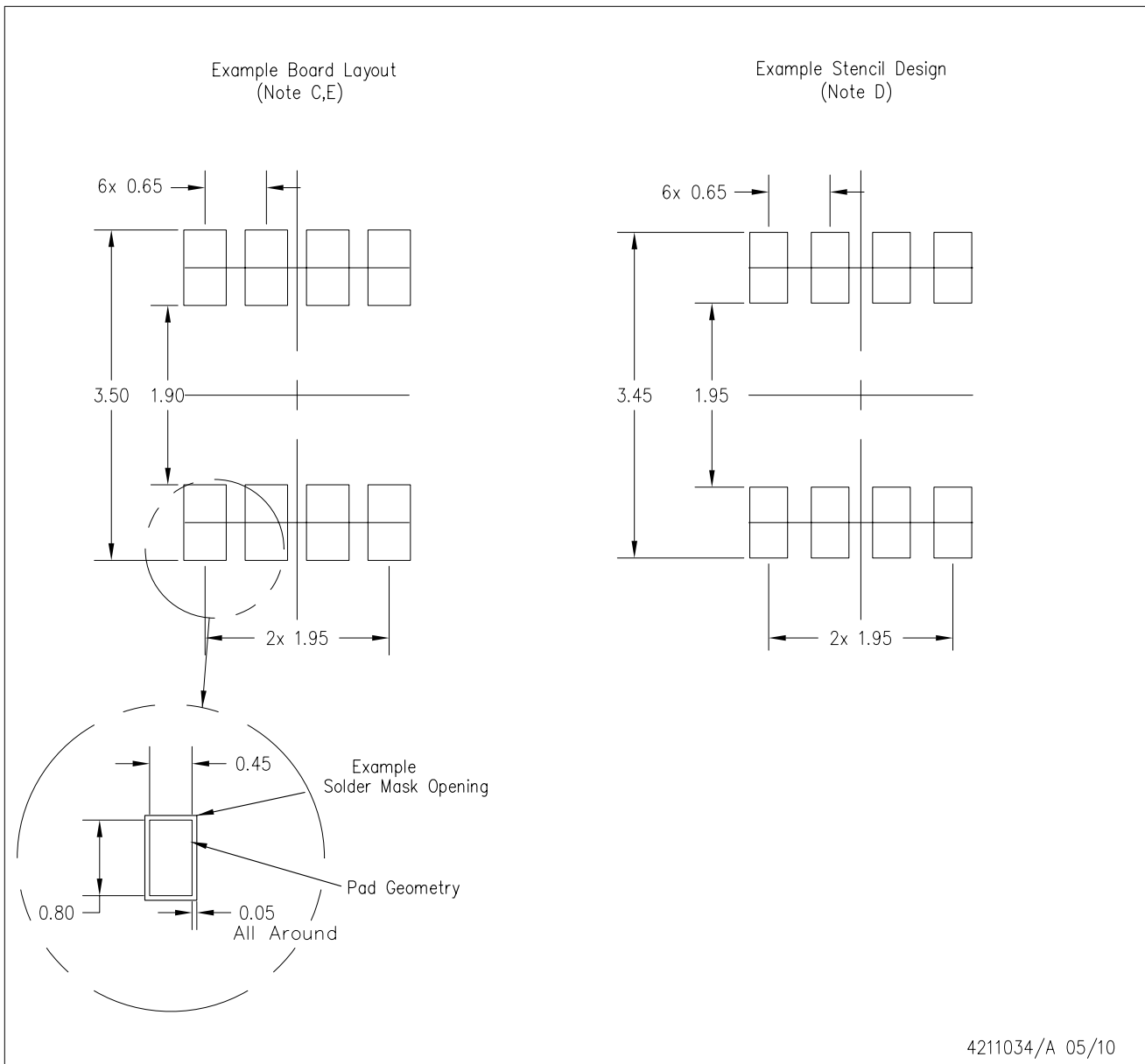
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
 - D. Package outline inclusive of solder plating.
 - E. A visual index feature must be located within the Pin 1 index area.
 - F. Falls within JEDEC MO-178 Variation BA.
 - G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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