

MOS FIELD EFFECT TRANSISTOR 2SK3402

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3402 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

• Low On-State Resistance

 $R_{DS(on)1}$ = 15 m Ω MAX. (Vgs = 10 V, ID = 18 A)

 $R_{DS(on)2} = 22 \text{ m}\Omega \text{ MAX.} \text{ (V}_{GS} = 4.0 \text{ V}, I_{D} = 18 \text{ A)}$

- Low Ciss : Ciss = 3200 pF TYP.
- Built-in Gate Protection Diode
- TO-251/TO-252 package

★ ORDERING INFORMATION

PART NUMBER	PACKAGE		
2SK3402	TO-251 (MP-3)		
2SK3402-Z	TO-252 (MP-3Z)		

(TO-251)

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	VDSS	60	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	I _{D(DC)}	±36	Α
Drain Current (pulse) Note1	D(pulse)	±144	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	40	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current Note2	IAS	35	Α
Single Avalanche Energy Note2	Eas	123	mJ

(TO-252)



Notes 1. PW \leq 10 μ s, Duty cycle \leq 1%

2. Starting Tch = 25°C, VdD = 30 V, Rg = 25 Ω , Vgs = 20 \rightarrow 0 V

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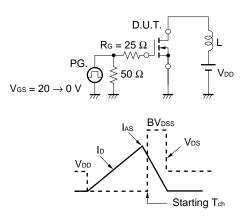


ETECTRICALOCITATION (TA = 25°C)

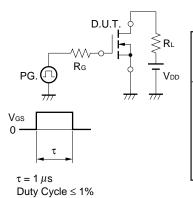
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 60 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μА
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	yfs	V _{DS} = 10 V, I _D = 18 A	13	27		S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10 V, I _D = 18 A		12	15	mΩ
	RDS(on)2	V _{GS} = 4.0 V, I _D = 18 A		15	22	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		3200		pF
Output Capacitance	Coss	V _{GS} = 0 V		520		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		270		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 18 A		36		ns
Rise Time	tr	V _{GS} = 10 V		310		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		170		ns
Fall Time	tf			180		ns
Total Gate Charge	QG	V _{DD} = 48 V		61		nC
Gate to Source Charge	Qgs	V _{GS} = 10 V		8.2		nC
Gate to Drain Charge	Q _{GD}	I _D = 36 A		17		nC
Body Diode Forward Voltage Note	V _F (S-D)	I _F = 36 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	trr	I _F = 36 A, V _{GS} = 0 V		48		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		89		nC

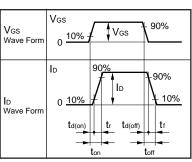
Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

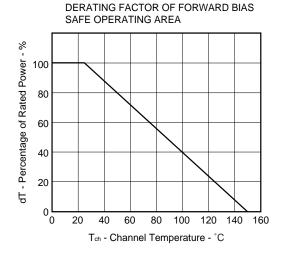


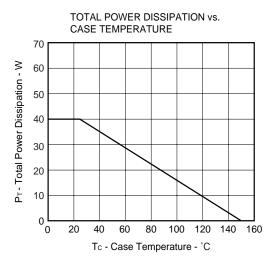


TEST CIRCUIT 3 GATE CHARGE

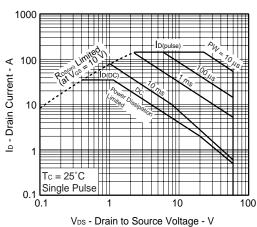


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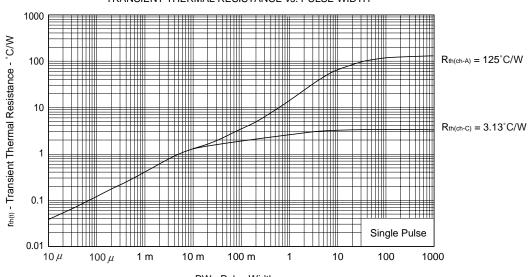




FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

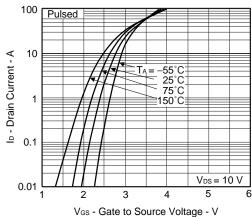


PW - Pulse Width - s

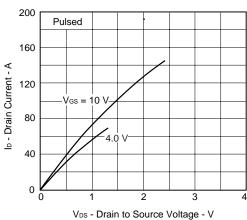
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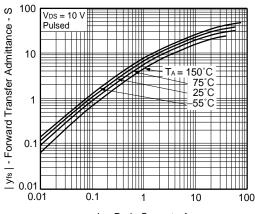
FORWARD TRANSFER CHARACTERISTICS



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

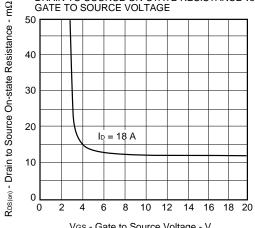


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



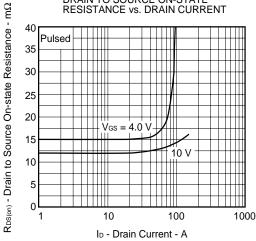
ID - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

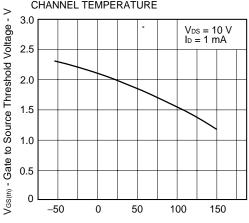


Vgs - Gate to Source Voltage - V

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

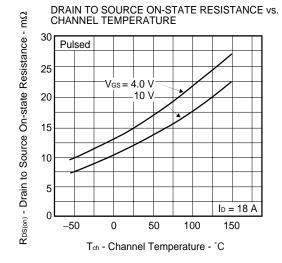


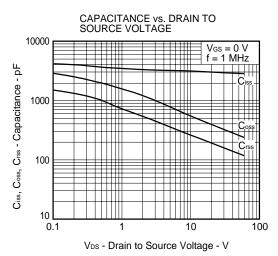
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

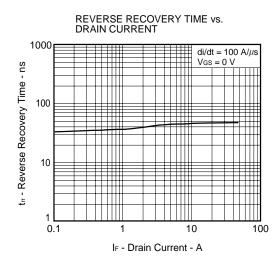


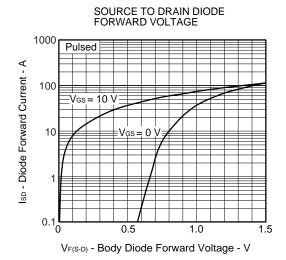
Tch - Channel Temperature - °C

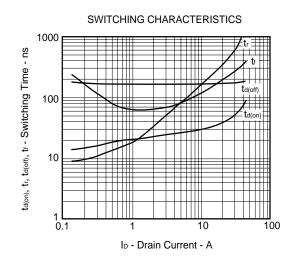


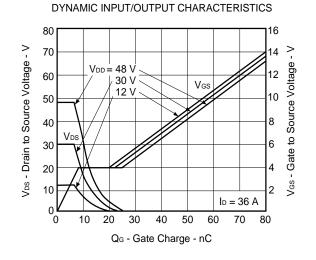




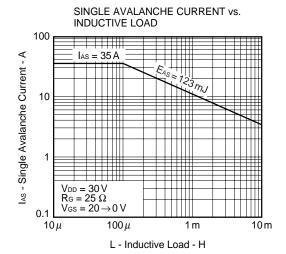


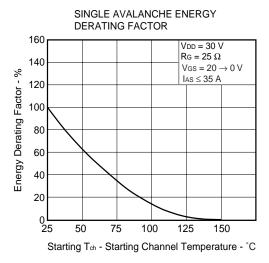






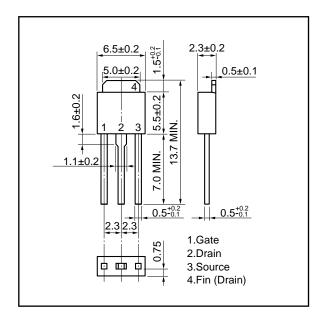




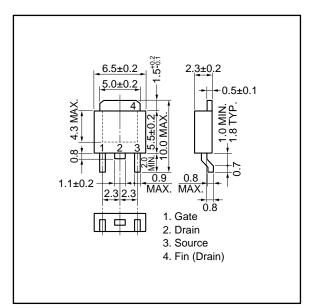




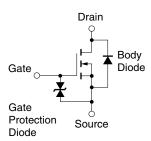
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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