



October 2001
Revised February 2002

74ALVCH16373 Low Voltage 16-Bit Transparent Latch with Bushold

General Description

The ALVCH16373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear to be transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in a high impedance state.

The ALVCH16373 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The 74ALVCH16373 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with output compatibility up to 3.6V.

The 74ALVCH16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

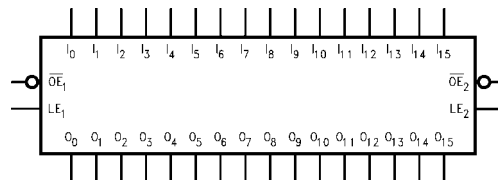
- 1.65V to 3.6V V_{CC} supply operation
- 3.6V tolerant control inputs and outputs
- Bushold on data inputs eliminates the need for external pull-up/pull-down resistors
- t_{PD} (I_n to O_n)
 - 3.6 ns max for 3.0V to 3.6V V_{CC}
 - 4.5 ns max for 2.3V to 2.7V V_{CC}
 - 6.8 ns max for 1.65V to 1.95V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up conforms to JEDEC JED78
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

Ordering Code:

Order Number	Package Number	Package Description
74ALVCH16373T	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

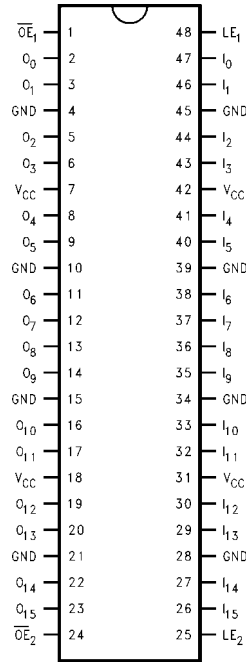
Logic Symbol



74ALVCH16373 Low Voltage 16-Bit Transparent Latch with Bushold

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Connection Diagram



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
LE _n	Latch Enable Input
I ₀ -I ₁₅	Bushold Inputs
O ₀ -O ₁₅	Outputs
NC	No Connect

Truth Tables

Inputs			Outputs
LE ₁	\overline{OE}_1	I ₀ -I ₇	O ₀ -O ₇
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O ₀

Inputs			Outputs
LE ₂	\overline{OE}_2	I ₈ -I ₁₅	O ₈ -O ₁₅
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O ₀

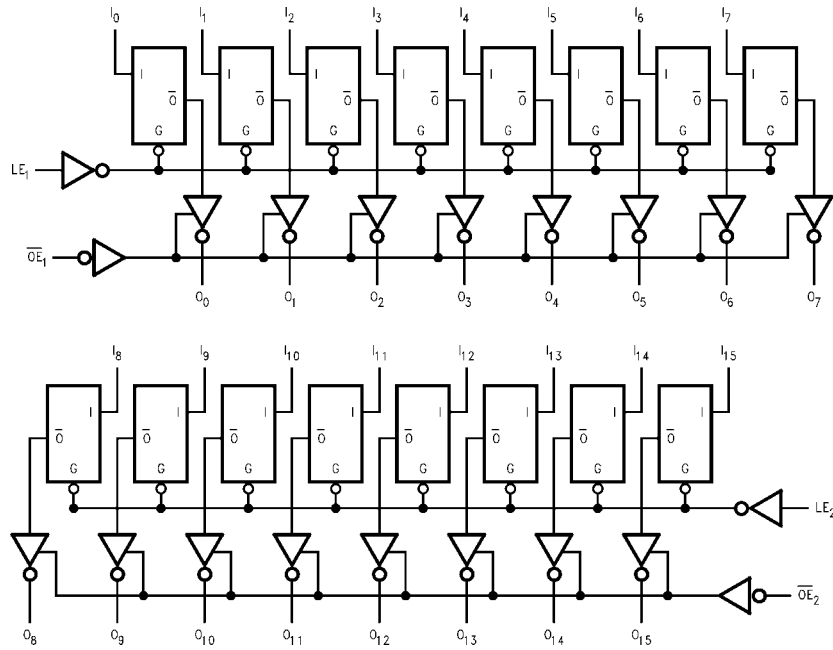
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, control inputs may not float)
 Z = High Impedance
 O₀ = Previous O₀ before HIGH-to-LOW of Latch Enable

Functional Description

The 74ALVCH16373 contains sixteen edge D-type latches with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time

its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on LE_n . The 3-STATE outputs are controlled by the Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW the standard outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 3)	
Supply Voltage (V_{CC})	-0.5V to +4.6V	Power Supply	
DC Input Voltage (V_I)	-0.5V to 4.6V	Operating	1.65V to 3.6V
Output Voltage (V_O) (Note 2)	-0.5V to $V_{CC} + 0.5V$	Input Voltage (V_I)	0V to V_{CC}
DC Input Diode Current (I_{IK})		Output Voltage (V_O)	0V to V_{CC}
$V_I < 0V$	-50 mA	Free Air Operating Temperature (T_A)	-40°C to +85°C
DC Output Diode Current (I_{OK})		Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_O < 0V$	-50 mA	$V_{IN} = 0.8V$ to $2.0V$, $V_{CC} = 3.0V$	10 ns/V
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA	Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	
DC V_{CC} or GND Current per Supply Pin (I_{CC} or GND)	± 100 mA	Note 2: I_O Absolute Maximum Rating must be observed.	
Storage Temperature Range (T_{STG})	-65°C to +150°C	Note 3: Floating or unused inputs must be held HIGH or LOW.	

DC Electrical Characteristics						
Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	$0.65 \times V_{CC}$ 1.7 2.0		V
V_{IL}	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		$0.35 \times V_{CC}$ 0.7 0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -4$ mA $I_{OH} = -6$ mA $I_{OH} = -12$ mA $I_{OH} = -24$ mA	1.65 - 3.6 1.65 2.3 2.7 3.0 3.0	$V_{CC} - 0.2$ 1.2 2 1.7 2.2 2.4		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 4$ mA $I_{OL} = 6$ mA $I_{OL} = 12$ mA $I_{OL} = 24$ mA	1.65 - 3.6 1.65 2.3 2.7 3		0.2 0.45 0.4 0.7 0.4 0.55	V
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		± 5.0	μA
$I_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current	$V_{IN} = 0.58V$ $V_{IN} = 1.07V$ $V_{IN} = 0.7V$ $V_{IN} = 1.7V$ $V_{IN} = 0.8V$ $V_{IN} = 2.0V$ $0 < V_O \leq 3.6V$	1.65 1.65 2.3 2.3 3.0 3.0 3.6	25 -25 45 -45 75 -75		μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		± 10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	μA

AC Electrical Characteristics										
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω								Units
		C _L = 50 pF				C _L = 30 pF				
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _W	Pulse Width	3.3		3.3		3.3		4.0		ns
t _S	Setup Time	1.1		1		1		2.5		ns
t _H	Hold Time	1.4		1.7		1.5		1.0		ns
t _{PHL} , t _{PLH}	Propagation Delay I _n to O _n	1.1	3.6		4.3	1	4.5	1.5	6.8	ns
t _{PHL} , t _{PLH}	Propagation Delay LE to O _n	1	3.9		4.6	1	4.9	1.5	7.8	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.0	4.7		5.7	1.0	6.0	1.5	9.2	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.4	4.1		4.5	1.2	5.1	1.5	6.8	ns
Capacitance										
Symbol	Parameter	Conditions	T _A = +25°C		Units					
			V _{CC}	Typical						
C _{IN}	Input Capacitance	Control	V _I = 0V or V _{CC}		pF					
		Data	V _I = 0V or V _{CC}							
C _{OUT}	Output Capacitance	V _I = 0V or V _{CC}		3.3	7	pF				
C _{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C _L = 50 pF		3.3	22	pF			
			f = 10 MHz, C _L = 50 pF		2.5	19				
		Outputs Disabled	f = 10 MHz, C _L = 50 pF		3.3	5				
			f = 10 MHz, C _L = 50 pF		2.5	4				

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AC Loading and Waveforms

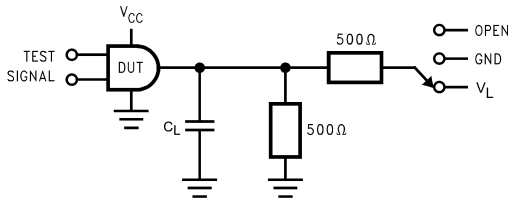


FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_L
t_{PZH} , t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: $f = 1\text{MHz}$; $t_r = t_f = 2\text{ns}$; $Z_0 = 50\Omega$)

Symbol	V_{CC}			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
V_Y	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
V_L	6V	6V	$V_{CC} \cdot 2$	$V_{CC} \cdot 2$

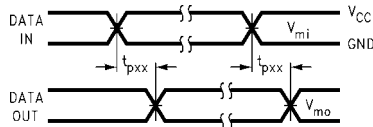


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

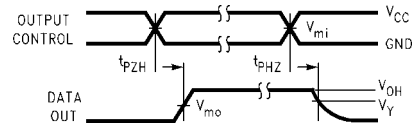


FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

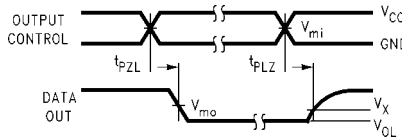


FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

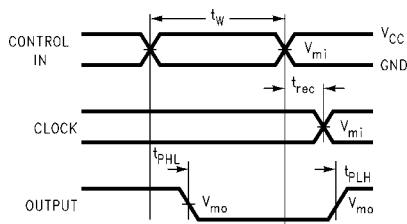


FIGURE 5. Propagation Delay, Pulse Width and t_{REC} Waveforms

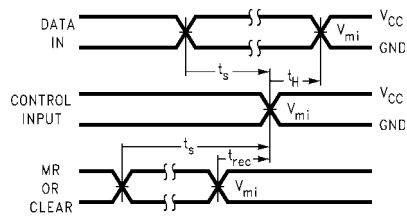


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

