REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19				

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY: DSCC Dr. Cenzo

DRAWING APPROVAL DATE: 26 AUGUST 1988

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, ERASEABLE, CMOS, PROGRAMMABLE LOGIC DEVICE

SIZE	CAGE CODE	
A	67268	5962-86864

SHEET 1 OF 19

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86864	01	L	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(see 6.4)	600 gate EPLD	55 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
L	D-9 (24-lead, 1.280" x 0.310" x 0.200"), dual-in-line package 1/
X	See figure 1, (28-lead, 0.485" x 0.485" x 0.190"), J-leaded chip carrier 1/

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-2.0 V dc to 7.0 V dc
Programming supply voltage (V_{PP})	-2.0 V dc to +13.5 V dc
DC input voltage (V_I) 2/	-0.5 V dc to V_{CC} +0.3 V dc
Power dissipation (P_D)	650 mW
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+200°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case L	See MIL-M-38510, appendix C
Case X	20° C/W 3/
DC supply current, (I_{CC} or I_{SS})	±100 mA
DC output current, (I_O) per pin	±25 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage (V_{IL})	-0.3 V dc to +0.8 V dc
Input high voltage (V_{IH})	+2.0 V dc to V_{CC} +0.3 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input rise time (T_R)	500 ns maximum
Input fall time (T_F)	500 ns maximum
Clock pins, rise time	100 ns maximum
Clock pins, fall time	100 ns maximum

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Minimum dc input voltage is -0.5 V dc. During transitions the inputs may undershoot to -2.0 V dc for periods less than 20 ns under no load conditions.
3/ When a thermal resistance values is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.2.1 Unprogrammed or erased device. The truth table for unprogrammed devices shall be as specified on figure 3.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range with the low standby power mode disabled.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Processing EPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manfacturer prior to delivery.

3.5.1 Erasure of EPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and table III.

3.5.3 Verification of erasure of programmability of EPLDS. When specified, devices shall be verified as either programmed to the specific pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc (unless otherwise specified)	Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level input voltage	V_{IH}		01	1, 2, 3	2.0	V_{CC} 2/ +0.3	V
Low level input voltage	V_{IL}		01	1, 2, 3	-0.3 2/	0.8	V
Low level output voltage	V_{OL}	I_{OL} = 4.0 mA	01	1, 2, 3		0.45	V
High level TTL output voltage	V_{OH}(TTL)	I_{OH} = -4.0 mA	01	1, 2, 3	2.4		V
High level CMOS output voltage	V_{OH}(CMOS)	I_{OH} = -2.0 mA	01	1, 2, 3	3.84		V
Input leakage current	I_I	$V_I = V_{CC}$ or GND	01	1, 2, 3	-10	10	µA
3-state output off current	I_{OZ}	$V_O = V_{CC}$ or GND	01	1, 2, 3	-10	10	µA
V_{CC} supply current 3/	I_{CC}	V_{IN} = 0 V or V_{CC} f = 1.0 MHz	01	1, 2, 3		60	mA
Input capacitance	C_{IN}	V_{IN} = 0 V dc; f = 1.0 MHz measured from pin to V_{SS} see 4.3.1c	01	4		20	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V dc; f = 1.0 MHz measured from pin to V_{SS} see 4.3.1c	01	4		20	pF
Clock pin capacitance	C_{CLK}	V_{IN} = 0 V dc; f = 1.0 MHz measured from pin to V_{SS} see 4.3.1c	01	4		20	pF
Clk/V_{PP} capacitance	C_{VPP}	V_{OUT} = 0 V dc; f = 1.0 MHz measured from pin to V_{SS} see 4.3.1c	01	4		50	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc (unless otherwise specified)	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Input to non-registered output 4/	t_{PD}	C_L = 50 pF (see figures 4 and 5)	01	9, 10, 11		55	ns
Input to output enable 4/	t_{PZX}	C_L = 50 pF (see figures 4 and 5)	01	9, 10, 11		55	ns
Input to output disable 4/ 5/	t_{PXZ}	C_L = 5 pF (see figures 4 and 5) output change = 500 mV	01	9, 10, 11		55	ns
Asynchronous output clear time 4/	t_{CLR}	C_L = 50 pF (see figures 4 and 5)	01	9, 10, 11		60	ns
Input setup time 4/	t_{SU}	(see figures 4 and 5)	01	9, 10, 11	45		ns
Input hold time 4/	t_H		01	9, 10, 11	0		ns
Clock high time 2/	t_{CH}		01	9, 10, 11	22.5		ns
Clock low time 2/	t_{CL}		01	9, 10, 11	22.5		ns
Clock to output delay	t_{CO1}		01	9, 10, 11		30	ns
Minimum clock period (register output feedback to register input, 3/ 6/ internal path)	t_{CNT}		01	9, 10, 11		65	ns
Maximum frequency ($1/t_{SU}$) 4/ 7/ 8/	f_{MAX}		01	9, 10, 11	22.2		MHz
Minimum clock period ($t_{SU} + t_{CO1}$)	t_{P2}		01	9, 10, 11		75	ns
Internal maximum frequency ($1/t_{CNT}$) 3/ 9/	f_{CNT}		01	9, 10, 11	15.4		MHz
Asynchronous input 2/ 4/ setup time	t_{ASU}		01	9, 10, 11	10		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc (unless otherwise specified)	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Asynchronous input 2/ 4/ hold time	t_{AH}	See figures 4 and 5	01	9, 10, 11	15		ns
Asynchronous clock high 2/ time	t_{ACH}		01	9, 10, 11		22.5	ns
Asynchronous clock low 2/ time	t_{ACL}		01	9, 10, 11		22.5	ns
Asynchronous clock to output delay 2/ 4/	t_{ACO1}		01	9, 10, 11		65	ns
Asynchronous minimum clock period (register output feedback to register input, 3/ 10/ internal path)	t_{ACNT}		01	9, 10, 11		65	ns
Asynchronous internal maximum frequency ($1/t_{ACNT}$) 11/	f_{ACNT}		01	9, 10, 11	15.4		MHz

1/ Screening and characterization of ac delay parameters is typically conducted while operating at less than maximum frequency.

2/ May not be tested, but shall be guaranteed to the limits specified in table I.

3/ Specified with device programmed as a 16 bit counter and no output loading.

4/ All array-dependent delays are specified for an XOR pattern. This pattern involves two product terms and two pure inputs with all other product terms in the macrocell held low by one EPROM pulldown. Other patterns may result in longer delays than those specified. Delays involving only one product term such as t_{PXZ} are specified for an "XOR-like" pattern which involves one pure input switching at a time, and the single product term.

5/ Not tested directly, but guaranteed by testing of t_{PD}.

6/ Tested using register output feedback to register input test mode, correlated to a 16 bit counter.

7/ f_{MAX} represents the highest frequency for pipelined data.

8/ Not tested directly, but derived from t_{SU}.

9/ Not tested directly, but derived from t_{CNT}.

10/ Not tested directly, but guaranteed by testing of t_{CNT}.

11/ Not tested directly, but derived from t_{ACNT}.

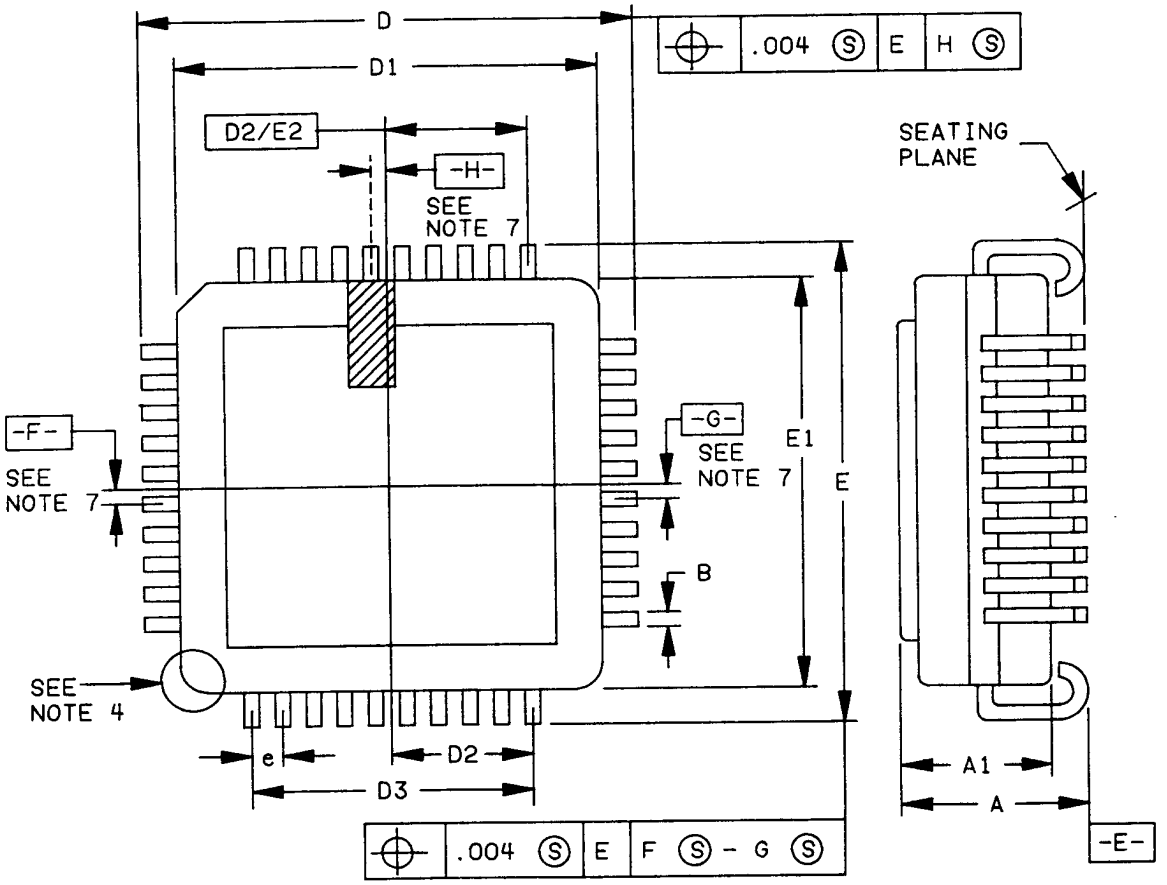
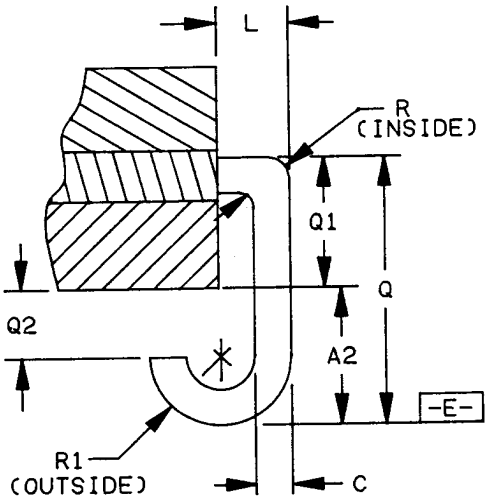


FIGURE 1. Quad cerpac leaded chip carrier.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86864
		REVISION LEVEL	SHEET 8

Case outline

Symbol	Min	Max	Note	Symbol	Min	Max	Note
A	.085	.190	5	e	.050	BSC	
A1	.075	.155		L	.015	REF.	
A2	.035	REF.	8	Q	.095	.115	
B	.018	.022		Q1	.060	.070	
C	.007	.011		Q2	.003	--	
D/E	--	.485		R	.005	--	
D1/E1	.440	.460	6	R1	.030	--	
D2/E2	.150	BSC		ND	7		2, 7
D3/E3	.300	BSC		NE	7		2, 7
				N	28	--	2, 3



NOTES:
1. The controlling dimension is in inch.
2. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminal along the sides of length "D" and "E" respectively.
3. The index feature for terminal 1 identification, optical orientation or handling purposes shall be within the shaded index area shown on plane 1. Terminal identification is optional on the surface closest to the seating plane.
4. The corner shape (square, notch, radius, etc.) may vary at the vendors option from that shown on the drawing.
5. Packages shall be constructed of a minimum of two ceramic layers.
6. This dimension allows for package edge anomalies caused by material protrusion, such as rough ceramic, misaligned ceramic layers and/or lids, meniscus, and/or glass overrun.
7. When the number of terminals per side is even, datums F-G and -H are located at the terminal array centers. When the number of terminals per side is odd, datums F-G and -H- are located at the centers of the center terminals. The measurement point for establishing these datums is the package/lead interface.
8. The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall be .008 inch TIR.

FIGURE 1. Quad cerpac leaded chip carrier - Continued.

	Terminal symbol	
Device	01	
Case	L	X
Terminal number		
1	CLK1/PGM	V_{CC}
2	INPUT	CLK1/PGM
3	I/O	INPUT
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	INPUT	NC
12	GND	I/O
13	CLK2/V_{PP}	INPUT
14	INPUT	GND
15	I/O	GND
16	I/O	CLK2/V_{PP}
17	I/O	INPUT
18	I/O	I/O
19	I/O	NC
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	INPUT	I/O
24	V_{CC}	I/O
25	--	I/O
26	--	I/O
27	--	INPUT
28	--	V_{CC}

FIGURE 2. Terminal connections.

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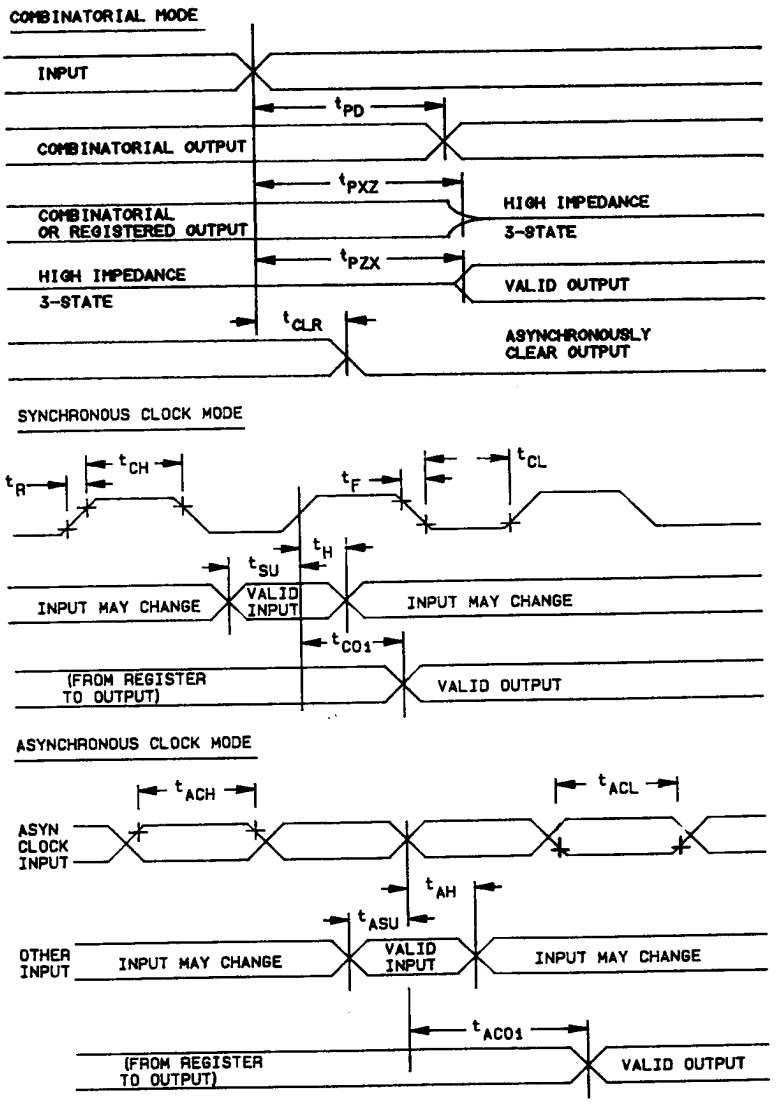
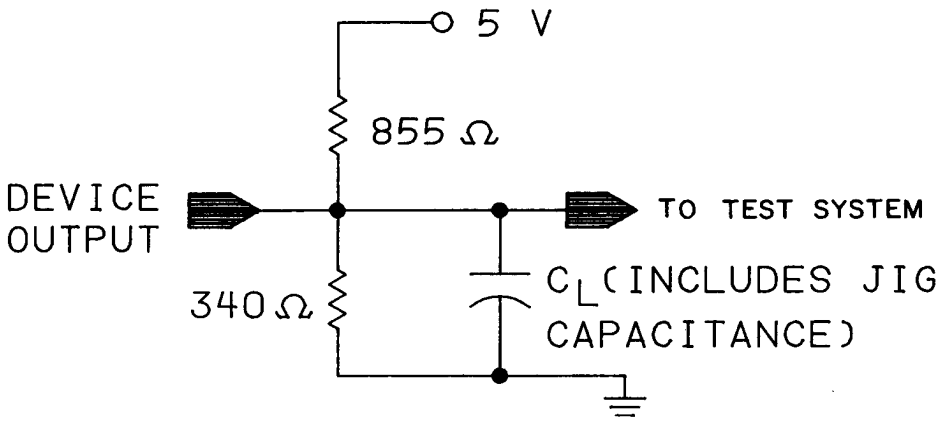
Mode	CLK 2/Vpp	CLK 1/PGM	I/O	Input
Normal operation	V_{IL} or V_{IH} (clock)	V_{IL} or V_{IH} (clock)	defined by application	V_{IL} or V_{IH} (data input)
Program	(Programming) supply	V_{ILP} (program pulse)	V_{ILP} or V_{IHP} (data input)	V_{ILP} to V_{IHP} (address)
Verify	Don't care	(Verify control)	(data out)	V_{ILP} to V_{IHP} (address)

FIGURE 3. Truth table (unprogrammed).



NOTES: t_R and t_F = 6 ns maximum
t_{CL} and t_{CH} are specified at 0.3 V and 2.7 V respectively all other timings are at 1.5 V
input levels are at 0 V and 3 V

FIGURE 4. Timing waveforms.



Device input rise and fall times ≤ 6 ns.

FIGURE 5. Test load circuit.

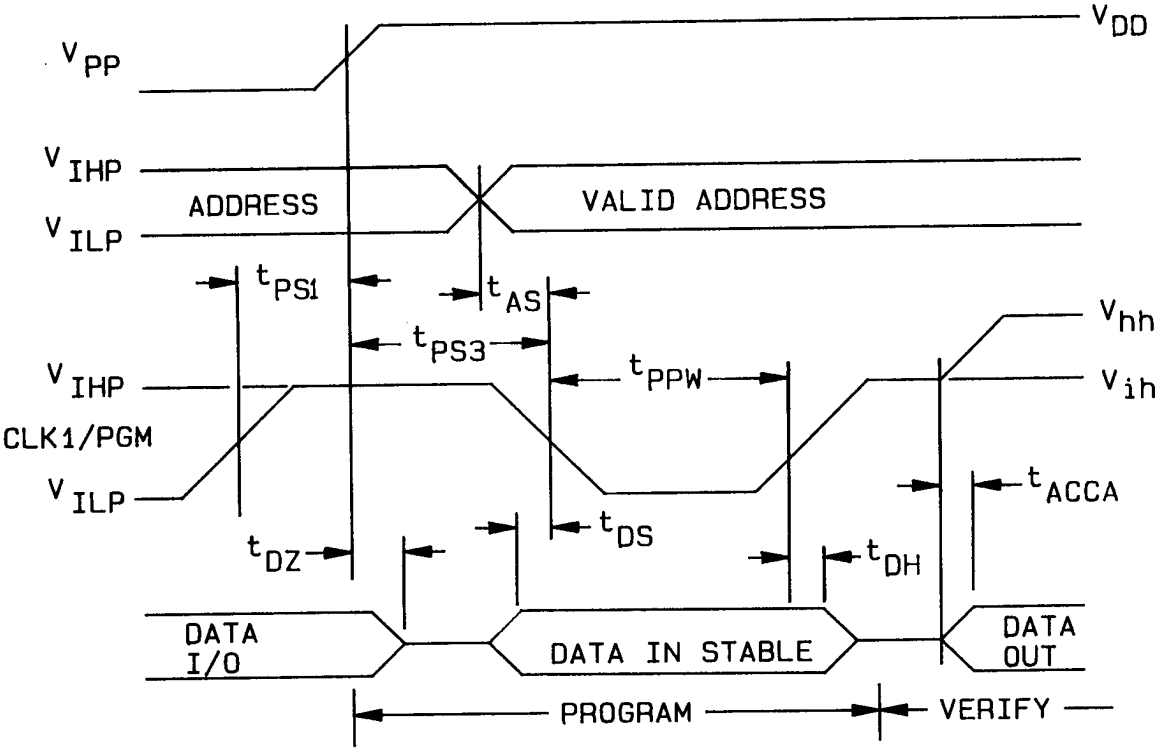


FIGURE 6. Programming waveform.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure (may be performed prior to the Internal visual inspection of method 5004 at the discretion of the manufacturer) and shall consist of the following steps:

Margin Test Method

(1) Each device shall be verified to be erased and subjected to a full functional test. Each device shall then have all bit locations (except the security bit) programmed and verified.

(2) Each device shall then be subjected to an unbiased retention bake at 140°C for 72 hours minimum (or equilavent time and temperature implied by an activation energy of 0.4 eV).

(3) After the retention bake, each device shall again be verified. Each device shall be electrically tested with guardbanding. A margin voltage of V_{CC} = 5.8 V dc shall be used, and each programmed bit shall be verified to have maintained the proper logic state.

(4) Any device containing a bit which does not verify as programmed, or erased, as applicable, or which does not maintain the proper logic state during margin testing, shall be rejected and shall not be delivered to this drawing.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (capacitance measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 functional tests shall verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedures. The recommended erasure procedure is exposing to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of fifteen (15) Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming charactertistics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure all bits are in the "0" state. A programmed "1" can be changed to a "0" by ultraviolet light erasure (see 4.4).

c. Programming occurs when the V_{pp} is at 12.5 V and PGM pulse is at 12.5 V.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8, 10

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

TABLE III. Programming characteristics.

Parameter	Symbol	Conditions 1/ T_A = +25°C ±5°C	Limits			Units
			Min	Recommended	Max	
Programming supply voltage	V_{PP}		12.5	12.75	13.0	V
High-level control voltage	V_{hh}		11.5	12.75	13.0	V
Operating supply voltage	V_{CC}		4.7	5.0	5.2	V
Programming supply voltage	V_{CC}		5.75	6.0	6.25	V
Low level program/verify input voltage	V_{ILP}				0.4	V
High level program/verify input voltage	V_{IHP}		3.5			V
Programming supply current	I_{PP}				65	mA
Operating supply current	I_{CC}				70	mA
Base program pulse width	t_{PPW}		0.95	1.0	1.20	ms
Set-up time CLK1	t_{PS1}			2		µs
Set-up time CLK1	t_{PS3}			2		µs
Address set-up time	t_{AS}			2		µs

See footnote at end of table.

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TABLE III. Programming characteristics - Continued.

Parameter	Symbol	Conditions 1/ T_A = +25°C ±5°C	Limits			Units
			Min	Recommended	Max	
Data to 3-state time	t_{DZ}			2		µs
Data-input set-up time	t_{DS}			2		µs
Data-input hold time	t_{DH}			2		µs
Data-output delay time	t_{ACCA}			2		µs

1/ Parameters not specified on figure 6 shall be specified in the programming development system.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8686401LX	67183 34649	EP600DM883B MD5C060-55/B
5962-8686401XX	67183	EP600JM883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
67183	Altera Corporation 3525 Monroe Street Santa Clara, CA 95051
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051