

LOW DROP VOLTAGE REGULATOR

Table 2. Pin Function

SO8 N°	SO20 N°	Pin Name	Function
1	1	En	Enable input If high, regulator, watchdog and reset are operating. If low, regulator, watchdog and reset are shut down.
2	4	gnd	Ground reference
	5,6,15,16	gnd	Ground These pins are to be connected to a heat spreader electrically grounded
3	7	Res	Reset output. It is pulled down when output voltage drops below Vo_th or frequency at Wi is too low.
4	10	Vcr	Reset timing adjust A capacitor between Vcr pin and gnd sets the reset delay time (trd)
5	11	Vcw	Watchdog timer adjust A capacitor between Vcw pin and gnd sets the time response of the watchdog monitor.
6	14	Wi	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
7	17	Vo	Voltage regulator output Output capacitor >100nF is needed for regulator stability
8	20	Vs	Supply voltage Supply capacitor (e.g. 200nF) is needed for regulator stability.
	2, 3, 8, 9, 12, 13, 18, 19	N. C.	not connected

Figure 3. Pins Connection (Top view)

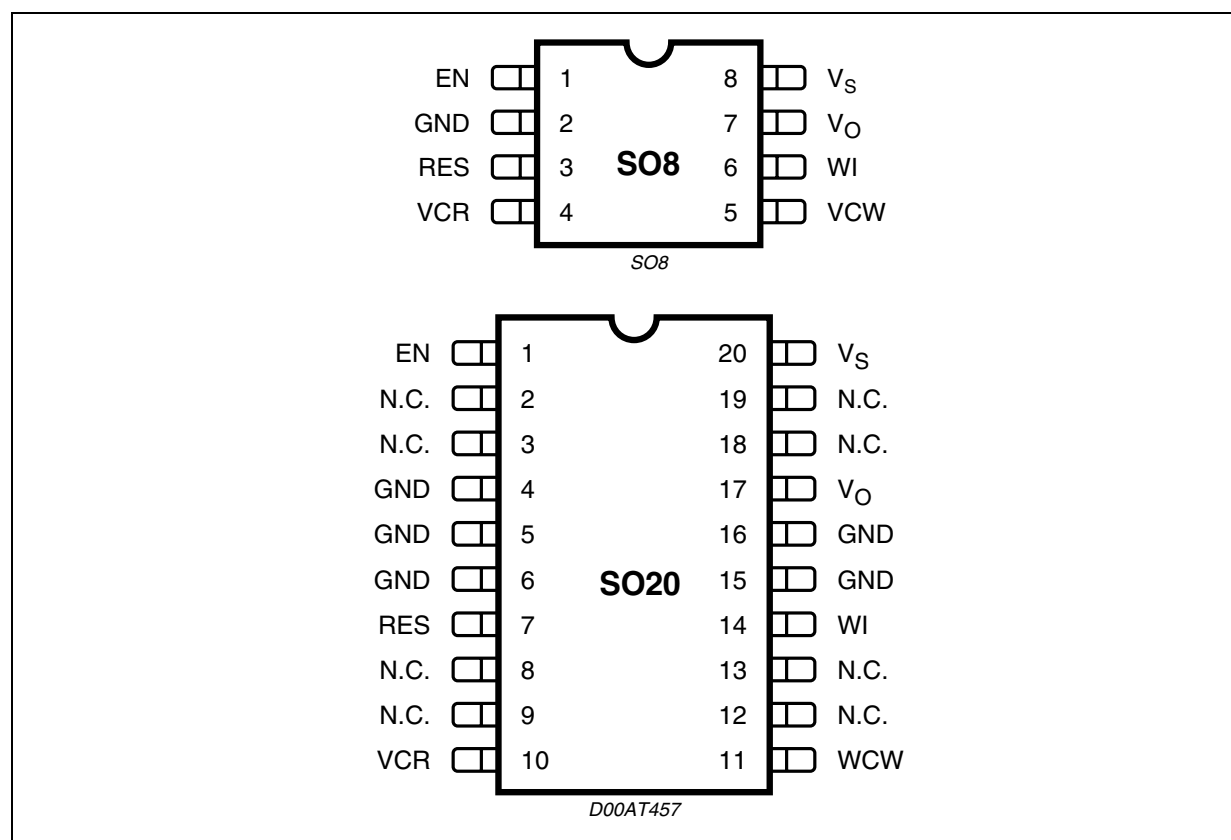


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{vsdc}	DC supply voltage	-0.3 to 40	V
I _{vsdc}	Input current	internally limited	
V _{vo}	DC output voltage	-0.3 to 6	V
I _{vo}	DC output current	internally limited	
V _{wi}	Watchdog input voltage	-0.3 to V _{vo} +0.3	V
V _{od}	Open drain output voltage (RES)	-0.3 to V _{vo} +0.3	V
I _{od}	Open drain output current (RES)	internally limited	
V _{cr}	Reset delay voltage	-0.3 to V _{vo} +0.3	V
V _{cw}	Watchdog delay voltage	-0.3 to V _{vo} +0.3	V
V _{en}	Enable input voltage	-0.3 to 40	V
T _j	Junction temperature	-40 to 150	°C
VESD	ESD voltage level (HBM-MIL STD 883C)	±2	kV

Note: 1. Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 4. Thermal Data

Symbol	Parameter	SO8	SO16+2+2	Unit
R _{th j-amb}	Thermal resistance Junction to Ambient	130 to 180	50 to 80	°C/W

Table 5. Electrical Characteristics

(V_s = 5.6V to 31V, T_j = -40°C to +150°C unless otherwise specified)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GENERAL							
V _s , V _o	I _q	Quiescent current	V _s = 13.5V, I _o = 150mA, enable high all I/O currents = 0		1.5	3	mA
V _s , V _o	I _q	Quiescent current	V _s = 13.5V, I _o = 0mA, enable high all I/O currents = 0		100	200	μA
V _s , V _o	I _q	Quiescent current	V _s = 13.5V, I _o = 0mA, enable low all I/O currents = 0		6	20	μA
	T _w	Thermal protection temperature		150		190	°C
	T _{w_hy}	Thermal protection temperature hysteresis			10		°C

Table 5: Electrical Characteristics (continued)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLTAGE REGULATOR							
V _o	V _{o_ref}	Output voltage	V _s = 5.6 to 31V I _o = 1 to 150mA	4.90	5.00	5.10	V
V _o	I _{short}	Output short circuit current ⁽¹⁾	V _s = 13.5V	150	280	400	mA
V _o	I _{lim}	Output current limitation ⁽¹⁾	V _s = 13.5V	150	320	500	mA
V _s , V _o	V _{line}	Line regulation voltage	V _s = 5.6 to 31V I _o = 1 to 150mA			25	mV
V _o	V _{load}	Load regulation voltage	I _o = 1 to 150mA			25	mV
V _s , V _o	V _{dp}	Drop voltage	I _o = 150mA		200	400	mV
V _s , V _o	SVR	Ripple rejection ⁽²⁾	f _r = 100 Hz	55			dB
RESET							
R _{es}	V _{res_l}	Reset output low voltage	R _{ext} = 5kΩ to V _o , V _o > 1V			0.4	V
R _{es}	I _{res_h}	Reset output high leakage current	V _{res} = 5V			1	μA
R _{es}	R _{p_u}	Internal Pull up resistance	with respect to V _o	12	25	50	kΩ
R _{es}	V _{o_th}	Reset threshold voltage	V _s = 5.6 to 31V I _o = 1 to 150mA	6% below V _{o_ref}	8% below V _{o_ref}	10% below V _{o_ref}	
V _{cr}	V _{rhth}	Reset timing high threshold	V _s = 13.5V	44% V _{o_ref}	47% V _{o_ref}	50% V _{o_ref}	
V _{cr}	V _{rlth}	Reset timing low threshold	V _s = 13.5V	10% V _{o_ref}	13% V _{o_ref}	16% V _{o_ref}	
V _{cr}	I _{cr}	Charge current	V _s = 13.5V	8	17	30	μA
V _{cr}	I _{dr}	Discharge current	V _s = 13.5V	8	17	30	μA
R _{es}	t _{rr_2}	Reset delay time (3)	V _o = V _{o_th} -100mV	100	250	700	μs
R _{es}	t _{rd}	Reset pulse delay	V _s = 13.5V, C _{tr} = 1nF	65		150	ms
WATCHDOG							
W _i	V _{ih}	Input high voltage	V _s = 13.5V	3.5			V
W _i	V _{il}	Input low voltage	V _s = 13.5V			1.5	V
W _i	V _{ih}	Input hysteresis	V _s = 13.5V		300		mV
W _i	I _i	Pull down current	V _s = 13.5V		10	20	μA
V _{cw}	V _{whth}	High threshold	V _s = 13.5V	2.20	2.35	2.50	V
V _{cw}	V _{wlth}	Low threshold	V _s = 13.5V	0.50	0.65	0.80	V

ELECTRICAL CHARACTERISTICS (continued)

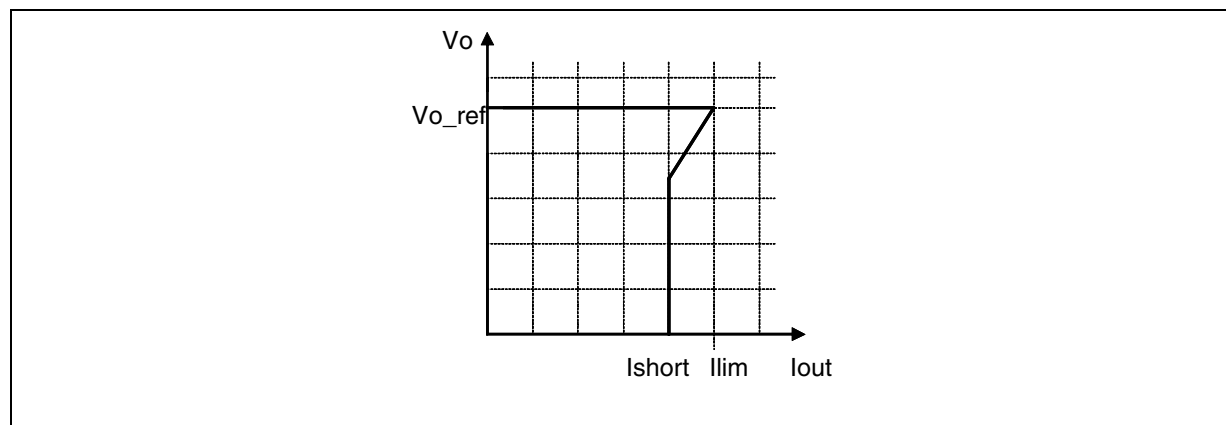
Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _{cw}	I _{cwc}	Charge current	V _s = 13.5V, V _{cw} = 0.1V	4	7.5	14	μA
V _{cw}	I _{cwd}	Discharge current	V _s = 13.5V, V _{cw} = 2.5V	1.0	2.4	4.5	μA
V _{cw}	T _{wop}	Watchdog period	V _s = 13.5V, C _{tw} = 47nF	25	50	90	ms
R _{es}	t _{wol}	Watchdog output low time	V _s = 13.5V, C _{tw} = 47nF	6	10	22	ms
ENABLE							
E _n	V _{en_l}	Enable input low voltage				1	V
E _n	V _{en_h}	Enable input high voltage		3			V
E _n	V _{en_hy}	Enable input hysteresis		700	1000	1100	mV
E _n	I _{leak}	Pull down current	E _n = 5V	2	10	20	μA

Note: 1. see fig4 (behavior of output current versus regulated voltage Vo)
2. guaranteed by design
3. When Vo becomes lower than 4V, the reset reaction time decreases down to 2μs assuring a faster reset condition in this particular case.

2 VOLTAGE REGULATOR

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure a low drop-out voltage at current up to 150mA is achieved. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. A short circuit protection to GND is provided.

Figure 4. Behavior of output current versus regulated voltage Vo (see a.m. Note 1)



3 RESET

The reset circuit monitors the output voltage V_o . If the output voltage drops below V_{o_th} then Res becomes low with a delay time t_{rr} . Real t_{rr} value changes as a non-linear function of $\Delta(V_{o_th} - V_o)$. The reset low signal is guaranteed for an output voltage V_o greater than 1V.

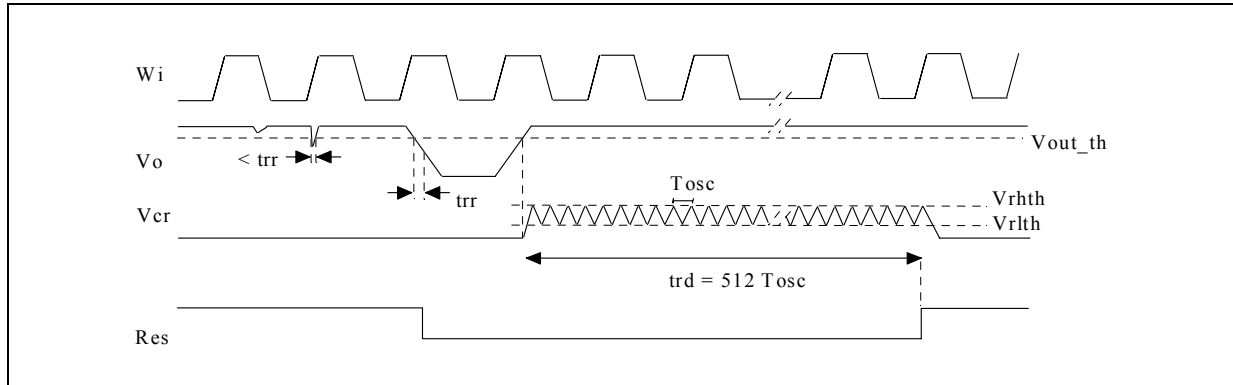
When the output voltage becomes higher than V_{o_th} then Res goes high with a delay t_{rd} . This delay is obtained by 512 periods of an oscillator (see fig. 5). The oscillator period is given by:

$$T_{osc} = \frac{[(V_{rth} - V_{rlth}) \cdot C_{tr}]}{I_{cr}} + \frac{[(V_{rth} - V_{rlth}) \cdot C_{tr}]}{I_{dr}}$$

and reset pulse delay t_{rd} is given by:

$$t_{rd} = 512 \times T_{osc}$$

Figure 5. Reset Time Diagram.



4 WATCHDOG

The watchdog input W_i monitors a connected microcontroller. If pulses are missing, the reset output Res is set to low. The pulse sequence time can be set within a wide range through the external capacitor C_{tw} . The watchdog circuit discharges the capacitor C_{tw} with the constant current I_{cwd} . If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this reset, the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth} . In order to calculate the minimum time T_{dis} during which the microcontroller must generate the positive edge, the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times T_{dis}$$

Each W_i positive edge switches the current source from discharging to charging; the same happens when the lower V_{wlth} threshold is reached. When the voltage reaches the upper threshold V_{whth} the current switches from charging to discharging. The result is a saw tooth voltage at the watchdog timer capacitor C_{tw} .

Figure 6. Watchdog time diagram

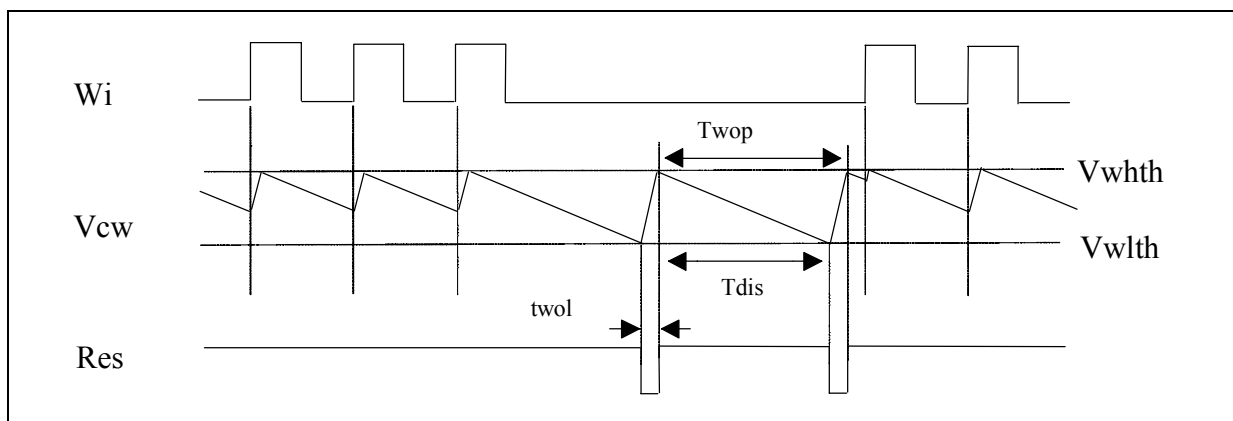


Figure 7. SO-8 Mechanical Data & Package Dimensions

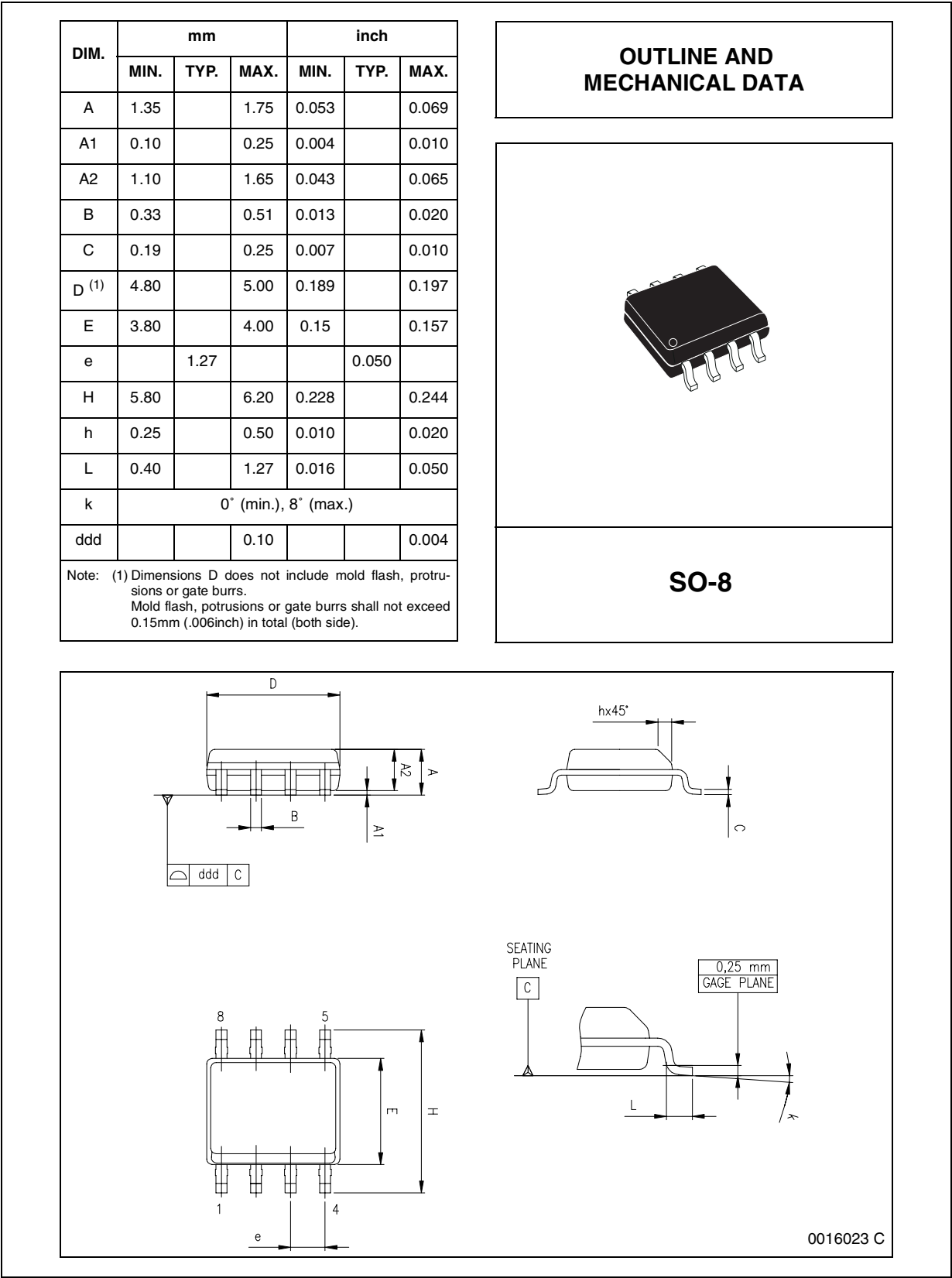
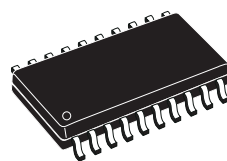


Figure 8. SO-20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D ⁽¹⁾	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20

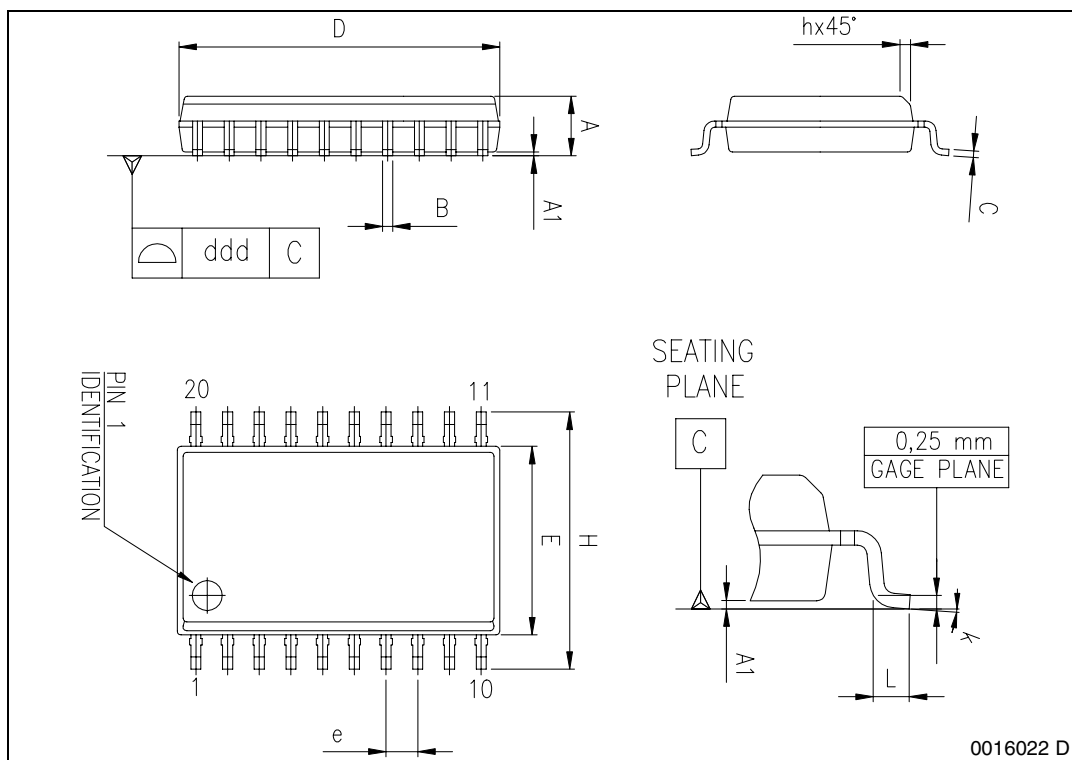


Table 6. Revision History

Date	Revision	Description of Changes
June 2004	3	Changed the values of the parameter "Reset timing high/low threshold.
July 2004	4	Pin Connection SO-20 changed. Changed some textes in the Features and table 2. Changed some values in the tables 3, 4 and 5. Changed some textes in the sections 2, 3 and 4.
October 2004	5	Changed from Product Preview to final datasheet.
February 2006	6	Modified the orderable part numbers for Tape & Reel.

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