

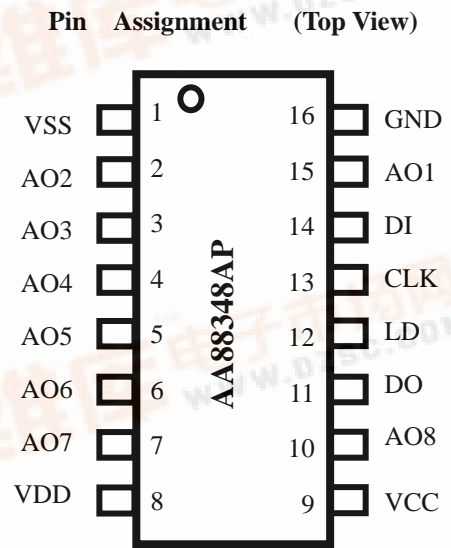


PRELIMINARY

8-BIT DAC

■ **FEATURE**

- 12 bits serial data input(3 wire serial data transfer method, DI, CLK, LD)
- R-2R resistor ladder used for D/A conversion
- 8 channels with 8-bit resolution monotonic D/A converted
- 8 channel buffer operational amplifiers operating in the full voltage range from VCC to GND only if VDD=VCC and VSS=GND
- Max. 10 MHz serial digital data input
- Serial I/O for cascade application
- Max. 1.0 mA output drive/sink current
- Two separate power supply/ground lines for system and analog power supply
- Single +5 V system power supply





■ **PIN DESCRIPTION**

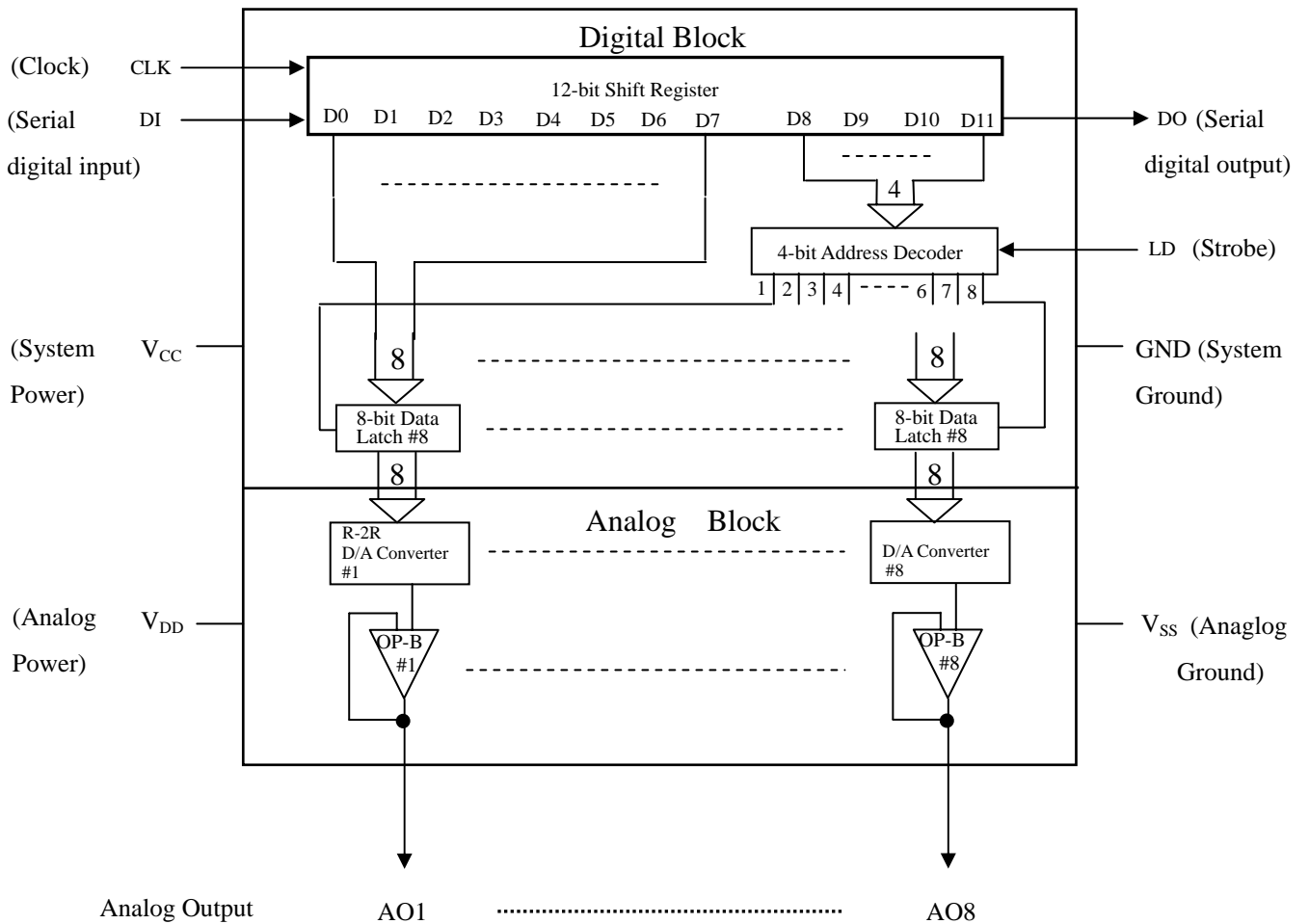
Symbol	Pin No.	Type	Name & Function
VCC	9	—	+5V system power supply pin
GND	16	—	System ground pin
VDD	8	—	Analog power supply pin
VSS	1	—	Analog ground pin
CLK	13	I	Serial clock input pin. At its rising edge, DI data shift into the Shift-Register.
LD	12	I	Data Strobe pin. When it's on high, upper 4-bit and lower 8-bit of the 12-bit in the Shift-Register be latched into the Address Decoder and the Data-Latch, respectively
Data Input/Output			
DI	14	I	Serial Digital Data input pin
DO	11	O	Serial Digital Data output pin. Output from the 12 th data in the Shift-Register
DAC Output			
AO1	15	O	8-bit D/A converter outputs Output range is from VSS to VDD
AO2	2	O	
AO3	3	O	
AO4	4	O	
AO5	5	O	
AO6	6	O	
AO7	7	O	
AO8	10	O	



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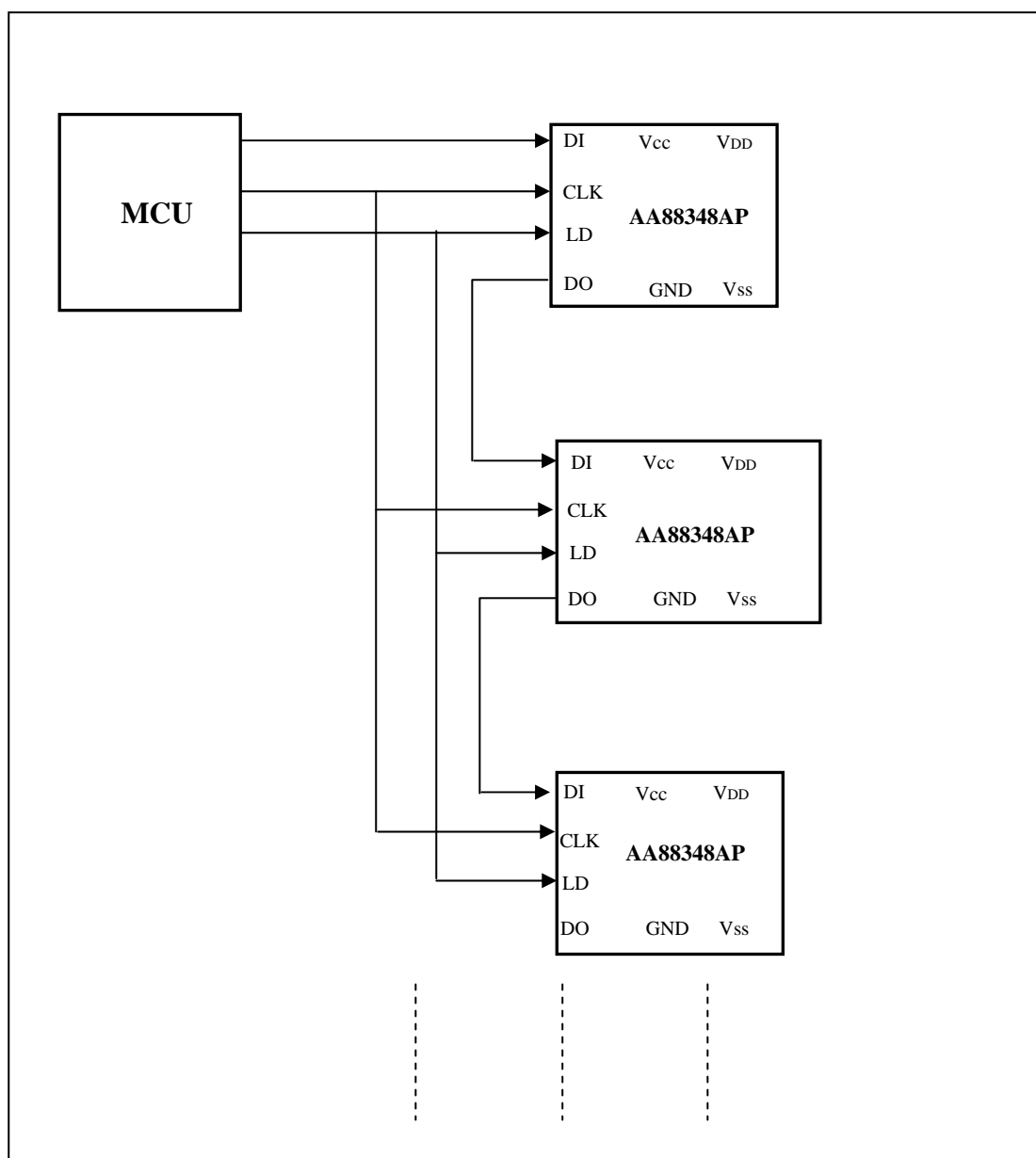
■ BLOCK DIAGRAM



- * Vcc and GND are for digital block and operational amplifier buffer block
- * VDD, VSS are only for Analog block except operational amplifier buffer block
- * $V_{SS} + 2V \leq V_{DD} \leq V_{CC}$
- * $GND \leq V_{SS} \leq V_{DD} - 2V$



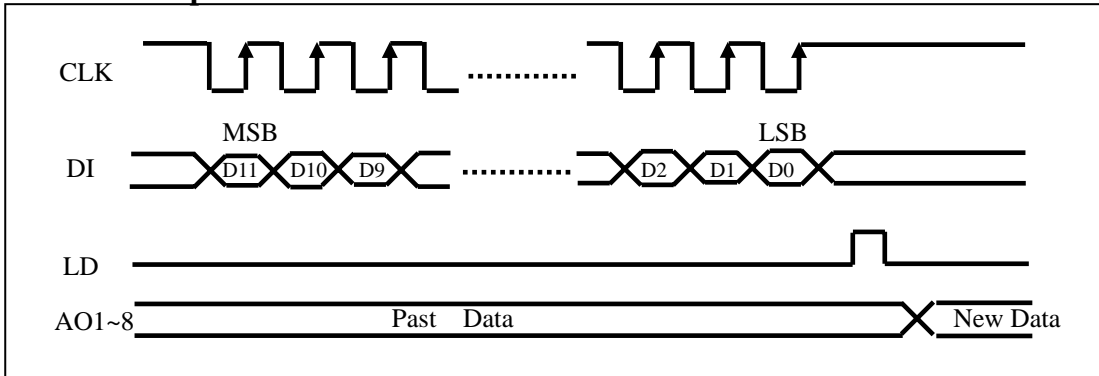
■ **Cascade Connection**



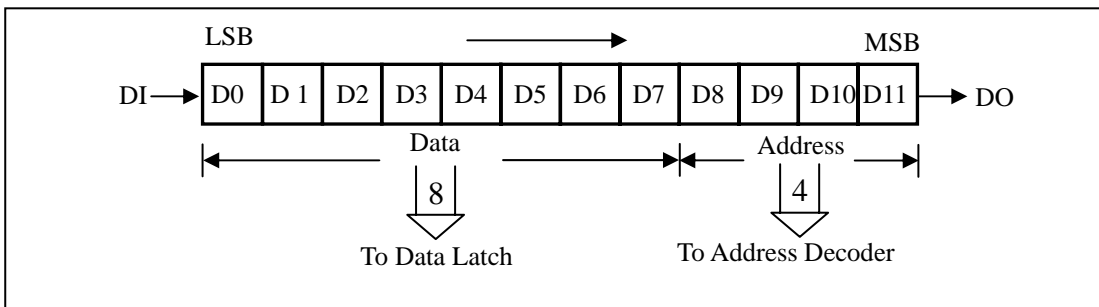
* VDD and VSS of each AA88348AP could be different depend on the application consideration



■ **Data Input Format**



■ **Data Format in Shift Register**



■ **Data Conversion**

Data								DAC Output Level
D7	D6	D5	D4	D3	D2	D1	D0	AOx
0	0	0	0	0	0	0	0	V _{SS}
0	0	0	0	0	0	0	1	V _{SS} + LSB*
0	0	0	0	0	0	1	0	V _{SS} + 2 * LSB
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	V _{DD} - LSB
1	1	1	1	1	1	1	1	V _{DD}

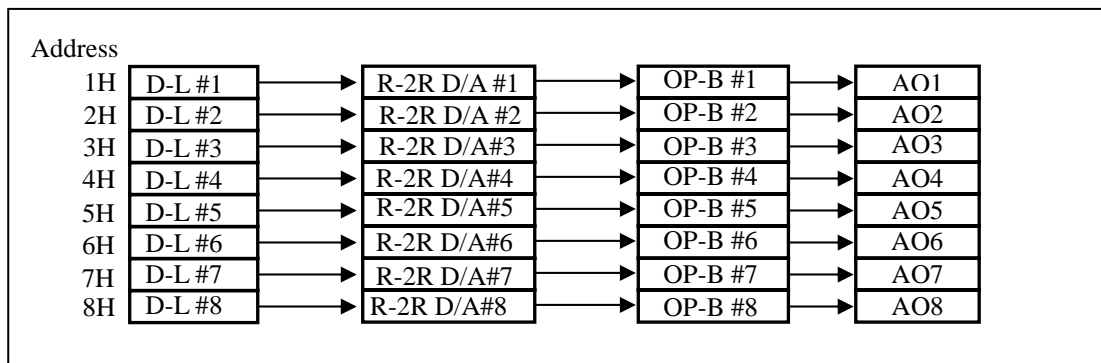
* LSB = (V_{DD}-V_{SS})/255



PRELIMINARY

8-BIT DAC

■ **Channel Map**



■ **Address Decoding**

Address				Data Latch Selected
D8	D9	D10	D11	
0	0	0	0	NA
0	0	0	1	Data Latch #1
0	0	1	0	Data Latch #2
0	0	1	1	Data Latch #3
0	1	0	0	Data Latch #4
0	1	0	1	Data Latch #5
0	1	1	0	Data Latch #6
0	1	1	1	Data Latch #7
1	0	0	0	Data Latch #8
1	0	0	1	NA
1	0	1	0	NA
1	0	1	1	NA
1	1	0	0	NA
1	1	0	1	NA
1	1	1	0	NA
1	1	1	1	Reserve



PRELIMINARY

8-BIT DAC

■ **ELECTRICAL CHARACTERISTICS**

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
System Voltage	V _{CC}	-0.3	—	+7.0	V	Ta = +25°C GND = 0V V _{DD} ≤ V _{CC} ,
Analog Voltage	V _{DD}	-0.3	—	+7.0	V	
Input Voltage	V _{IN}	-0.3	—	V _{CC} + 0.3	V	Ta = +25°C GND = 0V
Output Voltage	V _{OUT}	-0.3	—	V _{CC} + 0.3	V	
Power Dissipation	P _D	—	—	250	mW	
Operating Ambient Temperature	T _a	-20	—	+85	°C	
Storage Temperature	T _s	-55	—	+150	°C	

NOTE: Stress above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for the extended periods of time may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
System Voltage	V _{CC}	4.5	5.0	5.5	V	V _{CC} ≥ V _{DD} , V _{DD} - V _{SS} ≥ 2.0V V _{SS} ≥ GND
	GND	—	0	—	V	
Analog Voltage	V _{DD}	2.0	—	V _{CC}	V	
	V _{SS}	GND	—	V _{CC} - 2.0	V	
Analog Output Current	I _{AO}	-1.0	—	+1.0	mA	V _{AO} shift ≤ 0.3V
Analog Output Load Capacitance for Oscillation limit	COL	—	—	+1.0	μF	
Operating Ambient Temperature	T _a	-20	—	+85	°C	



PRELIMINARY

8-BIT DAC

■ **DC CHARACTERISTICS**

◆ **Digital Block**

Ta = 25°C

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
System Voltage	VCC	4.5	5.0	5.5	V	
System Current	ICC	—	1.2	2.5	mA	CLK = 1 MHz, No load;
Input Leakage Current	IILK	-5	—	+5	μA	VIN = 0V / 5V
Digital Input Low Voltage	VIL	—	—	0.2 • VCC	V	
Digital Input High Voltage	VIH	0.5 • VCC	—	—	V	
Digital Output Low	VOL	—	—	0.4	V	IOL = +2.5 mA
Digital Output High	VOH	VCC - 0.4	—	—	V	IOH = -400 μA

◆ **Analog Block**

Ta = 25°C

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Analog Current	IDD	—	0.7	1.0	mA	No load
Analog Voltage	VDD	2.0	—	VCC	V	VDD - VSS ≥ 2V
	VSS	GND	—	VCC - 2.0	V	
Analog Output Drive Range (VCC=VDD=5V, VSS=GND=0V, Data=#FF)	VAOH	VDD - 0.1	VDD	VDD + 0.1	V	IAOH = 0 μA
	VAOH	VDD - 0.2	VDD	VDD + 0.2	V	IAOH = -500 μA
	VAOH	VDD - 0.3	VDD	VDD + 0.3	V	IAOH = -1mA
Analog Output Sink Range (VCC=VDD=5V, VSS=GND=0V, Data=#00)	VAOL	VSS - 0.1	VSS	VSS + 0.1	V	IAOL = 0 μA
	VAOL	VSS - 0.2	VSS	VSS + 0.2	V	IAOL = 500 μA
	VAOL	VSS - 0.3	VSS	VSS + 0.3	V	IAOL = 1mA
Resolution (AOx)	Res	—	8	—	bit	VCC = 5.5V, GND=0V
Integral Non-Linearity	INL	-1.5	—	+2	LSB	VDD=4.775V, VSS=0.95
Differential Non-Linearity	DNL	-0.5	0	+3.5	LSB	LSB = 15mv, no load

NOTES:

Integral Non-Linearity : The difference between the digital data converted DC analog values and a reference straight line drawn through the first and the last output values

Differential Non-Linearity : The difference between the ideal and real increment value of DC analog voltage when the digital data increase 1 bit.



PRELIMINARY

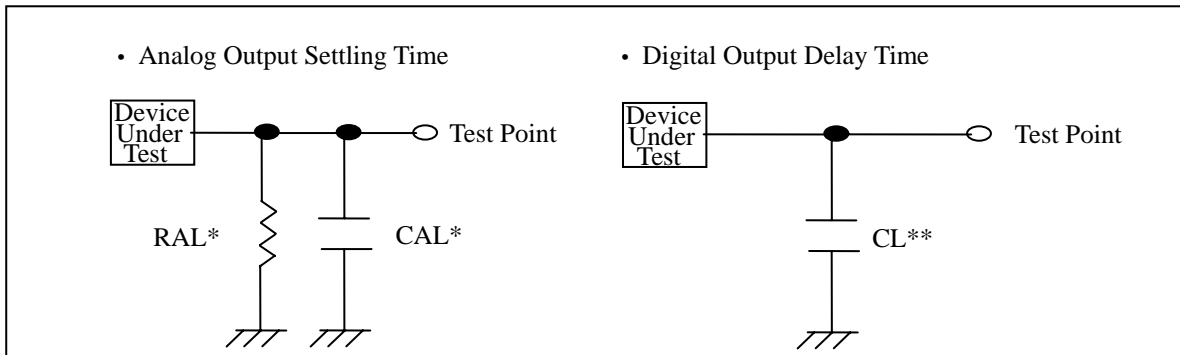
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■ **AC CHARACTERISTICS**

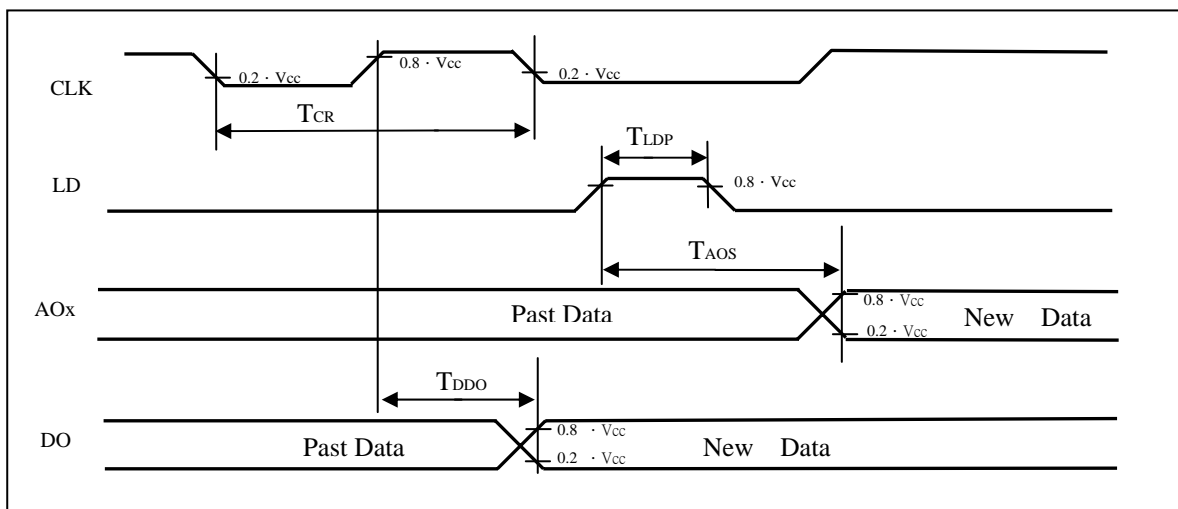
Ta = 25°C

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Clock Rate	T _{CR}	100	—	—	ns	
Load Strobe Pulse Width	T _{LDP}	50	—	—	ns	
Analog Output Settling Time	T _{AOS}	—	—	20	μs	*RAL = 10 kΩ, CAL = 50pF (#00--> #FF)
Digital Output Delay Time	T _{DDO}	—	—	200	ns	**CL = 100 pF (Max.)

◆ **AC Test Condition**



◆ **Timing Chart**

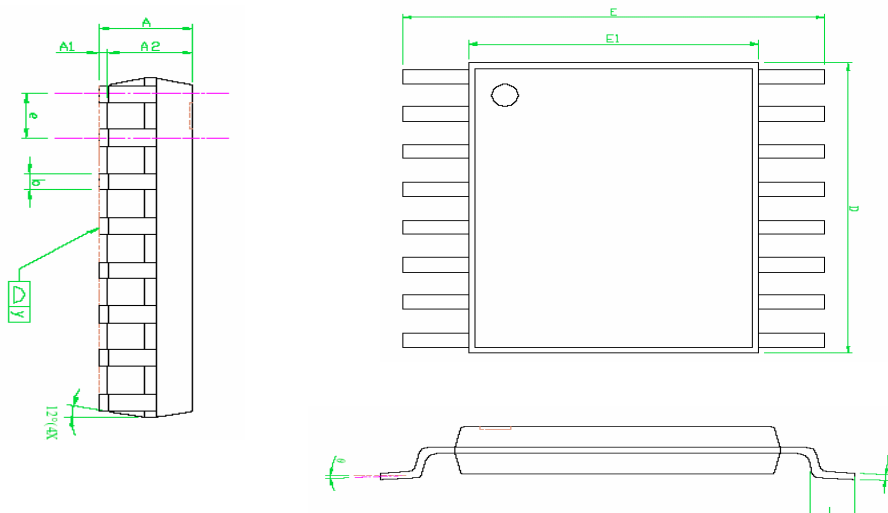




PRELIMINARY

8-BIT DAC

■ **TSSOP PACKAGE DIMENSION**



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.048
A1	0.05	---	0.15	0.002	---	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	---	0.30	0.007	---	0.012
C	0.09	---	0.20	0.004	---	0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	---	0.65	---	---	0.026	---
L	0.45	0.60	0.75	0.018	0.024	0.030
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°

NOTES:

1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance $\pm 0.1 \text{ mm}$ (4 mil) unless otherwise specified
3. Coplanarity: 0.1 mm
4. Controlling dimension is millimeter converted inch dimensions are not necessarily exact
5. Followed from jedec mo-153