# Agilent Technologies
# Measurement Modules for the 16900 Series

Data Sheet

Modularity is the key to the Agilent 16900 Series logic analysis systems' long term value. You purchase only the capability you need now, then expand as your needs evolve. All modules are tightly integrated to provide time-correlated, cross domain measurements.

Customize your system with the measurement capability that will meet your performance and price needs. Protect your investment by upgrading logic analyzer module memory depths or state speeds as your needs change.

**Measurement Capability:**

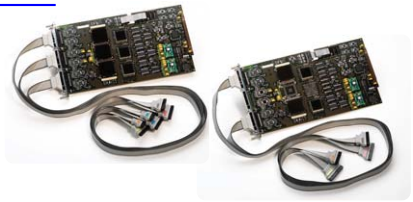
- Timing/State logic analyzers
- Pattern Generator
- Time Correlation to external scopes

**Timing/State Logic Analyzer Modules**
Agilent's timing and state modules give you the power to:

- Accurately measure precise timing relationships using 4 GHz (250 ps) timing zoom with 64 K depth.
- Extend the measurement window with precision when signals transition less frequently using transitional timing.
- Find anomalies separated in time with deep memory depths (up to 256 M across all channels).
- Buy what you need today and upgrade in the future. 16900 Series timing/state modules come with independent upgrades for memory depth and state speed.
- Sample high-speed synchronous buses accurately and confidently using eye finder. Eye finder automatically adjusts threshold and setup and hold for your highest confidence in measurements on high-speed buses.
- Track problems from symptom to root cause across several measurement modes by viewing time-correlated data in waveform/chart, listing, inverse assembly, source code, or compare display.
- Set up triggers quickly and confidently with intuitive simple, quick, and advanced triggering. This capability combines new trigger functionality with an intuitive user interface.
- The Agilent logic analyzer modules are compatible with the industry's widest range of probing accessories with capacitive loading down to 0.7 pF.
- Monitor and correlate multiple buses using a single module with split analyzer capability. This provides single and multi-bus support using a single module (timing, state, timing/state or state/state configurations).

# Logic Analyzer Selection Guide for 16900 Series Mainframes





| Agilent Model Number | 16910A/16911A | 16950B/16951B | 16760A |
|---|---|---|---|
| Channels per module | 102/68 | 68 | 34 |
| Maximum channels on single time base | 510/340 | 340 | 170 |
| **Timing Mode** | | | |
| High-speed timing zoom [1] | 4 GHz (250 ps) with 64 K depth | 4 GHz (250 ps) with 64 K depth | N/A |
| Maximum timing sample rate: half channel mode | 1.0 GHz (1 ns) | 1.2 GHz (833 ps) | 800 MHz |
| Maximum timing sample rate: full channel mode | 500 MHz (2.0 ns) | 600 MHz (1.67 ns) | 800 MHz |
| Transitional timing | 500 MHz (2.0 ns) | 600 MHz (1.67 ns) | 400 MHz |
| **State Mode** | | | |
| Maximum state clock rate | 450 MHz with option 500,<br>250 MHz with option 250 | 667 MHz | 800 Mb/s (full channel),<br>1.5 Gb/s (half channel) |
| Maximum state data rate | 500 Mb/s with option 500,<br>250 Mb/s with option 250 | 667 Mb/s (DDR)<br>1066 Mb/s (Dual Sample) | 1.5 Gb/s |
| Setup/hold window<br>Adjustment resolution | 1.5 ns<br>80 ps typical | 1 ns (600 ps typical),<br>80 ps typical | 1 ns<br>10 ps |
| State clock, data rate (upgradeable) | Yes (Agilent E5865A for 16910A)<br>(Agilent E5866A for 16911A) | No | No |
| Automated threshold/sample position, Simultaneous eye diagrams, all channels | Yes | Yes | Yes |
| **Memory Depth [2]** | | | |
| 256 M | | 16951B | |
| 64 M | | 16950B, Option 064 | 16760A |
| 32 M | Option 032 | 16950B, Option 032 | |
| 16 M | Option 016 | 16950B, Option 016 | |
| 4 M | Option 004 | 16950B, Option 004 | |
| 1 M | Option 001 | 16950B, Option 001 | |
| 256 K | Option 256 | | |
| Memory depth (upgradeable) | Yes (Agilent E5865A for 16910A)<br>(Agilent E5866A for 16911A) | Yes (Agilent E5875A) | 64 M standard |
| **Other** | | | |
| Supported signal types | Single-ended | Single-ended and differential | Single-ended and differential |
| Probe compatibility [3] | 40-pin cable connector | 90-pin cable connector | 90-pin cable connector |
| Voltage threshold | –5 V to 5 V (10 mV increments) | –3 V to 5 V (10 mV increments) | –3 V to 5 V (10 mV increments) |
| Threshold Accuracy | ±50 mV + 1% of setting | ±30 mV ±2% of setting | ±(30 mV + 1% of setting) |

[1] All channels, all the time, simultaneous state and timing through same probe.
[2] Specify desired memory depth using available options.
[3] Probes are ordered separately. Please specify probes when ordering to ensure the correct connection between your logic analyzer and the device under test.

# Data Acquisition and Stimulus

## Timing/State Modules



Agilent logic analyzer modules offer the speed, features, and usability your digital development team needs to quickly debug, validate, and optimize your digital system – at a price that fits your budget.

**Accurately measure precise timing relationships**
Make accurate high-speed timing measurements with 4 GHz (250 ps) high-speed timing zoom. A parallel acquisition architecture provides high-speed timing measurements simultaneously through the same probe with other state or timing measurements. Timing zoom stays active all the time with no tradeoffs. View data at high resolution over longer periods of time with 64 K deep timing zoom.

**Automate measurement setup and quickly gain diagnostic clues**
Quickly get up and running by automating your measurement setup process. In addition, the logic analyzer's setup/hold window (or sampling position) and threshold voltage settings are automatically determined so that data on high-speed buses is captured with the highest accuracy. Auto Threshold and Sample Position mode allows you to...

- Obtain accurate and reliable measurements
- Save time during measurement setup
- Gain diagnostic clues and identify problem signals quickly
- Scan all signals and buses simultaneously or just a few
- View results as a composite display or as individual signals
- See skew between signals and buses
- Find and fix inappropriate clock thresholds
- Measure data valid windows
- Identify signal integrity problems related to rise times, fall times, data valid window widths

**Identify problem signals over hundreds of channels simultaneously**
As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement in the design validation process. Eye scan lets you acquire signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes. Identify problem signals quickly for further investigation with an oscilloscope. Results can be viewed for each individual signal or as a composite of multiple signals or buses.

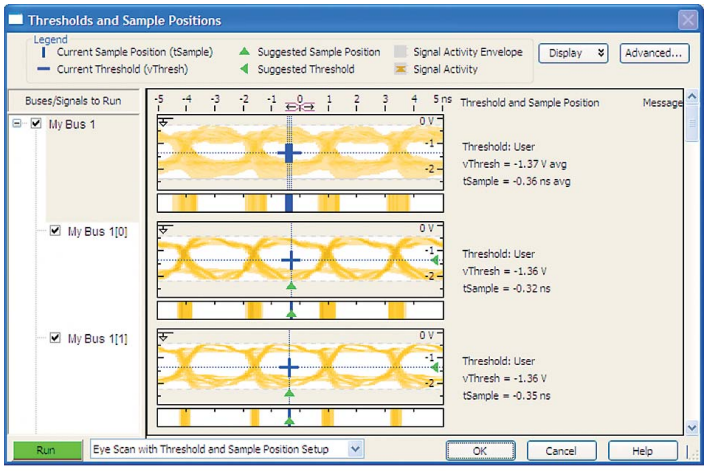



**Figure 1. Identify problem signals quickly by viewing eye diagrams across all buses and signals simultaneously.**

# Data Acquisition and Stimulus

## Pattern Generation Modules



**Digital Stimulus and Response in a Single Instrument**

Configure the logic analysis system to provide both stimulus and response in a single instrument. For example, the pattern generator can simulate a circuit initialization sequence and then signal the state or timing analyzer to begin measurements. Use the compare mode on the state analyzer to determine if the circuit or subsystem is functioning as expected. Time correlate to an external oscilloscope to help locate the source of timing problems or troubleshoot signal problems due to noise, ringing, overshoot, crosstalk, or simultaneous switching.

**Parallel Testing of Subsystems Reduces Time to Market**

By testing system subcomponents before they are complete, you can fix problems earlier in the development process. Use the Agilent 16720A as a substitute for missing boards, integrated circuits (ICs), or buses instead of waiting for the missing pieces. Software engineers can create infrequently encountered test conditions and verify that their code works—before complete hardware is available. Hardware engineers can generate the patterns necessary to put their circuit in the desired state, operate the circuit at full speed or step the circuit through a series of states.

## Key Characteristics

**Agilent Model 16720A**

| | |
|---|---|
| Maximum clock (full/half channel) | 180/300 MHz |
| Number of data channels (full/half channel) | 48/24 Channels |
| Memory depth (full/half channels) | 8/16 MVectors |
| Maximum vector width (5 module system, full/half channel) | 240/120 Bits |
| Logic levels supported | 5V TTL, 3-state TTL, 3-state TTL/CMOS, 3-state 1.8V, 3-state 2.5V, 3-state 3.3V, ECL, 5V PECL, 3.3V LVPECL, LVDS |
| Editable vector size (full/half channels) | 8/16 MVectors |

### Vectors Up To 240 Bits Wide

Vectors are defined as a “row” of labeled data values, with each data value from one to 32 bits wide. Each vector is output on the rising edge of the clock.

Up to five, 48-channel 16720A modules can be interconnected within a 16900 Series mainframe. This configuration supports vectors of any width up to 240 bits with excellent channel-to-channel skew characteristics (see specific data pod characteristics in Pattern Generation Modules Specifications starting on page 23). The modules operate as one time-base with one master clock pod. Multiple modules also can be configured to operate independently with individual clocks controlling each module.

### Depth Up to 16 MVectors

With the 16720A pattern generator, you can load and run up to 16 MVectors of stimulus. Depth on this scale is most useful when coupled with powerful stimulus generated by electronic design automation tools, such as SynaptiCAD’s WaveFormer and VeriLogger. These tools create stimulus using a combination of graphically drawn signals, timing parameters that constrain edges, clock signals, and temporal and Boolean equations for describing complex signal behavior. The stimulus also can be created from design simulation waveforms. The SynaptiCAD tools allow you to convert .VCD files into .PGB files directly, offering you an integrated solution that saves you time.

### Synchronized Clock Output

You can output data synchronized to either an internal or external clock. The external clock is input via a clock pod, and has no minimum frequency (other than a 2 ns minimum high time).

The internal clock is selectable between 1 MHz and 300 MHz in 1 MHz steps. A Clock Out signal is available from the clock pod and can be used as an edge strobe with a variable delay of up to 8 ns.

### Initialize (INIT) Block for Repetitive Runs

When running repetitively, the vectors in the initialize (init) sequence are output only once, while the main sequence is output as a continually repeating sequence. This “init” sequence is very useful when the circuit or subsystem needs to be initialized. The repetitive run capability is especially helpful when operating the stimulus module independent of the other modules in the logic analysis system.

### “Send Arm out to...” Coordinates System Module Activity

A “Send Arm out to...” instruction acts as a trigger arming event for other logic analysis modules to begin measurements. Arm setup and trigger setup of the other logic analysis modules determine the action initiated by “Send Arm out to...”.

### “Wait for External Event” for Input Pattern

The clock pod also accepts a 3-bit input pattern. These inputs are level-sensed so that any number of “Wait for External Event” instructions can be inserted into a stimulus program. Up to four pattern conditions can be defined from the OR-ing of the eight possible 3-bit input patterns. A “Wait for External Event” also can be defined to wait for an Arm. This Arm signal can come from any other module in the logic analysis system.

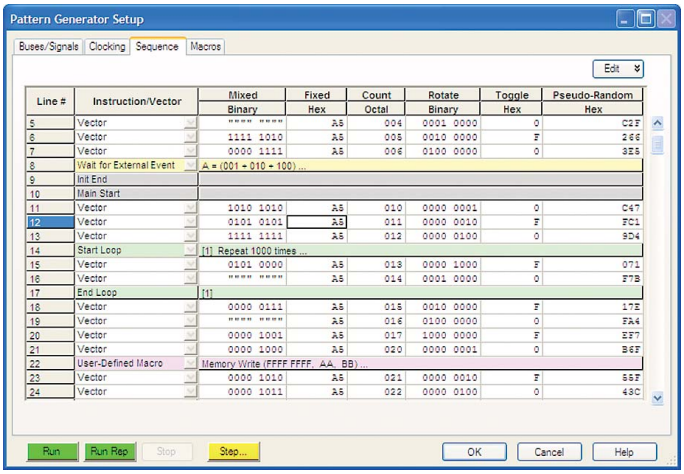



**Figure 2. Define your unique stimulus vectors, including an initialization sequence, in the Sequence tab.**

### "User-Defined Macro" and "Loop" Simplify Creation of Stimulus Programs

User macros permit you to define a pattern sequence once, then insert the macro by name wherever it is needed. Passing parameters to the macro will allow you to create a more generic macro. For each call to the macro you can specify unique values for the parameters.

Loops enable you to repeat a defined block of vectors for a specified number of times. Loops and macros can be nested, except that a macro can not be nested within another macro. At compile time, loops and macros are expanded in memory to a linear sequence.

### Convenient Data Entry and Editing Feature

You can conveniently enter patterns in hex, octal, binary, decimal, and signed decimal (two's complement) bases. The data associated with an individual label can be viewed with multiple radixes to simplify data entry. Delete, Insert, and Copy commands are provided for easy editing. Fast and convenient Pattern Fills give the programmer useful test patterns with a few key strokes. Fixed, Count, Rotate, Toggle, and Random are available to quickly create a test pattern, such as "walking ones." Pattern parameters, such as Step Size and Repeat Frequency, can be specified in the pattern setup.

### ASCII Input File Format: Your Design Tool Connection

The 16720A supports an ASCII file format to facilitate connectivity to other tools in your design environment. Because the ASCII format does not support the instructions listed earlier, they cannot be edited into the ASCII file. User macros and loops also are not supported, so the vectors need to be fully expanded in the ASCII file. Many design tools will generate ASCII files and output the vectors in this linear sequence. Data must be in Hex format, and each label must represent a set of contiguous output channels.

### Configuration

The 16720A pattern generators require a single slot in a logic analysis system frame. The pattern generator operates with the clock pods, data pods, and lead sets described later in this section. At least one clock pod and one data pod must be selected to configure a functional system. Users can select from a variety of pods to provide the signal source needed for their logic devices. The data pods, clock pods and data cables use standard connectors. The electrical characteristics of the data cables also are described for users with specialized applications who want to avoid the use of a data pod. The 16720A can be configured in systems with up to five cards for a total of 240 channels of stimulus.

### Direct Connection to Your Target System

The pattern generator pods can be directly connected to a standard connector on your target system. Use a 3M brand #2520 Series, or similar connector. The 16720A clock or data pods will plug right in. Short, flat cable jumpers can be used if the clearance around the connector is limited. Use a 3M #3365/20, or equivalent, ribbon cable; a 3M #4620 Series, or equivalent, connector on the 16720A pod end of the cable; and a 3M #3421 Series, or equivalent, connector at your target system end of the cable.

### Probing Accessories

The probe tips of the Agilent 10474A, 10347A, 10498A, and E8142A lead sets plug directly into any 0.1 inch grid with 0.026 inch to 0.033 inch diameter round pins or 0.025 inch square pins. These probe tips work with the Agilent 5090-4356 surface mount grabbers and with the Agilent 5959-0288 through-hole grabbers.

# Agilent 16910A and 16911A Specifications and Characteristics



| Module Channel Counts | State Analysis 16910A | State Analysis 16911A | Timing Analysis 16910A | Timing Analysis 16911A |
|---|---|---|---|---|
| 1-card module | 98 data + 4 clocks | 64 data + 4 clocks | 102 | 68 |
| 2-card module | 200 data + 4 clocks | 132 data + 4 clocks | 204 | 136 |
| 3-card module | 302 data + 4 clocks | 200 data + 4 clocks | 306 | 204 |
| 4-card module | 404 data + 4 clocks | 268 data + 4 clocks | 408 | 272 |
| 5-card module | 506 data + 4 clocks | 336 data + 4 clocks | 510 | 340 |

### Probes

A probe must be used to connect the logic analyzer to your target system. Probes are ordered separately from the logic analysis module. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number in this help system or at **www.agilent.com** or *Probing Solutions for Agilent Technologies Logic Analyzers* Product Overview, publication number 5968-4632E.

### Timing Zoom

| | |
|---|---|
| Timing analysis sample rate | 4 GHz |
| Time interval accuracy | |
| Within a pod pair | ± (1.0 ns + 0.01% of time interval reading) |
| Between pod pairs | ± (1.75 ns + 0.01% of time interval reading) |
| Memory depth | 64 K samples |
| Trigger position | Start, center, end, or user-defined |
| Minimum data pulse width | 1 ns |

| State (Synchronous) Analysis Mode | Option 250 | Option 500 |
|---|---|---|
| tWidth* [1] | 1.5 ns | 1.5 ns |
| tSetup | 0.5 tWidth | 0.5 tWidth |
| tHold | 0.5 tWidth | 0.5 tWidth |
| tSample range [2] | –3.2 ns to +3.2 ns | –3.2 ns to +3.2 ns |
| tSample adjustment resolution | 80 ps typical | 80 ps typical |
| Maximum state data rate on each channel | 250 Mb/s | 500 Mb/s |
| Maximum channels on a single time base and trigger [4] | 16910A: 510 – (number of clocks)<br>16911A: 340 – (number of clocks) | 16910A: 510 – (number of clocks)<br>16911A: 340 – (number of clocks) |
| Memory depth [4]<br>(Option 256 is included in base price) | Option 256: 256 K samples<br>Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples | Option 256: 256 K samples<br>Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples |
| Number of independent analyzers [5] | 2 | 1 |
| Number of clocks [6] | 4 | 1 |
| Number of clock qualifiers [6] | 4 | N/A |
| Minimum time between active clock edges* [7] | 4.0 ns | 2.0 ns |
| Minimum master to slave clock time | 1 ns | N/A |
| Minimum slave to master clock time | 1 ns | N/A |
| Minimum slave to slave clock time | 4.0 ns | N/A |

* Items marked with an asterisk (*) are specifications. All others are characteristics.
"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

[1] Minimum eye width in system under test.

[2] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.

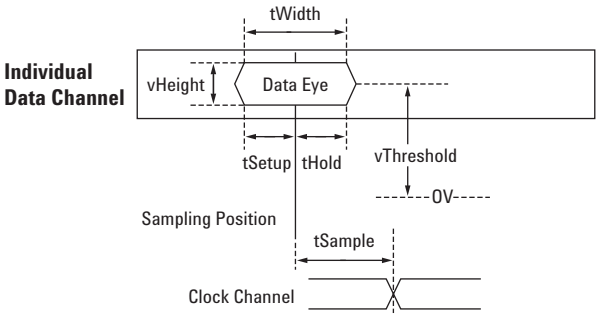
[3] Use of eye finder is recommended in 450 MHz and 500 Mb/s state mode.

[4] In 250 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full. One pod pair (34 channels) must remain unassigned for time tags in 500 Mb/s state mode.

[5] Independent analyzers may be either state or timing. When the 500 Mb/s state mode is selected, only one analyzer may be used.

[6] In the 250 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules.

[7] Tested with input signal Vh = +1.3 V, Vl = +0.7 V, threshold = +1.0 V, tr/tf = 180 ps ± 30 ps (10%, 90%).



| State (Synchronous) Analysis Mode | Option 250 | Option 500 |
|---|---|---|
| Minimum state clock pulse width | | |
| Single edge | 1.0 ns | 1.0 ns |
| Multiple edge | 1.0 ns | 2.0 ns |
| Clock qualifier setup time | 500 ps | N/A |
| Clock qualifier hold time | 0 | N/A |
| Time tag resolution | 2 ns | 1.5 ns |
| Maximum time count between stored states | 32 days | 32 days |
| Maximum trigger sequence speed | 250 MHz | 500 MHz |
| Maximum trigger sequence levels | 16 | 16 |
| Trigger sequence level branching | Arbitrary 4-way if/then/else | 2-way if/then/else |
| Trigger position | Start, center, end, or user-defined | Start, center, end, or user-defined |
| Trigger resources | 16 patterns evaluated as =, =/, >, ≥, <, ≤<br>14 double-bounded ranges evaluated as in range, not in range<br>2 timers per module<br>2 global counters<br>1 occurrence counter per sequence level<br>4 flags | 14 patterns evaluated as =, =/, >, ≥, <, ≤<br>7 double-bounded ranges evaluated as in range, not in range<br>1 occurrence counter per sequence level<br>4 flags |
| Trigger resource conditions | Arbitrary Boolean combinations | Arbitrary Boolean combinations |
| Trigger actions | Go To<br>Trigger, send e-mail, and fill memory<br>Trigger and Go To<br>Store/don't store sample<br>Turn on/off default storing<br>Timer start/stop/pause/resume<br>Global counter increment/decrement/reset<br>Occurrence counter reset<br>Flag set/clear | Go To<br>Trigger and fill memory |
| Store qualification | Default (global) and per sequence level | Default (global) |
| Maximum global counter | 2E+24 | N/A |
| Maximum occurrence counter | 2E+24 | 2E+24 |
| Maximum pattern width | 128 bits | 128 bits |
| Maximum range width | 64 bits | 64 bits |
| Timers range | 60 ns to 2199 seconds | N/A |
| Timer resolution | 2 ns | N/A |
| Timer accuracy | ± (5 ns +0.01%) | N/A |
| Timer reset latency | 60 ns | N/A |

# Agilent 16910A and 16911A Specifications and Characteristics



| Timing (Asynchronous) Analysis Mode | Conventional Timing | Transitional Timing [8] |
|---|---|---|
| Sample rate on all channels | 500 MHz | 500 MHz |
| Sample rate in half channel mode | 1000 MHz | N/A |
| Number of channels | 16910A: 102 x (number of modules)<br><br>16911A: 68 x (number of modules) | 16910A: For sample rates < 500 MHz: 102 x (number of modules)<br>For 500 MHz sample rate: 102 x (number of modules) – 34<br>16911A: For sample rates < 500 MHz: 68 x (number of modules)<br>For 500 MHz sample rate: 68 x (number of modules) – 34 |
| Maximum channels on a single time base and trigger | 16910A: 510<br>16911A: 340 | 16910A: 510<br>16911A: 340 |
| Number of independent analyzers [5] | 2 | 2 |
| Sample period (half channel) | 1.0 ns | N/A |
| Minimum sample period (full channel) | 2.0 ns | 2.0 ns |
| Minimum data pulse width | 1 sample period + 1.0 ns | 1 sample period + 1.0 ns |
| Time interval accuracy | ± (1 sample period + 1.25 ns + 0.01% of time interval reading) | ± (1 sample period + 1.25 ns + 0.01% of time interval reading) |
| Memory depth in full channel mode (Option 256 is included in base price) | Option 256: 256 K samples<br>Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples | Option 256: 256 K samples<br>Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples |
| Memory depth in half channel mode (Option 256 is included in base price) | Option 256: 512 K samples<br>Option 001: 2 M samples<br>Option 004: 8 M samples<br>Option 016: 32 M samples<br>Option 032: 64 M samples | N/A |
| Maximum trigger sequence speed | 250 MHz | 250 MHz |
| Maximum trigger sequence levels | 16 | 16 |

[5] Independent analyzers may be either state or timing. When the 500 Mb/s state mode is selected, only one analyzer may be used.
[8] Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.

| Timing (Asynchronous) Analysis Mode | Conventional Timing | Transitional Timing |
|---|---|---|
| Trigger sequence level branching | Arbitrary 4-way if/then/else | Arbitrary 4-way if/then/else |
| Trigger position | Start, center, end, or user-defined | Start, center, end, or user-defined |
| Trigger resources | 16 patterns evaluated as =, =/, >, ≥, <, ≤<br>14 double-bounded ranges evaluated as in range, not in range<br>3 edge/glitch<br>2 timers per module<br>2 global counters<br>1 occurrence counter per sequence level<br>4 flags | 15 patterns evaluated as =, =/, >, ≥, <, ≤<br>14 double-bounded ranges evaluated as in range, not in range<br>3 edge/glitch<br>2 timers per module<br>2 global counters<br>1 occurrence counter per sequence level<br>4 flags |
| Trigger resource conditions | Arbitrary Boolean combinations | Arbitrary Boolean combinations |
| Trigger actions | Go To<br>Trigger, send e-mail, and fill memory<br>Trigger and Go To<br>Turn on/off default storing<br>Timer start/stop/pause/resume<br>Global counter increment/decrement/reset<br>Occurrence counter reset<br>Flag set/clear | Go To<br>Trigger, send e-mail, and fill memory<br>Trigger and Go To<br>Turn on/off default storing<br>Timer start/stop/pause/resume<br>Global counter increment/decrement/reset<br>Occurrence counter reset<br>Flag set/clear |
| Maximum global counter | 2E+24 | 2E+24 |
| Maximum occurrence counter | 2E+24 | 2E+24 |
| Maximum range width | 32 bits | 32 bits |
| Maximum pattern width | 128 bits | 128 bits |
| Timer value range | 60 ns to 2199 seconds | 60 ns to 2199 seconds |
| Timer resolution | 2 ns | 2 ns |
| Timer accuracy | ± (5 ns +0.01%) | ± (5 ns +0.01%) |
| Greater than duration | 4.0 ns to 67 ms in 4.0 ns increments | 4.0 ns to 67 ms in 4.0 ns increments |
| Less than duration | 8.0 ns to 67 ms in 4.0 ns increments | 8.0 ns to 67 ms in 4.0 ns increments |
| Timer reset latency | 60 ns | 60 ns |

# Agilent 16950B and 16951B Specifications and Characteristics



**16950 Series module overview**
The 16950A, 16950B and 16951B are all compatible with the 16900 Series mainframes. This table shows the key differences for the 16950 series modules. All other specifications and characteristics are the same.

| | 16951B | 16950B | 16950A |
|---|---|---|---|
| State speed | 667 MHz | 667 MHz | 600 MHz |
| Max data rate | 667 Mb/s (DDR)<br>1066 Mb/s<br>(Dual sample) | 667 Mb/s (DDR)<br>1066 Mb/s<br>(Dual sample) | 600 Mb/s (DDR)<br>800 Mb/s<br>(Dual sample) |
| Memory depth | 256 M | 1 M to 64 M | 256 K to 64 M |
| Minimum eye width in system under test | 550 ps typical | 550 ps typical | 600 ps typical |
| Minimum time between active clock edges | 1.50 ns (667 Mb/s state mode) | 1.50 ns (667 Mb/s state mode) | 1.67 ns (600 Mb/s state mode) |
| Minimum state clock pulse width | 1.50 ns | 1.50 ns | 1.67 ns |

16950 Series module connections:

- You can combine up to five 16951Bs in a multiple-card set. The combined set will have 256 M memory depth across all channels.
- You can combine up to five 16950Bs in a multiple-card set. The combined set will default to the lowest memory depth in the set.
- You can combine any combination of 16753A, 16754A, 16755A, 16756A, and 16950As in a multiple-card set. The combined set will default to the lowest memory depth in the set.

| Module Channel Counts | State Analysis | Timing Analysis |
|---|---|---|
| 1-card module | 64 data + 4 clocks | 68 |
| 2-card module | 132 data + 4 clocks | 136 |
| 3-card module | 200 data + 4 clocks | 204 |
| 4-card module | 268 data + 4 clocks | 272 |
| 5-card module | 336 data + 4 clocks | 340 |

**Probes**

A probe must be used to connect the logic analyzer to your target system. For specifications and characteristics of a particular probe, see the documentation that is supplied with your probe or search for the probe's model number in this help system or at **www.agilent.com**.

**Timing Zoom**

| | |
|---|---|
| Timing analysis sample rate | 4 GHz |
| Time interval accuracy | |
| Within a pod pair | ± (1.0 ns + 0.01% of time interval reading) |
| Between pod pairs | ± (1.75 ns + 0.01% of time interval reading) |
| Memory depth | 64 K samples |
| Trigger position | Start, center, end, or user-defined |
| Minimum data pulse width | 750 ps |

# Agilent 16950B and 16951B Specifications and Characteristics



| State (Synchronous) Analysis Mode | 300 Mb/s State Mode | 667 Mb/s State Mode |
|---|---|---|
| tWidth* [1, 2] | 850 ps*, 550 ps typical | 850 ps*, 550 ps typical |
| tSetup | 0.5 tWidth | 0.5 tWidth |
| tHold | 0.5 tWidth | 0.5 tWidth |
| tSample range [3] | –4 ns to +4 ns | –4 ns to +4 ns |
| tSample adjustment resolution | 80 ps typical | 80 ps typical |
| tSample accuracy, manual adjustment | ± 300 ps | ± 300 ps [4] |
| Maximum state data rate | 300 Mb/s (DDR)<br>600 Mb/s (Dual sample) | 667 Mb/s (DDR)<br>1066 Mb/s (Dual sample) |
| Maximum channels on a single time base and trigger [5] | 340 – (number of clocks) | 306 – (1 clock) |
| Memory depth – 16950B [5] | Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples<br>Option 064: 64 M samples | Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples<br>Option 064: 64 M samples |
| Memory depth – 16951B [5] | 256 M samples | 256 M samples |
| Number of independent analyzers [6] | 2 | 1 |
| Number of clocks [7] | 4 | 1 |
| Number of clock qualifiers [7] | 4 | N/A |
| Minimum time between active clock edges* [8] | 3.33 ns | 1.50 ns |
| Minimum master to slave clock time | 1 ns | N/A |
| Minimum slave to master clock time | 1 ns | N/A |
| Minimum slave to slave clock time | 3.33 ns | N/A |

* Items marked with an asterisk (*) are specifications. All others are characteristics.

[1] Minimum eye width in system under test.

[2] Your choice of probe can limit system bandwidth. Choose a probe rated at 1066 Mb/s or greater to maintain system bandwidth.

[3] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.

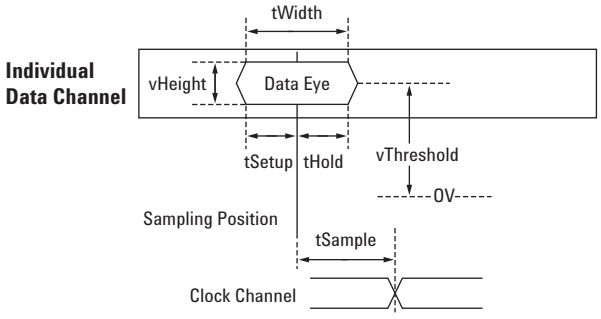
[4] Use of eye finder is recommended in 667 Mb/s state mode.

[5] In 300 Mb/s state mode, with all pods assigned, memory depth is half the maximum memory depth. With one pod pair (34 channels) unassigned, the memory depth is full. One pod pair (34 channels) must remain unassigned for time tags in 667 Mb/s state mode.

[6] Independent analyzers may be either state or timing. When the 667 Mb/s state mode is selected, only one analyzer may be used.

[7] In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master modules.

[8] Tested with input signal Vh = +1.125 V, Vl = +0.875 V = 1 V/ns, threshold = +1.0 V, tr/tf = 180 ps ± 30 ps (10%, 90%).



# Agilent 16950B and 16951B Specifications and Characteristics



| State (Synchronous) Analysis Mode | 300 Mb/s State Mode | 667 Mb/s State Mode |
|---|---|---|
| Minimum state clock pulse width | | |
| Single edge | 1.0 ns | 500 ps |
| Multiple edge | 1.0 ns | 1.50 ns |
| Clock qualifier setup time | 500 ps | N/A |
| Clock qualifier hold time | 0 | N/A |
| Time tag resolution | 2 ns | 1.5 ns |
| Maximum time count between stored states | 32 days | 32 days |
| Maximum trigger sequence speed | 300 MHz | 667 MHz |
| Maximum trigger sequence levels | 16 | 16 |
| Trigger sequence level branching | Arbitrary 4-way if/then/else | 2-way if/then/else |
| Trigger position | Start, center, end, or user-defined | Start, center, end, or user-defined |
| Trigger resources | 16 patterns evaluated as =, =/, >, ≥, <, ≤<br>14 double-bounded ranges evaluated as in range, not in range<br>2 timers per module<br>2 global counters<br>1 occurrence counter per sequence level<br>4 flags | 14 patterns evaluated as =, =/, >, ≥, <, ≤<br>7 double-bounded ranges evaluated as in range, not in range<br>1 occurrence counter per sequence level<br>4 flags |
| Trigger resource conditions | Arbitrary Boolean combinations | Arbitrary Boolean combinations |
| Trigger actions | Go To<br>Trigger, send e-mail, and fill memory<br>Trigger and Go To<br>Store/don't store sample<br>Turn on/off default storing<br>Timer start/stop/pause/resume<br>Global counter increment/decrement/reset<br>Occurrence counter reset<br>Flag set/clear | Go To<br>Trigger and fill memory |
| Store qualification | Default (global) and per sequence level | Default (global) |
| Maximum global counter | 2E+24 | N/A |
| Maximum occurrence counter | 2E+24 | 2E+24 |
| Maximum pattern width | 128 bits | 128 bits |
| Maximum range width | 64 bits | 64 bits |
| Timers range | 50 ns to 2199 seconds | N/A |
| Timer resolution | 2 ns | N/A |
| Timer accuracy | ± (5 ns +0.01%) | N/A |
| Timer reset latency | 50 ns | N/A |

# Agilent 16950B and 16951B Specifications and Characteristics



| Timing (Asynchronous) Analysis Mode | Conventional Timing | Transitional Timing [9] |
|---|---|---|
| Sample rate on all channels | 600 MHz | 600 MHz |
| Sample rate in half channel mode | 1200 MHz | N/A |
| Number of channels | 68 x (number of modules) | For sample rates < 600 MHz: 68 x (number of modules).<br>For 600 MHz sample rate: 68 x (number of modules) – 34 |
| Maximum channels on a single time base and trigger | 340 | 340 |
| Number of independent analyzers [6] | 2 | 2 |
| Sample period (half channel) | 833 ps | N/A |
| Minimum sample period (full channel) | 1.67 ns | 1.67 ns |
| Minimum data pulse width | 1 sample period + 500 ps | 1 sample period + 500 ps |
| Time interval accuracy | ± (1 sample period + 1.25 ns + 0.01% of time interval reading) | ± (1 sample period + 1.25 ns + 0.01% of time interval reading) |
| Memory depth in full channel mode – 16950B | Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples<br>Option 064: 64 M samples | Option 001: 1 M samples<br>Option 004: 4 M samples<br>Option 016: 16 M samples<br>Option 032: 32 M samples<br>Option 064: 64 M samples |
| Memory depth in full channel mode – 16951B | 256 M samples | 256 M samples |
| Memory depth in half channel mode – 16950B | Option 001: 2 M samples<br>Option 004: 8 M samples<br>Option 016: 32 M samples<br>Option 032: 64 M samples<br>Option 064: 128 M samples | N/A |
| Memory depth in half channel mode – 16951B | 512 M samples | N/A |
| Maximum trigger sequence speed | 300 MHz | 300 MHz |
| Maximum trigger sequence levels | 16 | 16 |

[6] Independent analyzers may be either state or timing. When the 600 Mb/s state mode is selected, only one analyzer may be used.
[9] Transitional timing speed and memory depth are halved unless a spare pod pair (34 channels) is unassigned.

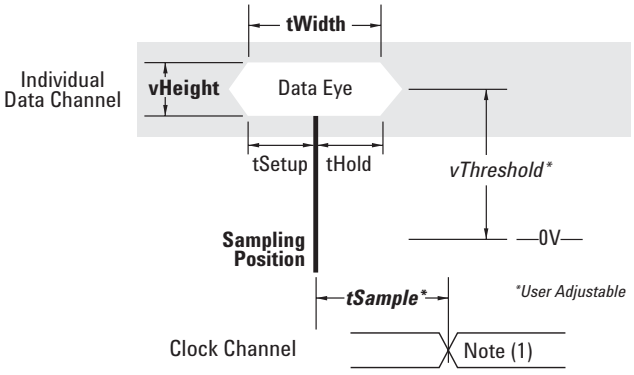
| Timing (Asynchronous) Analysis Mode | Conventional Timing | Transitional Timing |
|---|---|---|
| Trigger sequence level branching | Arbitrary 4-way if/then/else | Arbitrary 4-way if/then/else |
| Trigger position | Start, center, end, or user-defined | Start, center, end, or user-defined |
| Trigger resources | 16 patterns evaluated as =, =/, >, ≥, <, ≤<br>14 double-bounded ranges evaluated as in range, not in range<br>3 edge/glitch<br>2 timers per module<br>2 global counters<br>1 occurrence counter per sequence level<br>4 flags | 15 patterns evaluated as =, =/, >, ≥, <, ≤<br>14 double-bounded ranges evaluated as in range, not in range<br>3 edge/glitch<br>2 timers per module<br>2 global counters<br>1 occurrence counter per sequence level<br>4 flags |
| Trigger resource conditions | Arbitrary Boolean combinations | Arbitrary Boolean combinations |
| Trigger actions | Go To<br>Trigger, send e-mail, and fill memory<br>Trigger and Go To<br>Turn on/off default storing<br>Timer start/stop/pause/resume<br>Global counter increment/decrement/reset<br>Occurrence counter reset<br>Flag set/clear | Go To<br>Trigger, send e-mail, and fill memory<br>Trigger and Go To<br>Turn on/off default storing<br>Timer start/stop/pause/resume<br>Global counter increment/decrement/reset<br>Occurrence counter reset<br>Flag set/clear |
| Maximum global counter | 2E+24 | 2E+24 |
| Maximum occurrence counter | 2E+24 | 2E+24 |
| Maximum pattern/range width | 32 bits | 32 bits |
| Maximum pattern width | 128 bits | 128 bits |
| Timer value range | 50 ns to 2199 seconds | 50 ns to 2199 seconds |
| Timer resolution | 2 ns | 2 ns |
| Timer accuracy | ± (5 ns +0.01%) | ± (5 ns +0.01%) |
| Greater than duration | 3.33 ns to 55 ms in 3.3 ns increments | 3.33 ns to 55 ms in 3.3 ns increments |
| Less than duration | 6.67 ns to 55 ms in 3.3 ns increments | 6.67 ns to 55 ms in 3.3 ns increments |
| Timer reset latency | 50 ns | 50 ns |

# Agilent 16760A Specifications and Characteristics



## Agilent Technologies 16760A Supplemental Specifications* and Characteristics

### Synchronous Data Sampling




### Specifications for Each Input

| | Parameter | Minimum | | Description/Notes |
|---|---|---|---|---|
| | | 800, 1250, 1500 Mb/s modes | 200, 400 Mb/s modes | |
| Data to Clock | tWidth | 500 ps | 1.25 ns | Eye width in system under test [2] |
| | tSetup | 250 ps | 625 ps | Data setup time required before *tSample* |
| | tHold | 250 ps | 625 ps | Data hold time required after *tSample* |
| All Inputs | vHeight [1] | 100mV | 100mV | E5379A 100-pin differential probe [3]<br>E5381A differential flying-lead probe [3]<br>E5387A differential soft touch [3]<br>E5405A differential pro series soft touch [3] |
| | | 250 mV | 250 mV | E5378A 100-pin single-ended probe [4],<br>E5382A single-ended flying-lead probe set<br>E5406A pro series soft touch [4]<br>E5390A soft touch [4]<br>E5398A half-size soft touch [4] |
| | | 300mV | 300mV | E5380A 38-pin single-ended probe |

* All specifications noted by an asterisk in the table are the performance standards against which the product is tested.

[1] The analyzer can be configured to sample on the rising edge, the falling edge, or both edges of the clock. If both edges are used with a single ended clock input, take care to set the clock threshold accurately to avoid phase error.

[2] Eye width and height are specified at the probe tip. Eye width as measured by eye finder in the analyzer may be less, and still sample reliably.

[3] For each side of a differential signal.

[4] The clock inputs in the E5378A, E5398A, E5406A, E5390A, and E5382A may be connected differentially or single ended. Use the E5379A vHeight spec for clock channel(s) connected differentially.

[5] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes synchronous sampling coincident with each active clock edge.

[6] Threshold applies to single-ended input signals. Thresholds are independently adjustable for the clock input of each pod and for each set of 16 data inputs for each pod. Threshold limits apply to both the internal reference and to the external reference input on the E5378A.

## Agilent Technologies 16760A Supplemental Specifications* and Characteristics (continued)

### Synchronous Data Sampling

#### User Adjustable Settings for Each Input

| | Parameter | Adjustment Range | | | | |
|---|---|---|---|---|---|---|
| | | 1500 Mb/s mode | 1250 Mb/s mode | 800 Mb/s mode | 400 Mb/s mode | 200 Mb/s mode |
| Data to Clock | Adjustment Resolution<br>tSample [5] | 10 ps<br>0 to +4 ns | 10 ps<br>–2.5 to +2.5 ns | 10 ps<br>–2.5 to +2.5 ns | 100 ps<br>–3.2 to +3.2 ns | 100 ps<br>–3.5 to +3 ns |
| All Inputs | vThreshold [6] | 10 mV resolution<br>–3 to +5 V | 10 mV resolution<br>–3 to +5 V | 10 mV resolution<br>–3 to +5 V | 10 mV resolution<br>–3 to +5 V | 10 mV resolution<br>–3 to +5 V |

* All specifications noted by an asterisk in the table are the performance standards against which the product is tested.

[1] The analyzer can be configured to sample on the rising edge, the falling edge, or both edges of the clock. If both edges are used with a single ended clock input, take care to set the clock threshold accurately to avoid phase error.

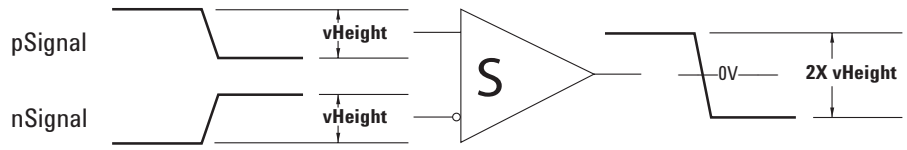
[2] Eye width and height are specified at the probe tip. Eye width as measured by eye finder in the analyzer may be less, and still sample reliably.

[3] For each side of a differential signal.

[4] The clock inputs in the E5378A, E5398A, E5406A, E5390A, and E5382A may be connected differentially or single ended. Use the E5379A vHeight spec for clock channel(s) connected differentially.

[5] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes synchronous sampling coincident with each active clock edge.

[6] Threshold applies to single-ended input signals. Thresholds are independently adjustable for the clock input of each pod and for each set of 16 data inputs for each pod. Threshold limits apply to both the internal reference and to the external reference input on the E5378A.



# Agilent 16760A Specifications and Characteristics



## Agilent Technologies 16760A Supplemental Specifications* and Characteristics (continued)

| Synchronous State Analysis | 1.5 Gb/s mode | 1.25 Gb/s mode | 800 Mb/s mode | 400 Mb/s mode | 200 Mb/s mode |
|---|---|---|---|---|---|
| Maximum data rate on each channel [3] | 1.5 Gb/s | 1.25 Gb/s | 800 Mb/s | 400 Mb/s | 200 Mb/s |
| Minimum clock interval, active edge to active edge* [3] | 667 ps | 800 ps | 1.25 ns | 2.5 ns | 5 ns |
| Minimum state clock pulse width with clock polarity rising or falling [3] | N/A | N/A | 600 ps | 1.5 ns | 1.5 ns |
| Clock periodicity | Clock must be periodic | Clock must be periodic | Periodic or aperiodic | Periodic or aperiodic | Periodic or aperiodic |
| Number of clocks | 1 | 1 | 1 | 1 | 1 |
| Clock polarity | Both edges | Both edges | Rising, falling, or both | Rising, falling, or both | Rising, falling, or both |
| Minimum data pulse width* | 600 ps | 750 ps | E5378A, E5379A, E5382A probes: 750 ps<br>E5380A probe: 1.5 ns | 1.5 ns | 1.5 ns |
| Number of channels [1] | | | | | |
| • With time tags | 16 x (number of modules) – 8 | 16 x (number of modules) – 8 | 34 x (number of modules) – 16 | 34 x (number of modules) – 16 | 34 x (number of modules) |
| • Without time tags | 16 x (number of modules) | 16 x (number of modules) | 34 x (number of modules) – 1 | 34 x (number of modules) | 34 x (number of modules) |
| Maximum channels on a single time base and trigger | 80 (5 modules) | 80 (5 modules) | 170 (5 modules) | 153 (5 modules) | 170 (5 modules) |
| Maximum memory depth | 128M samples | 128M samples | 64M samples | 32M samples | 32M samples |
| Time tag resolution | 4 ns [2] | 4 ns [2] | 4 ns [2] | 4 ns [2] | 4 ns |
| Maximum time count between states | 17 seconds | 17 seconds | 17 seconds | 17 seconds | 17 seconds |

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] In 1.25 Gb/s and 1.5 Gb/s modes, only the even-numbered channels (0, 2, 4, etc.) are acquired.
[2] The resolution of the hardware used to assign time tags is 4 ns. Times of intermediate states are calculated.
[3] The choice of probe can limit system performance. Select a probe rated at the speed of the selected mode (or greater) to maintain system bandwidth.

# Agilent 16760A Specifications and Characteristics



## Agilent Technologies 16760A Supplemental Specifications* and Characteristics (continued)

| **Synchronous State Analysis** (continued) | **1.5 Gb/s mode** | **1.25 Gb/s mode** | **800 Mb/s mode** | **400 Mb/s mode** | **200 Mb/s mode** |
|---|---|---|---|---|---|
| Trigger resources | 3 Patterns on each pod evaluated as =, ≠, >, <, ≥, ≤ on one pod; or evaluated as =, ≠ across multiple pods; or 1 range on each pod<br>4 Flags<br>Arm in | 3 Patterns on each pod evaluated as =, ≠, >, <, ≥, ≤ on one pod; or evaluated as =, ≠ across multiple pods; or 1 range on each pod<br>4 Flags<br>Arm in | 4 Patterns on each pod evaluated as =, ≠, >, <, ≥, ≤ on one pod; or evaluated as =, ≠ across multiple pods; or 2 ranges on each pod<br>4 Flags<br>Arm in | 8 Patterns evaluated as =, ≠, >, <, ≥, ≤<br>4 Ranges evaluated as in range, not in range<br>2 Occurrence counters<br>4 Flags<br>Arm in | 16 Patterns evaluated as =, ≠, >, <, ≥, ≤<br>15 Ranges evaluated as in range, not in range<br>Timers: 2 x (number of modules) – 1<br>2 Global counters<br>1 Occurrence counter per sequence level<br>4 Flags<br>Arm in |
| Trigger actions | Trigger and fill memory | Trigger and fill memory | Trigger and fill memory | Goto<br>Trigger and fill memory | Goto<br>Trigger and fill memory<br>Trigger and goto<br>Store/don't store sample<br>Turn default storing on/off<br>Timer start/stop/ pause/resume<br>Global counter increment/reset<br>Occurrence counter reset<br>Flag set/clear |

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] In 1.25 Gb/s and 1.5 Gb/s modes, only the even-numbered channels (0, 2, 4, etc.) are acquired.
[2] The resolution of the hardware used to assign time tags is 4 ns. Times of intermediate states are calculated.
[3] The choice of probe can limit system performance. Select a probe rated at the speed of the selected mode (or greater) to maintain system bandwidth.

# Agilent 16760A Specifications and Characteristics



## Agilent Technologies 16760A Supplemental Specifications* and Characteristics (continued)

| **Synchronous State Analysis [4]** (continued) | **1.5 Gb/s mode** | **1.25 Gb/s mode** | **800 Mb/s mode** | **400 Mb/s mode** | **200 Mb/s mode** |
|---|---|---|---|---|---|
| Maximum trigger sequence levels | 2 | 2 | 4 | 16 | 16 |
| Maximum trigger sequencer speed | 1.5 Gb/s | 1.25 Gb/s | 800 MHz | 400 MHz | 200 MHz |
| Store qualification | Default | Default | Default | Default | Default and per sequence level |
| Maximum global counter | N/A | N/A | N/A | N/A | 16,777,215 |
| Maximum occurrence counter | N/A | N/A | N/A | N/A | 16,777,215 |
| Maximum pattern/ range term width | 32 bits [3] | 32 bits [3] | 32 bits [3] | 32 bits [3] | 32 bits [3] |
| Timer value range | N/A | N/A | N/A | N/A | 100 ns to 4397 seconds |
| Timer resolution | N/A | N/A | N/A | N/A | 4 ns |
| Timer accuracy | N/A | N/A | N/A | N/A | ±(10 ns + 0.01% of value) |
| Timer reset latency | N/A | N/A | N/A | N/A | 65 ns |
| Data in to BNC port out latency | 150 ns | 150 ns | 150 ns | 150 ns | 150 ns |
| Flag set/reset to evaluation latency | N/A | N/A | N/A | N/A | 110 ns |

[1] In 1.25 Gb/s and 1.5 Gb/s modes, only the even-numbered channels (0, 2, 4, etc.) are acquired.
[2] The resolution of the hardware used to assign time tags is 4 ns. Times of intermediate states are calculated.
[3] Maximum label width is 32 bits. Wider patterns can be created by "Anding" multiple labels together.
[4] The choice of probe can limit system performance. Select a probe rated at the speed of the selected mode (or greater) to maintain system bandwidth.

| **Asynchronous Timing Analysis** | **Conventional Timing Analysis** | **Transitional Timing Analysis** |
|---|---|---|
| Maximum timing analysis sample rate | 800 MHz | 400 MHz |
| Number of channels | 34 x (number of modules) | Sampling rates < 400 MHz: 34 x (number of modules)<br>Sampling rates = 400 MHz:<br>34 x (number of modules) – 17 [1] |
| Maximum channels on a single time base and trigger | 170 (5 modules) | 170 (5 modules) |
| Sample period | 1.25 ns | 2.5 ns to 1 ms [1] |
| Memory Depth | 64 M Samples | 32 M Samples [1] |

[1] With all pods assigned in transitional/store qualified timing, minimum sample period is 5 ns and maximum memory depth is 16 M samples.

# Agilent 16760A Specifications and Characteristics



## Agilent Technologies 16760A Supplemental Specifications* and Characteristics (continued)

| **Asynchronous Timing Analysis** (continued) | **Conventional Timing Analysis** | **Transitional Timing Analysis** |
|---|---|---|
| Sample period accuracy | ±(250 ps + 0.01% of sample period) | ±(250 ps + 0.01% of sample period) |
| Channel-to-channel skew | < 1.5 ns | < 1.5 ns |
| Time interval accuracy | ±[sample period + (channel-to-channel skew) + (0.01% of time interval)] | ±[sample period + (channel-to-channel skew) + (0.01% of time interval)] |
| Minimum data pulse width | 1.5 ns for data capture<br>5.1 ns for trigger sequencing | 3.8 ns for data capture<br>5.1 ns for trigger sequencing |
| Maximum trigger sequencer speed | 200 MHz | 200 MHz |
| Trigger resources | 16 Patterns evaluated as =, ≠, >, <, ≥, ≤<br>15 Ranges evaluated as in range, not in range<br>2 Edge/glitch<br>(2 Timers per module) – 1<br>2 Global counters<br>1 Occurrence counter per sequence level<br>4 Flags, Arm In | 16 Patterns evaluated as =, ≠, >, <, ≥, ≤<br>15 Ranges evaluated as in range, not in range<br>2 Edge/glitch<br>(2 Timers per module) – 1<br>2 Global counters<br>1 Occurrence counter per sequence level<br>4 Flags, Arm In |
| Trigger resource conditions | Arbitrary Boolean combinations | Arbitrary Boolean combinations |
| Trigger actions | Goto<br>Trigger and fill memory<br>Trigger and goto<br>Timer start/stop/pause/resume<br>Global counter increment/reset<br>Occurrence counter reset | Goto<br>Trigger and fill memory<br>Trigger and goto<br>Timer/start/stop/pause/resume<br>Global counter increment/reset<br>Occurrence counter reset |
| Maximum global counter | 16,777,215 | 16,777,215 |
| Maximum occurrence counter | 16,777,215 | 16,777,215 |
| Timer value range | 100 ns to 4397 seconds | 100 ns to 4397 seconds |
| Timer resolution | 4 ns | 4 ns |
| Timer accuracy | ±(10 ns + 0.01%) | ±(10 ns + 0.01%) |
| Greater than duration | 5 ns to 83 ms in 5 ns increments | 5 ns to 83 ms in 5 ns increments |
| Less than duration | 10 ns to 83 ms in 5 ns increments | 10 ns to 83 ms in 5 ns increments |
| Timer reset latency | 60 ns | 60 ns |
| Data in to BNC port out delay latency | 150 ns | 150 ns |
| Flag set/reset to evaluation latency | 110 ns | 110 ns |

| **Environmental** | |
|---|---|
| Operating temperature | 0 deg C to 45 deg C |

# Agilent 16720A Pattern Generator Specifications and Characteristics



**16720A Pattern Generator Characteristics**

| | |
|---|---|
| Maximum memory depth | 16 MVectors |
| Number of output channels at > 180 MHz and ≤ 300 MHz clock | 24 |
| Number of output channels at ≤ 180 MHz clock | 48 |
| Number of different macros<br>Maximum number of lines in a macro<br>Maximum number of parameters in a macro<br>Maximum number of macro invocations<br>Maximum loop count in a repeat loop | limited only by the pattern generator's available memory depth |
| Maximum number of repeat loop invocations | 1000 |
| Maximum number of "Wait" event patterns | 4 |
| Number of input lines to define a pattern | 3 |
| Maximum number of modules in a system | 5 |
| Maximum width of a vector (in a 5 module system) | 240 bits |
| Maximum width of a label | 128 bits |
| Maximum number of labels | limited only by system memory |
| Maximum number of vectors in all formats | 16 MVectors |
| Minimum number of vectors in binary format when loading into hardware | 4096 |

**Lead Set Characteristics**

| | |
|---|---|
| Agilent 10474A 8-channel probe lead set* | Provides most cost effective lead set for the 16720A clock and data pods. Grabbers are not included. Lead wire length is 12 inches. |
| Agilent 10347A 8-channel probe lead set | Provides 50 Ω coaxial lead set for unterminated signals, required for 10465A ECL Data Pod (unterminated). Grabbers are not included. |
| Agilent 10498A 8-channel probe lead set* | Provides most cost effective lead set for the 16720A clock and data pods. Grabbers are not included. Lead wire length is 6 inches. |
| Agilent E8142A 8-channel probe lead set | Provides lead set for the 16720A LVDS clock and data pods. Grabbers are not included. Lead wire length is 6 inches. |

* For all clock and data pods except 10465A unterminated ECL Data Pod and E8140A/E8141A clock and data pods.

# Agilent 16720A Pattern Generator Specifications and Characteristics

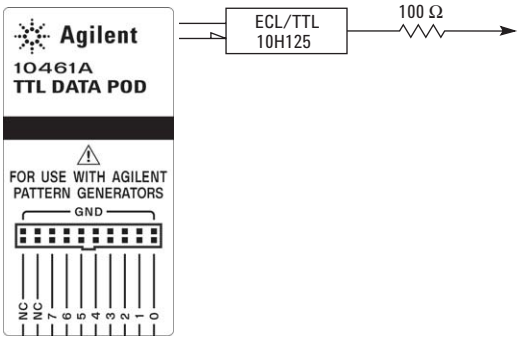


## Data Pod Characteristics

Note: Data Pod output parametrics depend on the output driver and the impedance load of the target system. Check the device data book for the specific drivers listed for each pod.

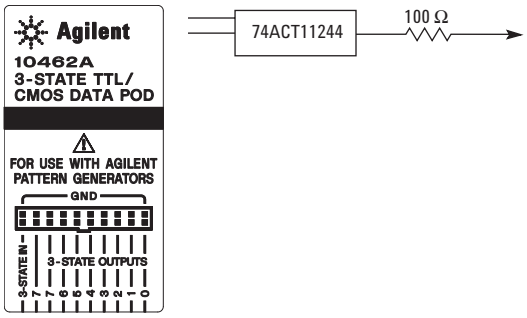
### Agilent 10461A TTL Data Pod

| | |
|---|---|
| Output type | 10H125 with 100 Ω series |
| Maximum clock | 200 MHz |
| Skew [1] | typical < 2 ns; worst case = 4 ns |
| Recommended lead set | Agilent 10474A |



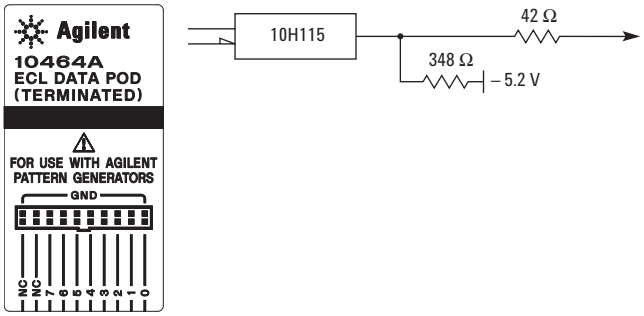

### Agilent 10462A 3-State TTL/CMOS Data Pod

| | |
|---|---|
| Output type | 74ACT11244 with 100 Ω series; 10H125 on non 3-state channel 7 [2] |
| 3-state enable | negative true, 100 KΩ to GND, enabled on no connect |
| Maximum clock | 100 MHz |
| Skew [1] | typical < 4 ns; worst case = 12 ns |
| Recommended lead set | Agilent 10474A |




### Agilent 10464A ECL Data Pod (terminated)

| | |
|---|---|
| Output type | 10H115 with 330 Ω pulldown, 47 Ω series |
| Maximum clock | 300 MHz |
| Skew [1] | typical < 1 ns; worst case = 2 ns |
| Recommended lead set | Agilent 10474A |




[1] Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits. Both numbers apply to any channel within a single or multiple module system.

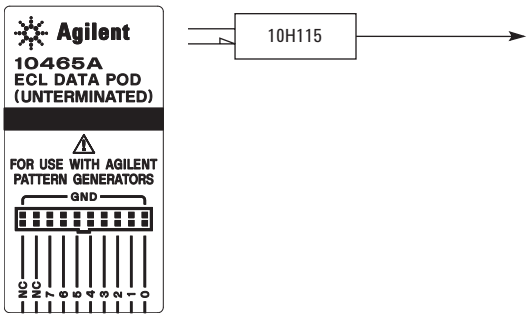
[2] Channel 7 on the 3-state pods has been brought out in parallel as a non 3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

# Agilent 16720A Pattern Generator Specifications and Characteristics



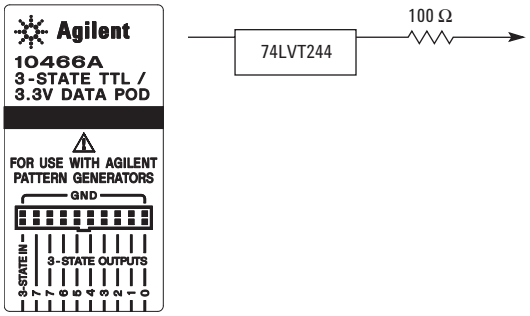
### Agilent 10465A ECL Data Pod (unterminated)

| | |
|---|---|
| Output type | 10H115 (no termination) |
| Maximum clock | 300 MHz |
| Skew [1] | typical < 1 ns; worst case = 2 ns |
| Recommended lead set | Agilent 10347A |




### Agilent 10466A 3-State TTL/3.3 volt Data Pod

| | |
|---|---|
| Output type | 74LVT244 with 100 Ω series;<br>10H125 on non 3-state channel 7 [2] |
| 3-state enable | negative true, 100 KΩ to GND, enabled on no connect |
| Maximum clock | 200 MHz |
| Skew [1] | typical < 3 ns; worst case = 7 ns |
| Recommended lead set | Agilent 10474A |




[1] Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits. Both numbers apply to any channel within a single or multiple module system.

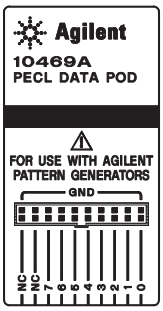
[2] Channel 7 on the 3-state pods has been brought out in parallel as a non 3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

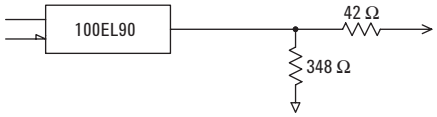
# Agilent 16720A Pattern Generator Specifications and Characteristics



### Agilent 10469A 5 volt PECL Data Pod

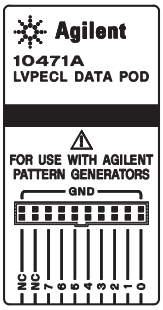
| | |
|---|---|
| Output type | 100EL90 (5V) with 348 ohm pulldown to ground and 42 ohm in series |
| Maximum clock | 300 MHz |
| Skew [1] | typical < 500 ps; worst case = 1 ns |
| Recommended lead set | Agilent 10498A |

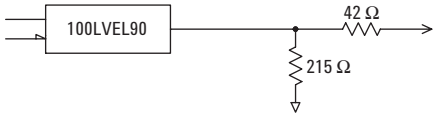



### Agilent 10471A 3.3 volt LVPECL Data Pod

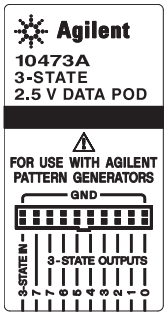
| | |
|---|---|
| Output type | 100LVEL90 (3.3V) with 215 ohm pulldown to ground and 42 ohm in series |
| Maximum clock | 300 MHz |
| Skew [1] | typical < 500 ps; worst case = 1 ns |
| Recommended lead set | Agilent 10498A |

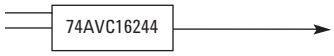



### Agilent 10473A 3-State 2.5 Volt Data Pod

| | |
|---|---|
| Output type | 74AVC16244 |
| 3-state enable | negative true, 38 KΩ to GND, enabled on no connect |
| Maximum clock | 300 MHz |
| Skew [1] | typical < 1.5 ns; worst case = 2 ns |
| Recommended lead set | Agilent 10498A |




[1] Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits. Both numbers apply to any channel within a single or multiple module system.

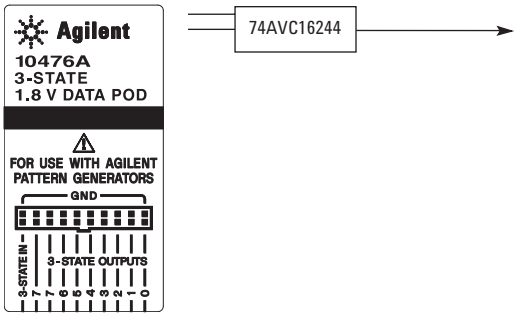
[2] Channel 7 on the 3-state pods has been brought out in parallel as a non 3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

# Agilent 16720A Pattern Generator Specifications and Characteristics



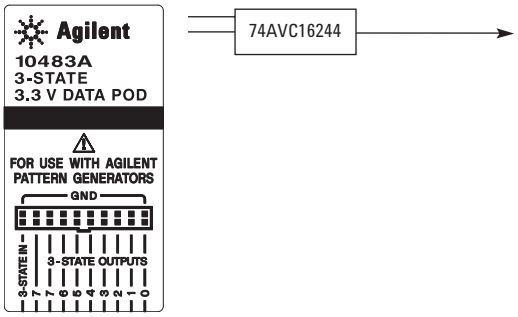
### Agilent 10476A 3-State 1.8 Volt Data Pod

| | |
|---|---|
| Output type | 74AVC16244 |
| 3-state enable | negative true, 38 KΩ to GND, enabled on no connect |
| Maximum clock | 300 MHz |
| Skew [1] | typical < 1.5 ns; worst case = 2 ns |
| Recommended lead set | Agilent 10498A |



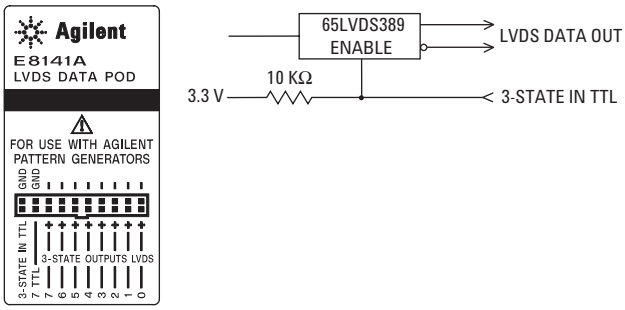

### Agilent 10483A 3-State 3.3 Volt Data Pod

| | |
|---|---|
| Output type | 74AVC16244 |
| 3-state enable | negative true, 38 KΩ to GND, enabled on no connect |
| Maximum clock | 300 MHz |
| Skew [1] | typical < 1.5 ns; worst case = 2 ns |
| Recommended lead set | Agilent 10498A |




### Agilent E8141A LVDS Data Pod

| | |
|---|---|
| Output type | 65LVDS389 (LVDS data lines)<br>10H125 (TTL non-3-state channel 7) |
| 3-state enable | positive true TTL; no connect=enabled |
| Maximum clock | 300 MHz |
| Skew | typical < 1 ns; worst case = 2 ns |
| Recommended lead set: | E8142A |
| Recommended lead set | Agilent 10498A |




[1] Typical skew measurements made at pod connector with approximately 10 pF/50 KΩ load to GND; worst case skew numbers are a calculation of worst case conditions through circuits. Both numbers apply to any channel within a single or multiple module system.

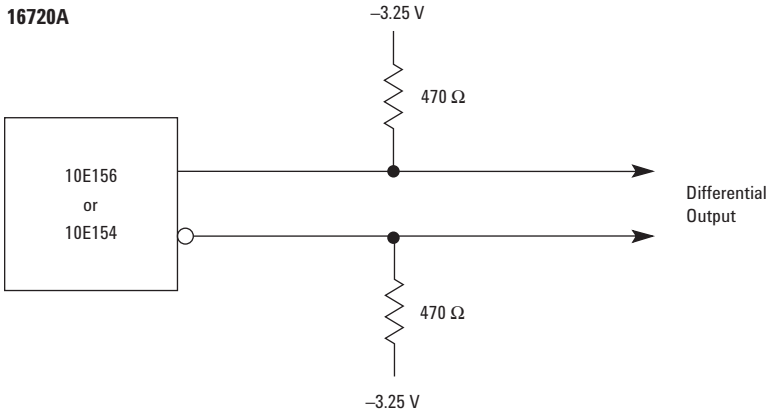
# Agilent 16720A Pattern Generator Specifications and Characteristics



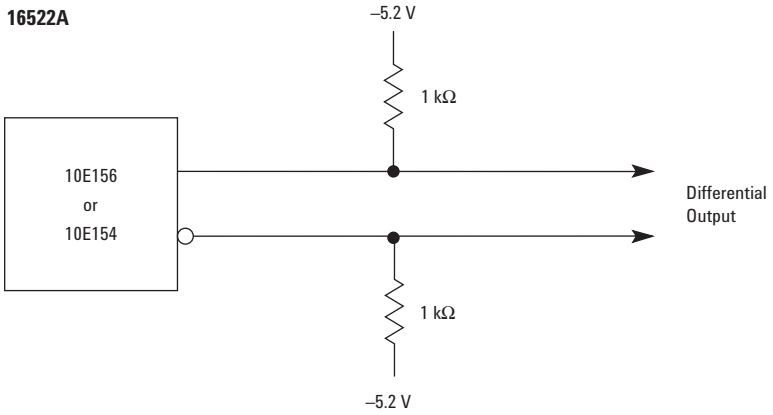
## Data Cable Characteristics Without a Data Pod

The Agilent 16720A data cables without a data pod provide an ECL terminated (1 KΩ to –5.2V) differential signal (from a type 10E156 or 10E154 driver). These are usable when received by a differential receiver, preferably with a 100 Ω termination across the lines. These signals should not be used single ended due to the slow fall time and shifted voltage threshold (they are not ECL compatible).

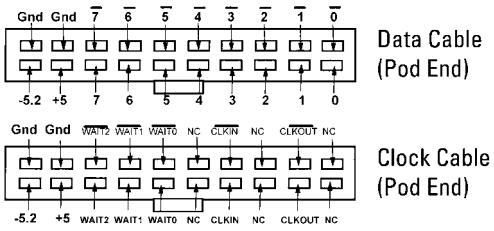
**16720A**




**16522A**

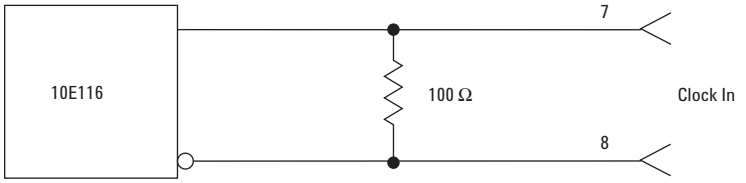


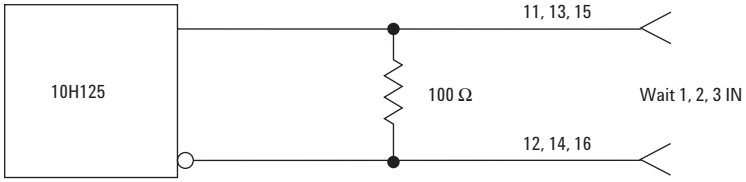

**16720A Cable Pin Outs**

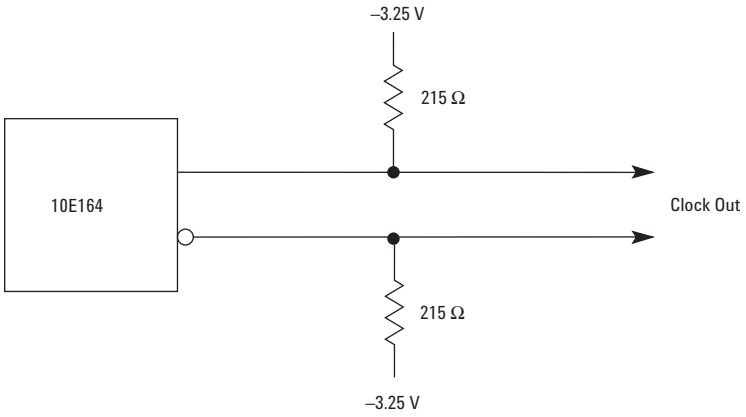


### Clock Cable Characteristics Without a Clock Pod

The Agilent 16720A clock cables without a clock pod provide an ECL terminated (1 KΩ to –5.2V) differential signal (from a type 10E164 driver). These are usable when received by a differential receiver, preferably with a 100 Ω termination across the lines. These signals should not be used single ended due to the slow fall time and shifted voltage threshold (they are not ECL compatible).



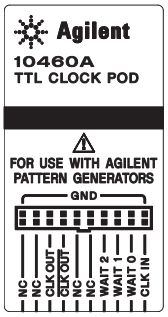
# Agilent 16720A Pattern Generator Specifications and Characteristics

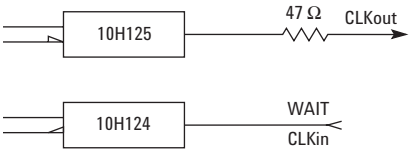


## Clock Pod Characteristics

### 10460A TTL Clock Pod

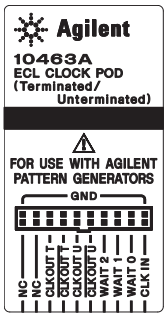
| | |
|---|---|
| Clock output type | 10H125 with 47 Ω series; true & inverted |
| Clock output rate | 100 MHz maximum |
| Clock out delay | approximately 8 ns total in 14 steps (16720A only);<br>11 ns maximum in 9 steps (16522A only) |
| Clock input type | TTL – 10H124 |
| Clock input rate | dc to 100 MHz |
| Pattern input type | TTL – 10H124 (no connect is logic 1) |
| Clock-in to clock-out | approximately 30 ns |
| Pattern-in to recognition | approximately 15 ns + 1 clk period |
| Recommended lead set | Agilent 10474A |

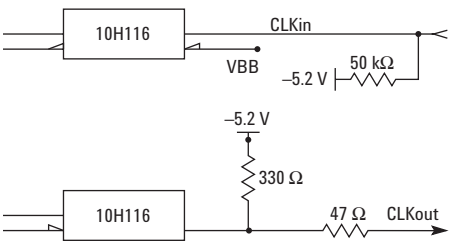



### 10463A ECL Clock Pod

| | |
|---|---|
| Clock output type | 10H116 differential unterminated; and differential with 330 Ω to –5.2V and 47 Ω series |
| Clock output rate | 300 MHz maximum |
| Clock out delay | approximately 8 ns total in 14 steps (16720A only);<br>11 ns maximum in 9 steps (16522A only) |
| Clock input type | ECL – 10H116 with 50 KΩ to –5.2v |
| Clock input rate | dc to 300 MHz |
| Pattern input type | ECL – 10H116 with 50 KΩ (no connect is logic 0) |
| Clock-in to clock-out | approximately 30 ns |
| Pattern-in to recognition | approximately 15 ns + 1 clk period |
| Recommended lead set | Agilent 10474A |



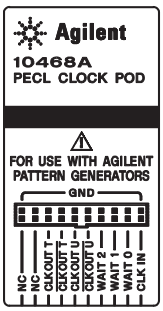



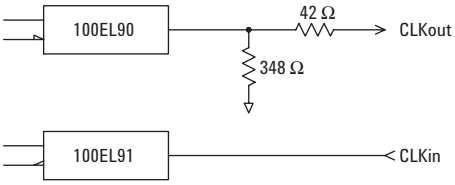
# Agilent 16720A Pattern Generator Specifications and Characteristics



### 10468A 5 volt PECL Clock Pod

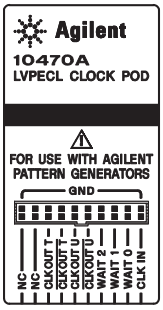
| | |
|---|---|
| Clock output type | 100EL90 (5V) with 348 ohm pulldown to ground and 42 ohm in series |
| Clock output rate | 300 MHz maximum |
| Clock out delay | approximately 8 ns total in 14 steps (16720A only);<br>11 ns maximum in 9 steps (16522A only) |
| Clock input type | 100EL91 PECL (5V), no termination |
| Clock input rate | dc to 300 MHz |
| Pattern input type | 100EL91 PECL (5V), no termination (no connect is logic 0) |
| Clock-in to clock-out | approximately 30 ns |
| Pattern-in to recognition | approximately 15 ns + 1 clk period |
| Recommended lead set | Agilent 10498A |

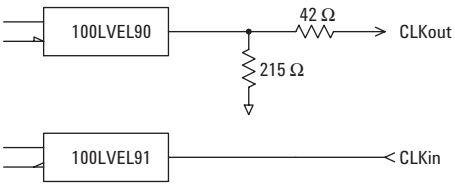



### 10470A 3.3 volt LVPECL Clock Pod

| | |
|---|---|
| Clock output type | 100LVEL90 (3.3V) with 215 ohm pulldown to ground and 42 ohm in series |
| Clock output rate | 300 MHz maximum |
| Clock out delay | approximately 8 ns total in 14 steps (16720A only);<br>11 ns maximum in 9 steps (16522A only) |
| Clock input type | 100LVEL91 LVPECL (3.3V), no termination |
| Clock input rate | dc to 300 MHz |
| Pattern input type | 100LVEL91 LVPECL (3.3V), no termination (no connect is logic 0) |
| Clock-in to clock-out | approximately 30 ns |
| Pattern-in to recognition | approximately 15 ns + 1 clk period |
| Recommended lead set | Agilent 10498A |



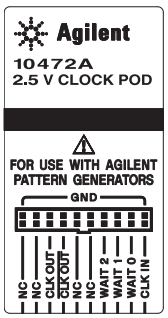



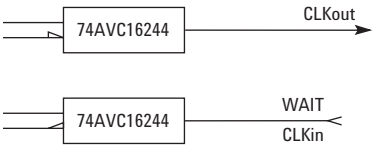
# Agilent 16720A Pattern Generator Specifications and Characteristics



### 10472A 2.5 volt Clock Pod

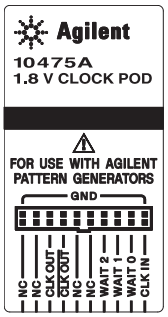
| | |
|---|---|
| Clock output type | 74AVC16244 |
| Clock output rate | 200 MHz maximum |
| Clock out delay | approximately 8 ns total in 14 steps (16720A only);<br>11 ns maximum in 9 steps (16522A only) |
| Clock input type | 74AVC16244 (3.6V max) |
| Clock input rate | dc to 200 MHz |
| Pattern input type | 74AVC16244 (3.6V max; no connect is logic 0) |
| Clock-in to clock-out | approximately 30 ns |
| Pattern-in to recognition | approximately 15 ns + 1 clk period |
| Recommended lead set | Agilent 10498A |

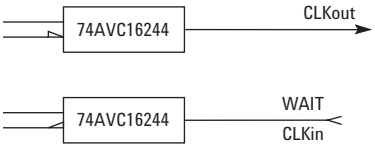



### 10475A 1.8 volt Clock Pod

| | |
|---|---|
| Clock output type | 74AVC16244 |
| Clock output rate | 200 MHz maximum |
| Clock out delay | approximately 8 ns total in 14 steps (16720A only);<br>11 ns maximum in 9 steps (16522A only) |
| Clock input type | 74AVC16244 (3.6V max) |
| Clock input rate | dc to 200 MHz |
| Pattern input type | 74AVC16244 (3.6V max; no connect is logic 0) |
| Clock-in to clock-out | approximately 30 ns |
| Pattern-in to recognition | approximately 15 ns + 1 clk period |
| Recommended lead set | Agilent 10498A |



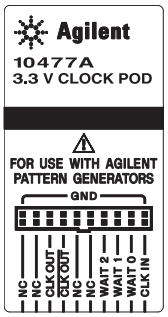



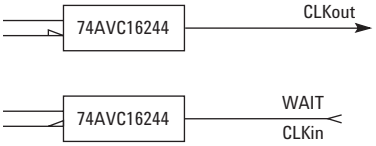
# Agilent 16720A Pattern Generator Specifications and Characteristics



### 10477A 3.3 volt Clock Pod

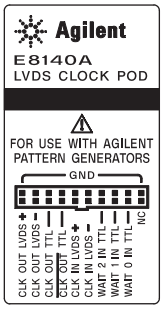
| | |
|---|---|
| Clock output type | 74AVC16244 |
| Clock output rate | 200 MHz maximum |
| Clock out delay | approximately 8 ns total in 14 steps (16720A only); 11 ns maximum in 9 steps (16522A only) |
| Clock input type | 74AVC16244 (3.6V max) |
| Clock input rate | dc to 200 MHz |
| Pattern input type | 74AVC16244 (3.6V max; no connect is logic 0) |
| Clock-in to clock-out | approximately 30 ns |
| Pattern-in to recognition | approximately 15 ns + 1 clk period |
| Recommended lead set | Agilent 10498A |

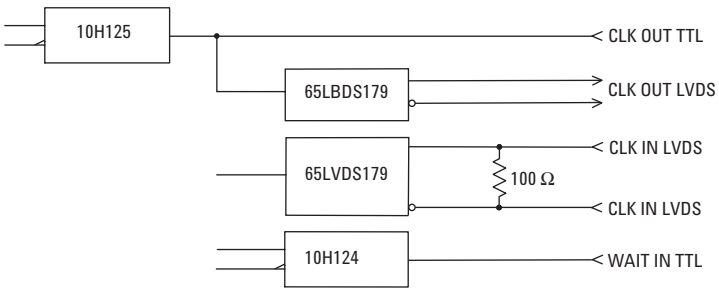



### E8140A LVDS Clock Pod

| | |
|---|---|
| Clock output type | 65LVDS179 (LVDS) and 10H125 (TTL) |
| Clock output rate | 200 MHz maximum (LVDS and TTL) |
| Clock out delay | approximately 8 ns total in 14 steps |
| Clock input type | 65LVDS179 (LVDS with 100 ohm) |
| Clock input rate | dc to 150 MHz (LVDS) |
| Pattern input type | 10H124 (TTL) (no connect = logic 1) |
| Clock-in to clock-out | approximately 30 ns |
| Pattern-in to recognition | approximately 15 ns + 1 clk period |
| Recommended lead set | Agilent 10498A |



# Agilent Module Specifications and Characteristics



| Power Requirements |
|---|
| All necessary power is supplied by the backplane connector of the logic analysis system mainframe. |

| Environmental Characteristics |
|---|
| Indoor use only |

| Operating Environment | |
|---|---|
| Temperature | 0 to 40 °C (+32 to +104 °F) when operating in a 16900A or 16902A/B mainframe.<br>0 to 45 °C (+32 to +113 °F) when operating in a 16901A mainframe.<br>0 to 50 °C (+32 to +122 °F) when operating in a 16903A mainframe. |
| Humidity | 0 to 80% relative humidity at 40 °C (+104 °F). Reliability is enhanced when operating within the range 20% to 80% non-condensing. |
| Altitude | 0 to 3000 m (10,000 ft) |
| Vibration | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 0.2 g rms |

| Non-Operating Environment | |
|---|---|
| Temperature | –40 to +75 °C (–40 to +167 °F). Protect the instrument from temperature extremes which cause condensation on the instrument. |
| Humidity | 0 to 90% at 65 °C (149 °F) |
| Altitude | 0 to 15,300 m (50,000 ft) |
| Vibration (in shipping carton) | Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 2.41 g rms; and swept sine resonant search, 5 to 500 Hz, 0.50 g (0-peak), 5-minute resonant dwell at 4 resonances per axis. |
| See individual probe Specifications and Characteristics for probe environmental characteristics. | |

The 16900 Series logic analysis system also supports the following logic analysis modules.

| State/Timing Modules |
|---|
| 16740A, 16741A, 16742A |
| 16750A/B, 16751A/B, 16752A/B |
| 16753A, 16754A, 16755A, 16756A |

## Related literature

| Publication title | Publication type | Publication number |
|---|---|---|
| *Agilent 16900 Series Logic Analysis System Mainframes* | Data Sheet | 5989-0421EN |
| *Agilent Technologies 16800 Series Portable Logic Analyzers* | Brochure | 5989-5062EN |
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