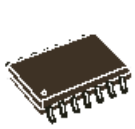
# L6392

## High-voltage high and low side driver

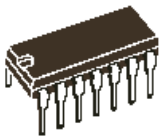
**Preliminary Data**

## Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability:
  - 270 mA source
  - 430 mA sink
- Switching times 75/35 nsec rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Operational amplifier for advanced current sensing
- Adjustable dead-time
- Interlocking function
- Compact and simplified layout
- Bill of material reduction
- Flexible, easy and fast design



DIP-14



SO-14

## Description

The L6392 is a high-voltage device, manufactured with the BCD “OFF-LINE" technology. It has a monolitich half-bridge gate driver for N-channel Power MOSFET or IGBT.

The high side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy of interfacing microcont roller/DSP

The IC embeds an op amp suitable for advanced current sensing in applications such as field oriented motor control.

## Application

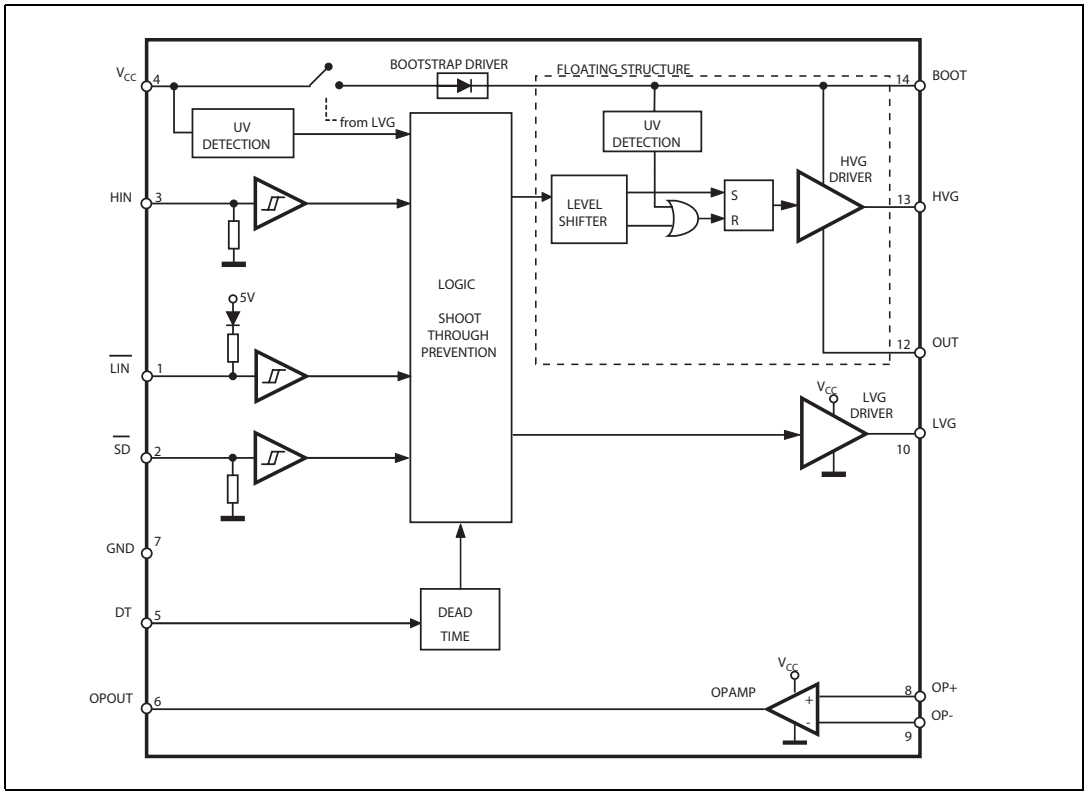
**Table 1. Device summary**

| Order codes | Package | Packaging |
|---|---|---|
| L6392 | DIP-14 | Tube |
| L6392D | SO-14 | Tube |
| L6392D013TR | SO-14 | Tape and reel |

# Contents

# 1 Block diagram

**Figure 1. Block diagram**



# 2 Pin connection

**Figure 2. Pins connection (top view)**

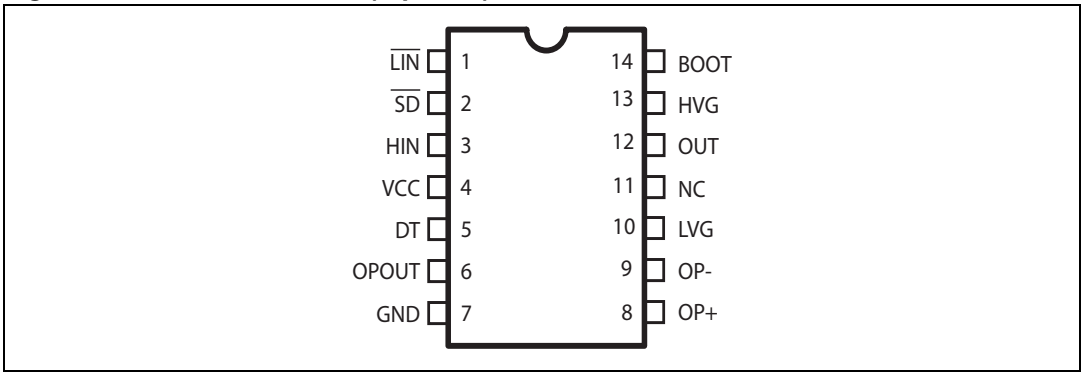



**Table 2. Pin description**

| Pin N# | Pin name | Type | Function |
|---|---|---|---|
| 1 | $\overline{\text{LIN}}$ | I | Low side driver logic input (active low) |
| 2 | $\overline{\text{SD}}$ (1) | I | Shut down logic input (active low) |
| 3 | HIN | I | High side driver logic input (active high) |
| 4 | VCC | P | Lower section supply voltage |
| 5 | DT | I | Dead time setting |
| 6 | OPOUT | O | Opamp output |
| 7 | GND | P | Ground |
| 8 | OP+ | I | Opamp non inverting input |
| 9 | OP- | I | Opamp inverting input |
| 10 | LVG (1) | O | Low side driver output |
| 11 | NC | | Not connected |
| 12 | OUT | P | High side (floating) common voltage |
| 13 | HVG (1) | O | High side driver output |
| 14 | BOOT | P | Bootstrapped supply voltage |

1. The circuit guarantees less than 1 V on the LVG and HVG pins (@ Isink = 10 mA), with $V_{CC}$ > 3 V. This allows to omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in $\overline{\text{SD}}$ condition.

# 3 Truth table

**Table 3. Truth table**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{SD}$ | $\overline{LIN}$ | HIN | LVG | HVG |
| L | X | X | L | L |
| H | L | L | H | L |
| H | L | H | L | L |
| H | H | L | L | L |
| H | H | H | L | H |

*Note: X: don't care*

# 4 Electrical data

## 4.1 Absolute maximum ratings

**Table 4. Absolute maximum rating**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{out}$ | Output voltage | $V_{boot}$ -21 to $V_{boot}$ +0.3 | V |
| $V_{CC}$ | Supply voltage | - 0.3 to + 21 | V |
| $V_{op+}$ | Opamp non-inverting input | -0.3 to $V_{CC}$ +0.3 | V |
| $V_{op-}$ | Opamp inverting input | -0.3 to $V_{CC}$ +0.3 | V |
| $V_{boot}$ | Floating supply voltage | $V_{CC}$ - 0.3 to 620 | V |
| $V_{hvg}$ | High side gate output voltage | $V_{out}$ - 0.3 to $V_{boot}$ + 0.3 | V |
| $V_{lvg}$ | Low side gate output voltage | -0.3 to $V_{CC}$ + 0.3 | V |
| $V_i$ | Logic input voltage | -0.3 to 15 | V |
| $dV_{out}/dt$ | Allowed output slew rate | 50 | V/ns |
| $P_{tot}$ | Total power dissipation ($T_A$= 85 °C) | TBD | mW |
| $T_J$ | Junction temperature | 150 | °C |
| $T_{stg}$ | Storage temperature | -50 to 150 | °C |

*Note: ESD immunity for pins 12, 13 and 14 is guaranteed up to TBD (Human Body Model)*

## 4.2 Thermal data

**Table 5. Thermal data**

| Symbol | Parameter | SO-14 | DIP-14 | Unit |
|---|---|---|---|---|
| $R_{th(JA)}$ | Thermal resistance junction to ambient | 165 | 100 | °C/W |

## 4.3 Recommended operating conditions

**Table 6. Recommended operating conditions**

| Symbol | Pin | Parameter | Test condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{out}$ | 12 | Output voltage (1) | | | 580 | V |
| $V_{BS}$ (2) | 14 | Floating supply voltage (1) | | TBD | TBD | V |
| $f_{sw}$ | | Switching frequency | HVG, LVG load $C_L$ = 1nF | | 800 | kHz |
| $V_{CC}$ | 4 | Supply voltage | | TBD | TBD | V |
| $T_J$ | | Junction temperature | | -40 | 125 | °C |

1. If the condition TBDV< $V_{boot}$ - $V_{out}$ < TBD V and $V_{boot}$ < TBD V are guaranteed, $V_{out}$ can range from TBD V to 580 V.
2. $V_{BS}$ = $V_{boot}$ -$V_{out}$

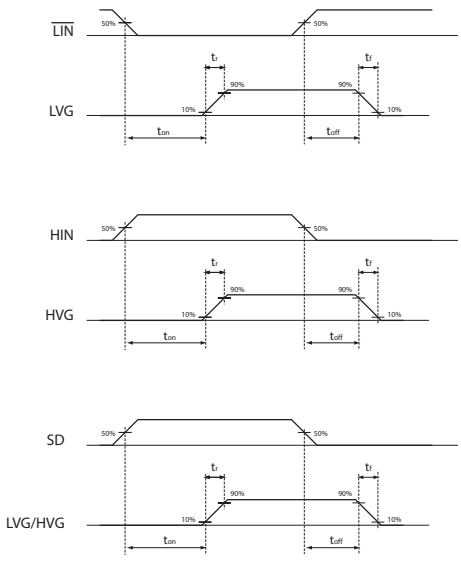
# 5 Electrical characteristics

## 5.1 AC operation

**Table 7. AC operation electrical characteristics ($V_{CC}$ = 15V; $T_J$ =+25 °C)**

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{on}$ | 1 vs 10<br>3 vs 13 | High/low side driver turn-on propagation delay | $V_{out}$ = 0 V<br>$V_{boot}$ = $V_{cc}$<br>$C_L$ = 1nF<br>$V_i$ = 0 to 3.3 V<br>See *Figure 3 on page 7* | | 125 | | ns |
| $t_{off}$ | | High/low side driver turn-off propagation delay | | | 125 | | ns |
| $t_{sd}$ | 2 vs 10, 13 | Shut down to high/low side propagation delay | | | 125 | | ns |
| MT | | Delay matching, HS and LS turn-on/off | | | | 40 | ns |
| dt | 5 | Dead time setting range | $R_{dt}$=0; $C_L$=1 nF; $C_{DT}$ =100 nF<br>$R_{dt}$=37 kΩ;$C_L$=1 nF;$C_{DT}$=100 nF<br>$R_{dt}$=136 kΩ;$C_L$=1 nF;$C_{DT}$=100 nF<br>$R_{dt}$=260 kΩ;$C_L$=1 nF;$C_{DT}$=100 nF | | 0.15<br>0.5<br>1.5<br>2.8 | | µs<br>µs<br>µs<br>µs |
| MDT | | Matching dead time | $R_{dt}$=0 Ω; $C_L$=1 nF; $C_{DT}$ =100 nF<br>$R_{dt}$=37 kΩ;$C_L$=1 nF;$C_{DT}$=100 nF<br>$R_{dt}$=136 kΩ;$C_L$=1 nF;$C_{DT}$=100 nF<br>$R_{dt}$=26 0kΩ;$C_L$=1 nF;$C_{DT}$=100 nF | | 60<br>TBD<br>TBD<br>TBD | | ns<br>ns<br>ns<br>ns |
| $t_r$ | 10, 13 | Rise time | $C_L$ = 1 nF | | 75 | | ns |
| $t_f$ | | Fall time | $C_L$ = 1 nF | | 35 | | ns |

**Figure 3. Timing characteristics**



## 5.2 DC operation

**Table 8. DC operation electrical characteristics ($V_{CC}$ = 15 V;$T_J$ = +25 °C)**

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Low supply voltage section** | | | | | | | |
| $V_{cc\_hys}$ | 4 | $V_{cc}$ UV hysteresis | | 700 | 1400 | | mV |
| $V_{cc\_thON}$ | | $V_{cc}$ UV turn ON threshold | | | 11.8 | | V |
| $V_{cc\_thOFF}$ | | $V_{cc}$ UV turn OFF threshold | | | 10.4 | | V |
| $I_{qccu}$ | | Undervoltage quiescent supply current | $V_{CC}$ = 10 V<br>$\overline{SD}$ = 5V; $\overline{LIN}$ = 5V;<br>HIN = GND;<br>$R_{DT}$ = 0 Ω;<br>OP + = GND; OP - = 5 V | | 110 | 150 | µA |
| $I_{qcc}$ | | Quiescent current | $V_{CC}$ = 15 V<br>$\overline{SD}$ = 5 V; $\overline{LIN}$ = 5 V;<br>HIN = GND;<br>$R_{DT}$ = 0 Ω;<br>OP + = GND; OP - = 5 V | | 680 | 1060 | µA |
| **Bootstrapped supply voltage section** | | | | | | | |
| $V_{BS\_hys}$ | 14 | $V_{BS}$ UV hysteresis | | 700 | 1400 | | mV |
| $V_{BS\_thON}$ | | $V_{BS}$ UV turn ON threshold | | | 11.6 | | V |
| $V_{BS\_thOFF}$ | | $V_{BS}$ UV turn OFF threshold | | | 10.2 | | V |
| $I_{QBSU}$ | | Undervoltage $V_{BS}$ quiescent current | $V_{BS}$ = 10 V<br>$\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V;<br>$R_{DT}$ = 0 Ω;<br>OP + = GND; OP - = 5 V | | 70 | 110 | µA |
| $I_{QBS}$ | | $V_{BS}$ quiescent current | $V_{BS}$ = 15 V<br>$\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V;<br>$R_{DT}$ = 0 Ω;<br>OP + = GND; OP - = 5 V | | 150 | 210 | µA |

**Table 8. DC operation electrical characteristics ($V_{CC}$ = 15 V;$T_J$ = +25 °C)**

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{LK}$ | | High voltage leakage current | $V_{hvg} = V_{out} = V_{boot}$ = 600 V | | | 10 | µA |
| $R_{dson}$ | | Bootstrap driver on resistance (1) | LVG ON | | 120 | | Ω |
| **Driving buffers section** | | | | | | | |
| $I_{so}$ | 10, 13 | High/low side source short circuit current | $V_i = V_{ih}$ ($t_p$ < 10 ms) | | 270 | | mA |
| $I_{si}$ | | High/low side sink short circuit current | $V_i = V_{il}$ (tp < 10 ms) | | 430 | | mA |
| **Logic inputs** | | | | | | | |
| $V_{il}$ | 1, 2, 3 | Low level logic threshold voltage | | | | 0.83 | V |
| $V_{ih}$ | | High level logic threshold voltage | | 2.21 | | | V |
| $I_{HINh}$ | 3 | HIN logic “1” input bias current | HIN = 15 V | | 175 | 260 | µA |
| $I_{HINl}$ | | HIN logic “0” input bias current | HIN = 0 V | | | 1 | µA |
| $I_{LINh}$ | 1 | $\overline{LIN}$ logic “1” input bias current | $\overline{LIN}$ = 0 V | | 6 | 40 | µA |
| $I_{LINl}$ | | $\overline{LIN}$ logic “0” input bias current | $\overline{LIN}$ = 15 V | | | 1 | µA |
| $I_{SDh}$ | 2 | $\overline{SD}$ logic “1” input bias current | $\overline{SD}$ = 15 V | | 30 | 100 | µA |
| $I_{SDl}$ | | $\overline{SD}$ logic “0” input bias current | $\overline{SD}$ = 0 V | | | 1 | µA |

1. $R_{DSon}$ is tested in the following way:
$R_{DSon} = [(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})] / [I_1(V_{CC},V_{CBOOT1}) - I_2(V_{CC},V_{CBOOT2})]$ where $I_1$ is pin 16 current when $V_{CBOOT} = V_{CBOOT1}$, $I_2$ when $V_{CBOOT} = V_{CBOOT2}$

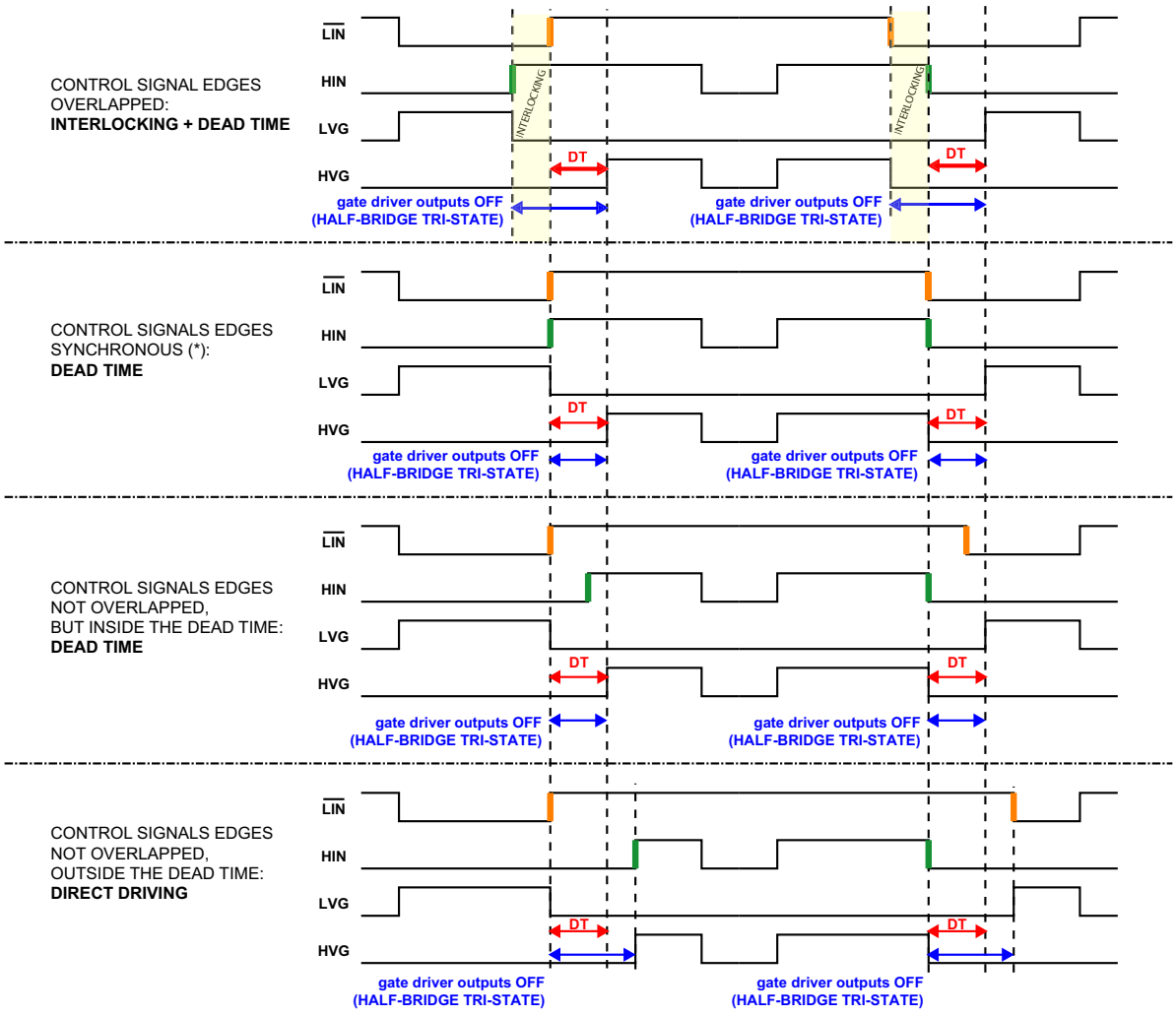
**Table 9. OPAMP characteristics ($V_{CC}$ = 15 V, $T_J$ = +25 °C)**

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{io}$ | 8, 9 | Input offset voltage | $V_O$ = TBD;<br>0 < $V_{icm}$ < $V_{CC}$ -TBD | | | 3 | mV |
| $I_{ib}$ | | Input bias current (1) | | | 15 | 200 | nA |
| $V_{icm}$ | | Input common mode voltage range | | 0 | | $V_{CC}$ - TBD | |
| $V_{OL}$ | 6 | Output voltage swing - low level | Isink = 3.5 mA, $R_L$ = 2 kΩ | | 180 | 360 | mV |
| $V_{OH}$ | | Output voltage swing - high level | Isource = 3.5 mA,<br>$R_L$ = 2 kΩ | 13.5 | 14.3 | | V |
| $I_o$ | | Output short circuit current | Source,<br>$V_{id}$ = TBD; $V_o$ = TBD | 16 | 30 | | mA |
| | | | Sink<br>$V_{id}$ = TBD; $V_o$ = TBD | 50 | 80 | | mA |
| SR | | Slew rate | $V_i$ = TBD; $R_L$ = 2 kΩ;<br>$C_L$ = TBD; unity gain | 2.5 | 3.8 | | V/µs |
| GBWP | | Gain bandwith product | $V_o$ = TBD; $R_L$ = 2 kΩ | | TBD | | MHz |
| $A_{vd}$ | | Large signal voltage gain | | 85 | 95 | | dB |
| SRV | | Power supply rejection ratio | vs $V_{cc}$ | | 85 | | dB |
| CMRR | | Common mode rejection ratio | | 80 | 100 | | dB |

1. The direction of input current is out of the IC.

# 6 Waveforms definitions

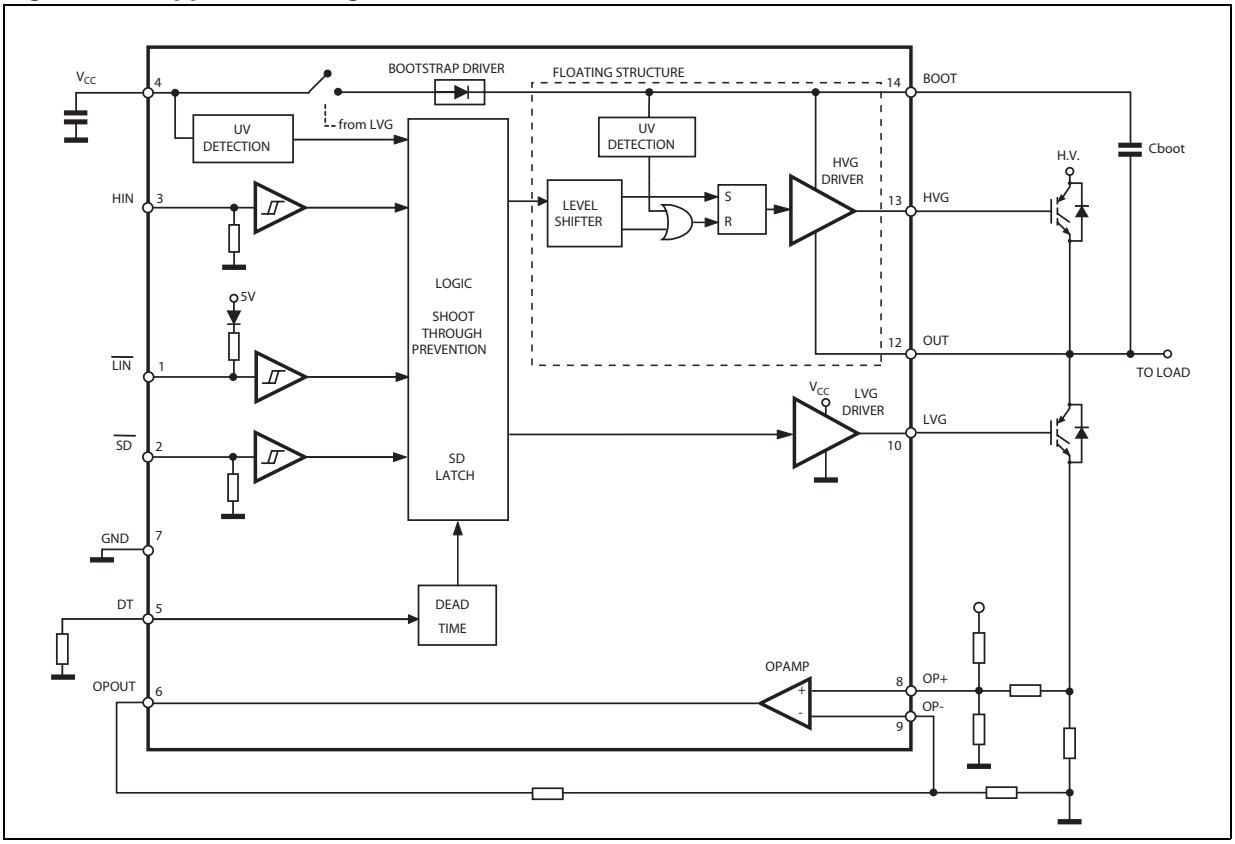
**Figure 4. Dead time - timing waveforms**




*(*) HIN and $\overline{LIN}$ can be connected togheter and driven by just one control signal*

# 7 Typical application diagram

**Figure 5. Application diagram**



# 8 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 6* a). In the L6392 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with diode in series, as shown in *Figure 6* b.
An internal charge pump (*Figure 6* b) provides the DMOS driving voltage.

## 8.1 $C_{BOOT}$ selection and charging

To choose the proper $C_{BOOT}$ value the external MOS can be seen as an equivalent capacitor. This capacitor $C_{EXT}$ is related to the MOS total gate charge:

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors $C_{EXT}$ and $C_{BOOT}$ is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} >>> C_{EXT}$$

e.g.: if $Q_{gate}$ is 30 nC and $V_{gate}$ is 10 V, $C_{EXT}$ is 3 nF. With $C_{BOOT}$ = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the $C_{BOOT}$ selection has to take into account also the leakage and quiescent losses.

e.g.: HVG steady state consumption is lower than 200 µA, so if HVG $T_{ON}$ is 5 ms, $C_{BOOT}$ has to supply 1 µC to $C_{EXT}$. This charge on a 1µF capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives agreat advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if $V_{OUT}$ is close to GND (or lower) and in the meanwhile the LVG is on. The charging time ($T_{charge}$ ) of the $C_{BOOT}$ is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DSON}$ (typical value: 120 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

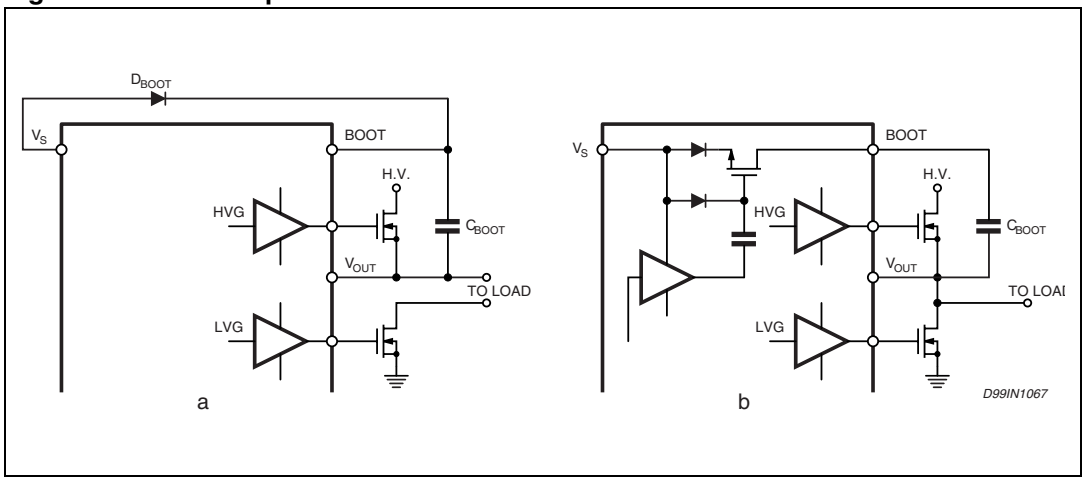
where $Q_{gate}$ is the gate charge of the external power MOS, $R_{dson}$ is the on resistance of the bootstrap DMOS, and $T_{charge}$ is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the $T_{charge}$ is 5 µs. In fact:

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 120\Omega \sim 0.7V$$

$V_{drop}$ has to be taken into account when the voltage drop on $C_{BOOT}$ is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

**Figure 6. Bootstrap driver**



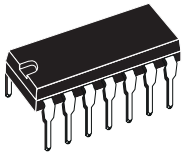
# 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

**Figure 7. DIP-14 mechanical data and package dimensions**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 15.24 | | | 0.600 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | 1.27 | | 2.54 | 0.050 | | 0.100 |

**OUTLINE AND MECHANICAL DATA**



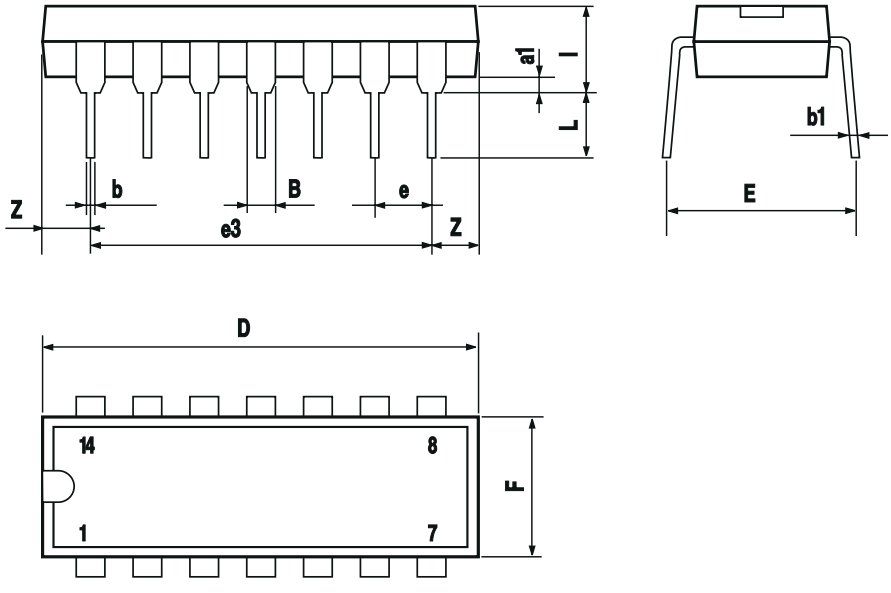
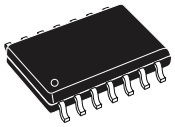


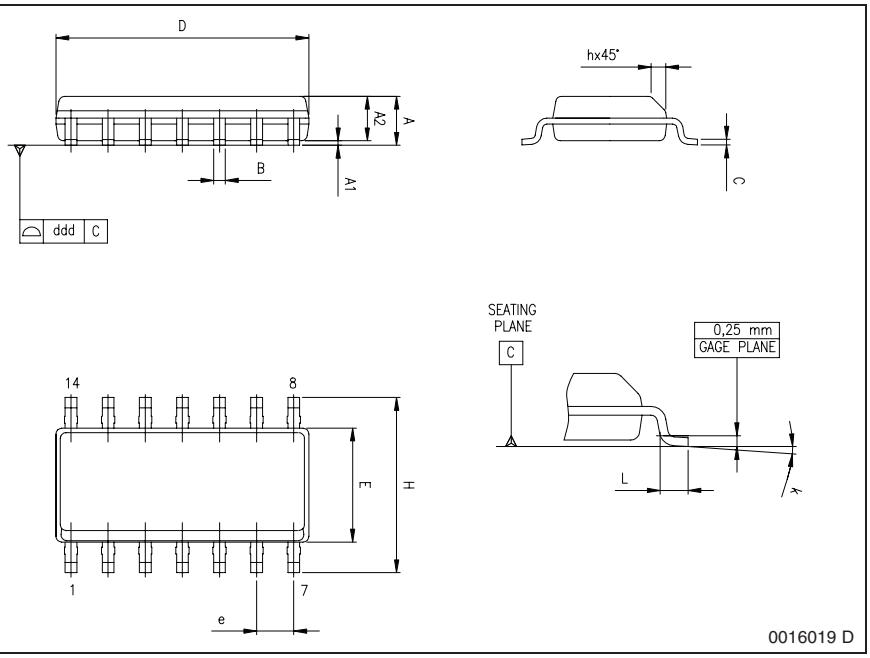
**Figure 8. SO-14 mechanical data and package dimensions**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| A1 | 0.10 | | 0.30 | 0.004 | | 0.012 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.01 |
| D (1) | 8.55 | | 8.75 | 0.337 | | 0.344 |
| E | 3.80 | | 4.0 | 0.150 | | 0.157 |
| e | | 1.27 | | | 0.050 | |
| H | 5.8 | | 6.20 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.01 | | 0.02 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 0° (min.), 8° (max.) | | | | | |
| ddd | | | 0.10 | | | 0.004 |

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

**OUTLINE AND MECHANICAL DATA**





# 10 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 29-Feb-2008 | 1 | Initial release |
| 18-Mar-2008 | 2 | Cover page updated |

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