May 10, 2010

ADC10D1000QML

Low Power, 10-Bit, Dual 1.0 GSPS or Single 2.0 GSPS A/D Converter

1.0 General Description

The ADC10D1000 is the latest advance in National's Ultra-High-Speed ADC family of products. This low-power, high-performance CMOS analog-to-digital converter digitizes signals at 10-bit resolution at sampling rates of up to 1.0 GSPS in dual channel mode or 2.0 GSPS in single channel mode. The ADC10D1000 achieves excellent accuracy and dynamic performance while consuming a typical 2.9 Watts of power. This space grade, Radiation Tolerant part is rad hard to a single event latch up level of greater than 120MeV and a total dose (TID) of 100 krad(Si). The product is packaged in a hermatic 376 column thermally enhanced CCGA package rated over the temperature range of -55°C to +125°C.

The ADC10D1000 builds upon the features, architecture and functionality of the 8-bit GHz family of ADCs. New features include an auto-sync feature for multi-chip synchronization, independent programmable15-bit gain and 12-bit offset adjustment per channel, LC tank filter on the clock input, and the option of two's complement format for the digital output data. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal track-and-hold amplifier and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist, producing a high 8.9 Effective Number of Bits (ENOB) with a 498 MHz input signal and a 1.0 GHz sample rate while providing a 10^{-18} Code Error Rate (C.E.R.) Consuming a typical 2.9 Watts in Non-Demultiplex Mode at 1.0 GSPS from a single 1.9 Volt supply, this device is guaranteed to have no missing codes over the full operating temperature range.

Each channel has its own independent DDR Data Clock, DCLKI and DCLKQ, which are in phase when both channels are powered up, so that only one Data Clock could be used to capture all data, which is sent out at the same rate as the input sample clock. If the 1:2 Demultiplexed Mode is selected, a second 10-bit LVDS bus becomes active for each channel, such that the output data rate is sent out two times slower, but two times wider to relax data-capture timing margin. The two channels (I and Q) can also be interleaved (DES Mode) and used as a single 2.0 GSPS ADC to sample on the Q input. The output formatting is offset binary or two's complement and the Low Voltage Differential Signaling (LVDS) digital outputs are compatible with IEEE 1596.3-1996, with the exception of an adjustable common mode voltage between 0.8V and 1.2V.

2.0 Features

- Total Ionizing Dose 100 krad(Si)
- Single Event Latch-up 120 Mev-cm²/mg
- Excellent accuracy and dynamic performance
- Low power consumption
- R/W SPI Interface for Extended Control Mode
- Internally terminated, buffered, differential analog inputs
- Ability to interleave the two channels to operate one channel at twice the conversion rate
- Test patterns at output for system debug
- Programmable 15-bit gain and 12-bit plus sign offset adjustments
- Option of 1:2 demuxed or 1:1 non-demuxed LVDS outputs
- Auto-sync feature for multi-chip systems
- Single 1.9V±0.1V power supply
- 376 Ceramic Column Grid Array package (28.2mm x 28.2mm x 3.1mm with 1.27mm ball-pitch)

3.0 Key Specifications

(Non-Demux Non-DES Mode, Fs = 1.0 GSPS, Fin = 248 MHz)

- Resolution 10 Bits
- Conversion Rate
  - — Dual channels at 1.0 GSPS (typ)
  - — Single channel at 2.0 GSPS (typ)
- Code Error Rate 10^{-18} (typ)
- ENOB 9.0 bits (typ)
- SNR 56.1 dBc (typ)
- SFDR 63 dBc (typ)
- Full Power Bandwidth 2.8 GHz (typ)
- DNL ±0.2 LSB (typ)
- Power Consumption
  - — Single Channel Enabled 1.64W (typ)
  - — Dual Channels Enabled 2.9W (typ)
  - — Power Down Mode 6 mW (typ)

4.0 Applications

- Data Acquisition Systems
- Wideband Communications
- Direct RF Down Conversion

5.0 Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
ADC10D1000CCMLS **Flight Part**		CCC376A	376 Ceramic Column Grid Array
ADC10D1000CCRQV **Flight Part**	TBD	CCC376A	376 Ceramic Column Grid Array
ADC10D1000CCMPR **Pre-flight Prototype**		CCC376A	376 Ceramic Column Grid Array
ADC10D1000CVAL **Ceramic Evaluation Board**			376 Ceramic Column Grid Array on Evaluation Board

6.0 Block Diagram

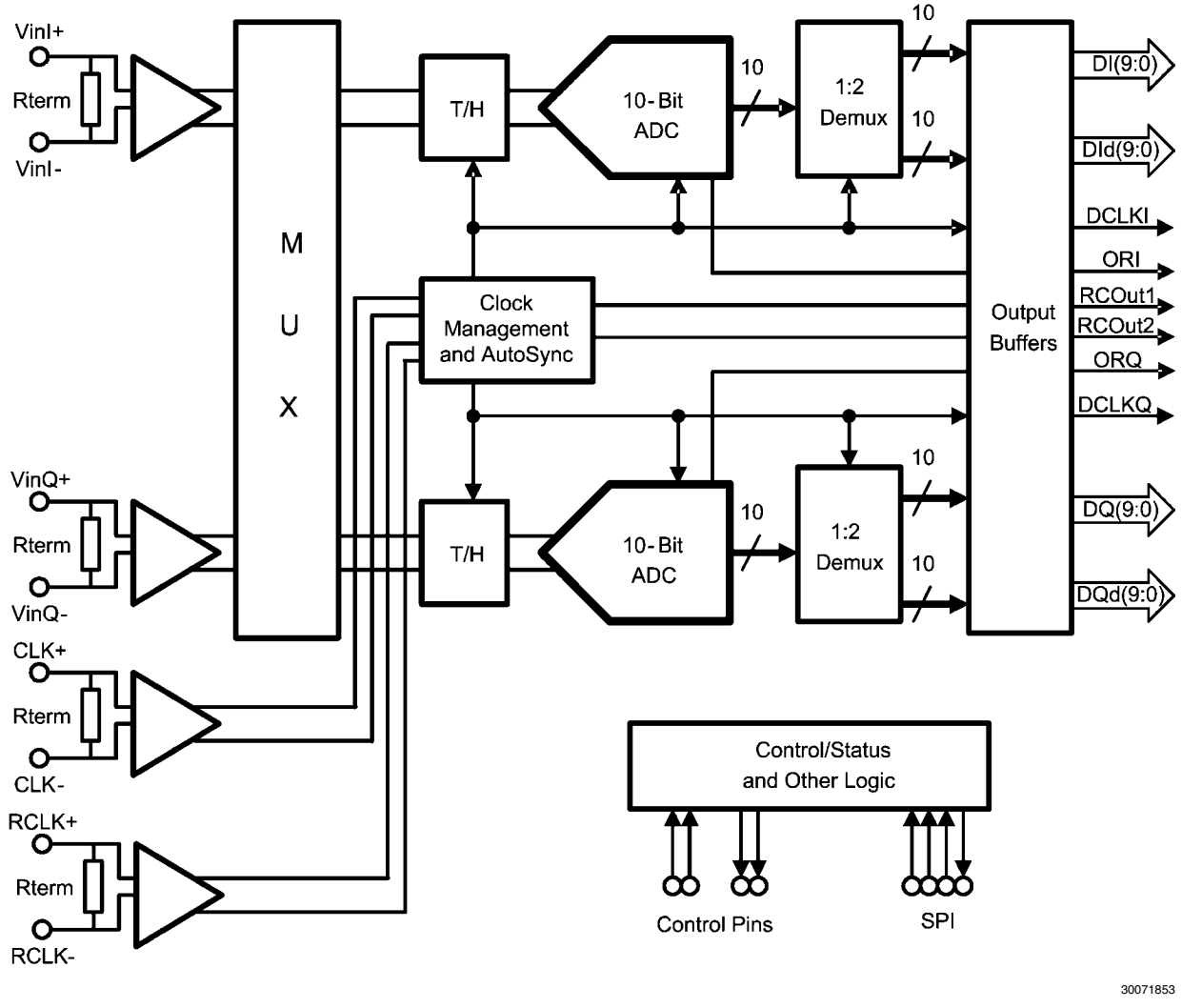

FIGURE 1. Simplified Block Diagram

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7.0 Connection Diagram

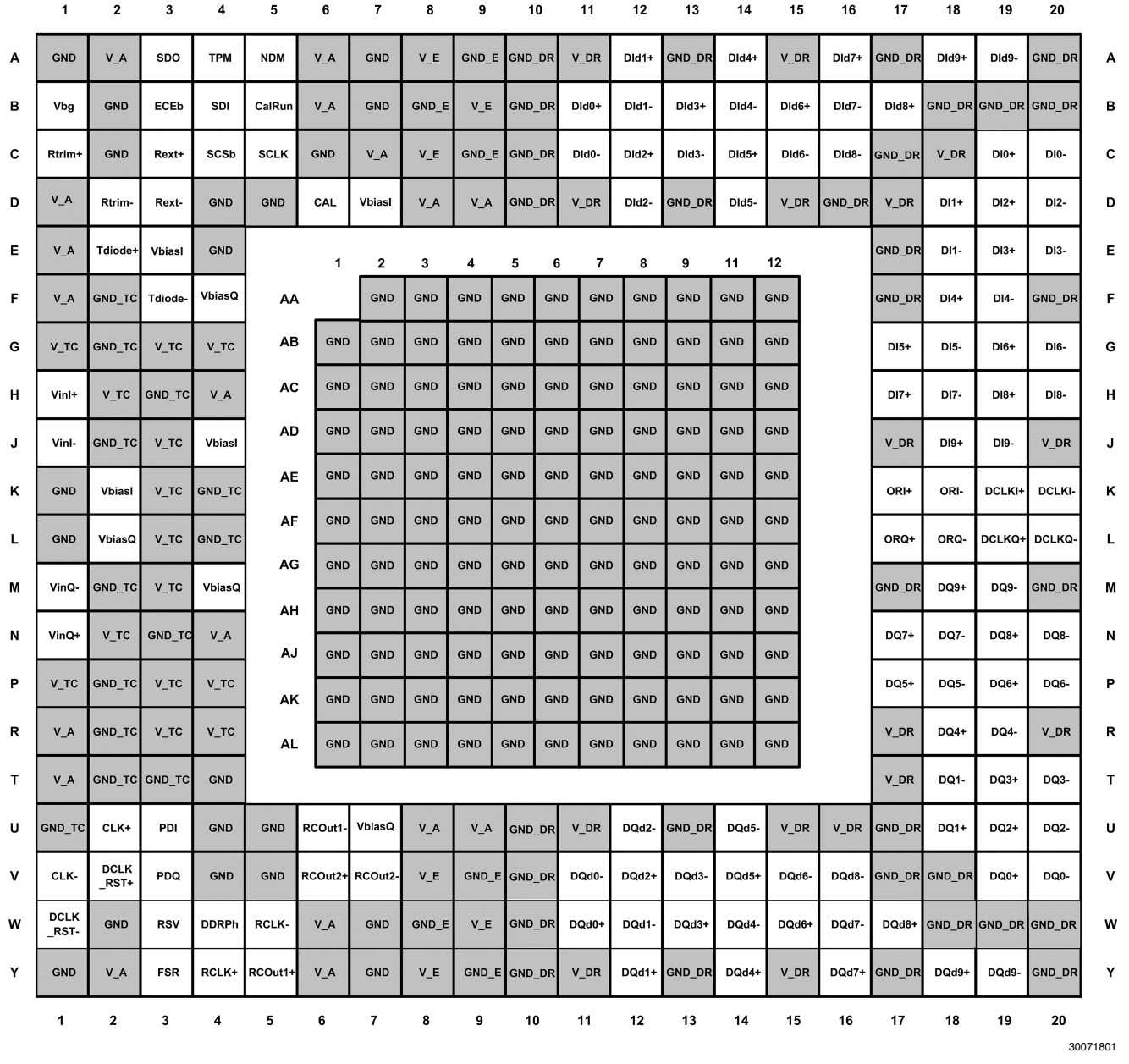
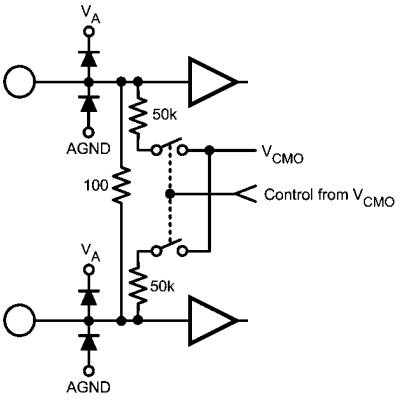
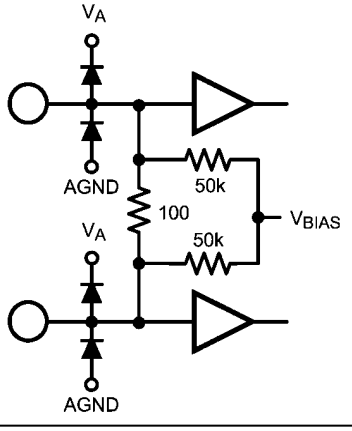
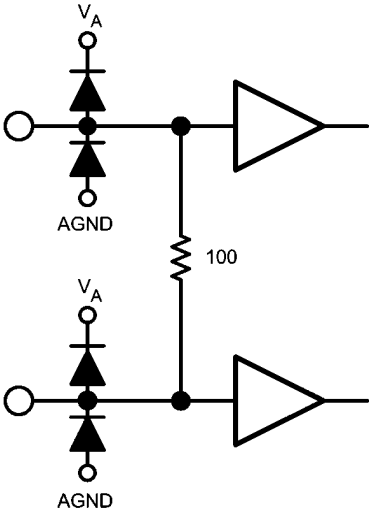


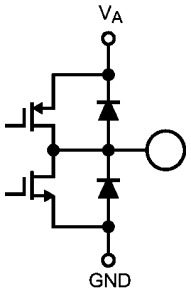
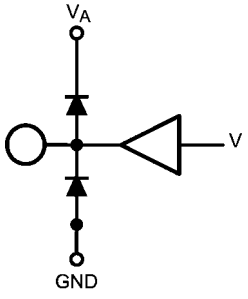
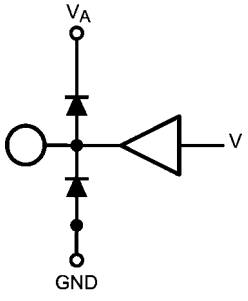
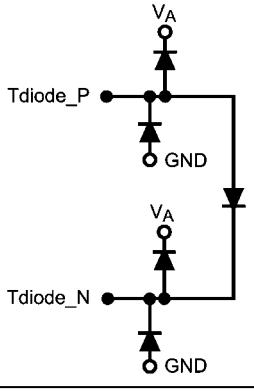
FIGURE 2. ADC10D1000 Connection Diagram

The center ground pins are for thermal dissipation and must be soldered to a ground plane to ensure rated performance. For best performance, a common ground plane on multiple PC board layers is recommended.

8.0 Column Descriptions and Equivalent Circuits

TABLE 1. Analog Front-End and Clock Pins

Column	Name	Equivalent Circuit	Description
H1/J1 N1/M1	VinI+/- VinQ+/-		Differential Signal I- and Q-Inputs. In the Non-Dual Edge Sampling (Non-DES) Mode, each I- and Q-channel is sampled and converted by its respective converter with each positive transition of the CLK+/- input. In the DES Mode and Extended Control Mode (ECM), only the Q-channel may be selected for conversion by the DESQ Bit (Addr: 0**h**, Bit 6). In the DES mode the Q-channel input is converted on the positive and negative edge of the CLK± input. Each I- and Q-channel input has an internal DC-bias. Both channels must be AC coupled. In Non-ECM, the full-scale range of these inputs is determined by FSR (Pin Y3) and both I- and Q-channels have the same full-scale input range. In ECM, the full-scale input range of the I- and Q-channel inputs is independently determined by the setting of Addr: 3**h** and Addr: B**h**, respectively. Note that the higher and lower full-scale input range setting in Non-ECM does not exactly correspond to the maximum and minimum full-scale input range in ECM. Additional features include: an input offset adjust, in Extended Control Mode.
U2/V1	CLK+/-		Differential Converter Sampling Clock. In the Non-DES Mode, the analog inputs are sampled on the positive transitions of this clock signal. In the DES Mode, the Q-channel is sampled on both transitions of this clock. This clock must be AC-coupled. Additional features include: LC filter on the clock input.
V2/W1	DCLK_RST+/-		Differential DCLK Reset. A positive pulse on this input is used to reset the DCLKI+/- and DCLKQ+/- outputs of two or more ADC10D1000s in order to synchronize them with other ADC10D1000s in the system. DCLKI+/- and DCLKQ+/- are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST+/- to become synchronized. The pulse applied here must meet timing relationships with respect to the CLK+/- input. This feature may still be used while the chip is in the AutoSync Mode.

Column	Name	Equivalent Circuit	Description
B1	V_{BG}		Bandgap Voltage Output or LVDS Common-mode Voltage Select. This pin provides the bandgap output voltage and is capable of sourcing/ sinking 100 uA and driving a load of up to 80 pF. Alternately, this pin may be used to select the LVDS digital output common-mode voltage. If tied to logic-high, the higher LVDS common-mode voltage is selected. The lower value is the default.
C1/D2	Rtrim+/-		External Reference and Input Termination Trim Resistor terminals. A 3.3 kΩ ±0.1% resistor should be connected between Rtrim+/-. The Rtrim resistor is used to establish the calibrated 100Ω input impedance of VinI+/-, VinQ+/- and CLK+/-. These impedances may be fine tuned by varying the value of the resistor by a corresponding percentage; however, the tuning range and performance is not guaranteed for such an alternate value.
C3/D3	Rext+/-		A 3.3 kΩ ±0.1% resistor should be connected between Rext+/-. The Rext resistor is used for setting internal temperature-independent bias currents; the value and precision of this resistor should not be compromised.
E2/F3	Tdiode+/-		Temperature Sensor Diode Positive (Anode) and Negative (Cathode) Terminals. This set of pins is used for die temperature measurements.

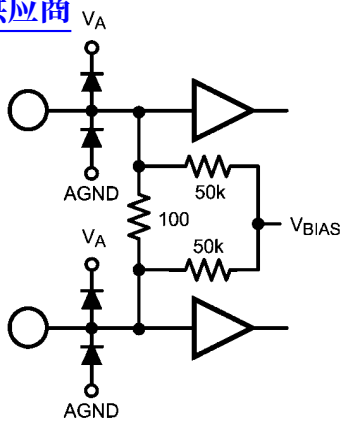
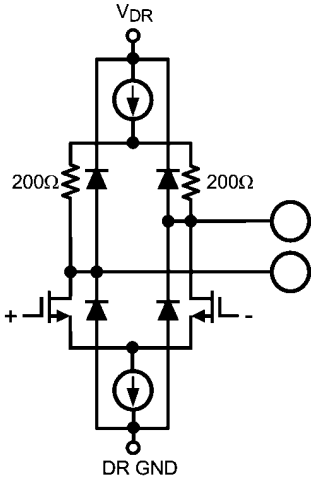
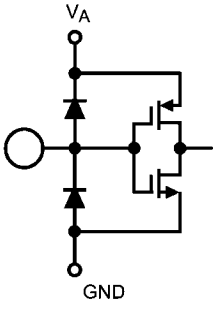
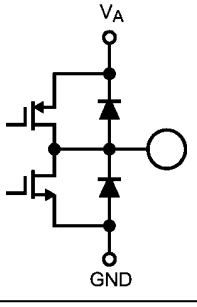
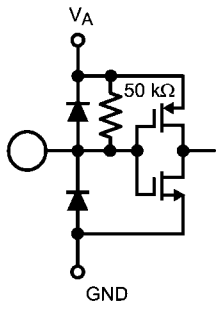
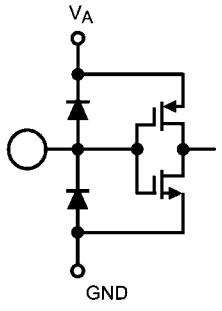
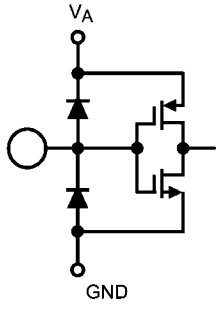
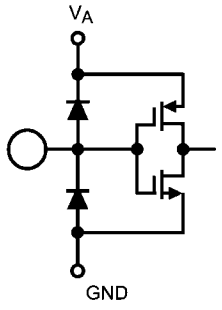
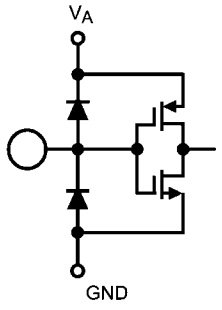
Column	Name	Equivalent Circuit	Description
Y4/W5	RCLK+/-		Reference Clock Input. When the AutoSync feature is active, and the ADC10D1000 is in Slave Mode, the internal divided clocks are synchronized with respect to this input clock. The delay on this clock may be adjusted when synchronizing multiple ADCs. This feature is available in ECM via Control Register (Addr: E**h**).
Y5/U6 V6/V7	RCOut1+/- RCOut2+/-		Reference Clock Output 1 and 2. These signals provide a reference clock at a rate of CLK/4, when enabled, independently of whether the ADC is in Master or Slave Mode. They are used to drive the RCLK of another ADC10D1000, to enable automatic synchronization for multiple ADCs (AutoSync feature.) The impedance of each trace from RCOut1+/- and RCOut2+/- to the RCLK+/- of another ADC10D1000 should be 100Ω differential. Having two clock outputs allows the auto-synchronization to propagate as a binary tree. Use the DOC Bit (Addr: E**h**, Bit 1) to enable/ disable this feature; default is disabled.

TABLE 2. Control and Status Pins

Column	Name	Equivalent Circuit	Description
D6	CAL		Calibration Cycle Initiate. The user can command the device to execute a self-calibration cycle by holding this input high a minimum of t_{CAL_H} after having held it low a minimum of t_{CAL_L}. This pin is active in both ECM and Non-ECM. In ECM, this pin is logically OR'd with the CAL Bit (Addr: 0**h**, Bit 15) in the Control Register. Therefore, both pin and bit must be set low and then either can be set high to execute an on-command calibration.
B5	CalRun		Calibration Running Indication. This output is logic-high while the calibration sequence is executing. This output is logic-low while the calibration sequence is not running.

Column	Name	Equivalent Circuit	Description
U3 V3	PDI PDQ		Power Down I- and Q-channel. Setting either input to logic-high powers down the respective I- or Q-channel converter. Setting either input to logic-low brings the respective I- or Q-channel converter to a fully operational state after a finite time delay. This pin is active in both ECM and Non-ECM. In the ECM, either this pin or the PDI and PDQ Bit in the Control Register can be used to power-down the I- and Q-channel (Addr: 0**h**, Bit 11 and Bit 10), respectively.
A4	TPM		Test Pattern Mode. With this input at logic-high, the device continuously outputs a fixed, repetitive test pattern at the digital outputs. In the ECM, this input is ignored and the test pattern mode can only be activated through the Control Register by the TPM Bit (Addr: 0**h**, Bit 12).
A5	NDM		Non-Demuxed Mode. Setting this input to logic-high causes the digital output bus to be in the 1:1 Non-Demuxed Mode. Setting this input to logic-low causes the digital output bus to be in the 1:2 Demuxed Mode. This feature is pin-controlled only and remains active during ECM and Non-ECM.
Y3	FSR		Full-Scale input Range Select. In Non-ECM, when this input is set to logic-low or logic-high, the full-scale differential input range for both I- and Q-channel inputs is set to the lower or higher value, respectively. In the ECM, this input is ignored and the full-scale range of the I- and Q-channel inputs is independently determined by the setting of Addr: 3**h** and Addr: B**h**, respectively. Note that the higher and lower FSR value in Non-ECM does not precisely correspond to the maximum and minimum available selection in ECM; in ECM, the selection range is greater.
W4	DDRPh		DDR Phase Select. This input, when logic-low, selects the 0-degree Data-to-DCLK phase relationship. When logic-high, it selects the 90-degree Data-to-DCLK phase relationship. This pin only has an effect when the chip is in 1:2 Demuxed Mode, e.g. the NDM pin is set to logic-low. In ECM, this input is ignored and the DDR phase is selected through the Control Register by the DPS Bit (Addr: 0**h**, Bit 14); the default is 0-degree Data-to-DCLK phase relationship.

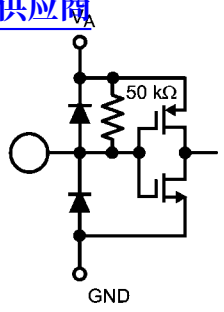
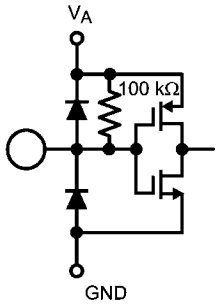
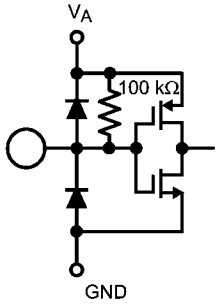
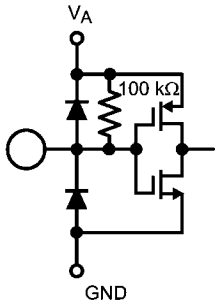
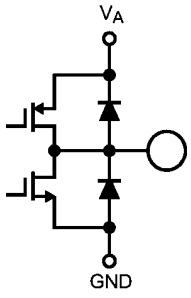
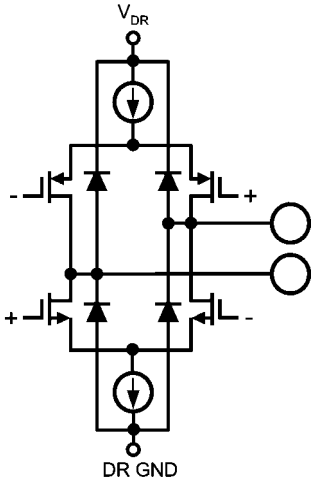
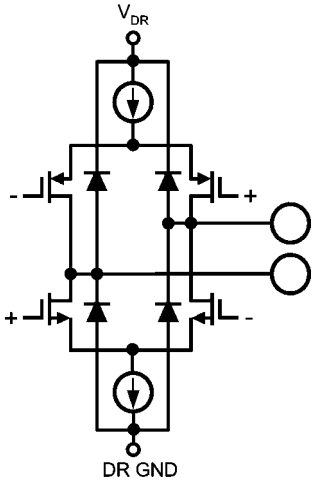
Column	Name	Equivalent Circuit	Description
B3	$\overline{ECE}$		Extended Control Enable bar. Extended feature control through the SPI interface is enabled when this signal is asserted logic-low. In this case, most of the direct control pins have no effect. When this signal is de-asserted, i.e. logic-high, the SPI interface is disabled and the direct control pins are enabled.
C4	$\overline{SCS}$		Serial Chip Select bar. In ECM, when this signal is asserted logic-low, SCLK is used to clock in serial data which is present on the SDI input and to source serial data on the SDO output. When this signal is de-asserted, i.e. logic-high, the SDI input is ignored and the SDO output is in tri-state mode.
C5	SCLK		Serial Clock. In ECM, serial data is shifted into and out of the device synchronously to this clock signal. This clock may be disabled and held logic-low, so long as timing specifications are not violated when the clock is enabled or disabled.
B4	SDI		Serial Data-In. In ECM, serial data is shifted into the device on this pin while $\overline{SCS}$ signal is asserted (logic-low).
A3	SDO		Serial Data-Out. In ECM, serial data is shifted out of the device on this pin while $\overline{SCS}$ signal is asserted (logic-low). This output is in tri-state mode when $\overline{SCS}$ is de-asserted.
W3	RSV	**NONE**	Reserved: This pin is used for internal purposes and should be connected to GND through a 100K Ω resistor.

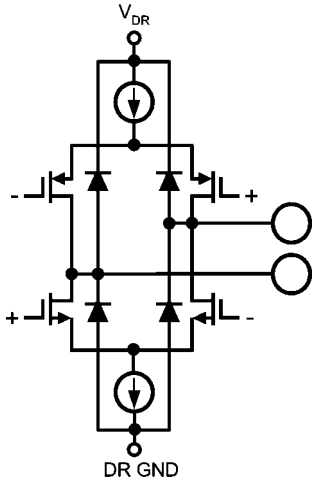
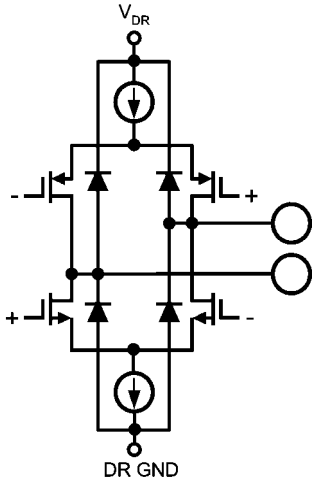
TABLE 3. Power and Ground Pins

Column	Name	Equivalent Circuit	Description
A2, A6, B6, C7, D1, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6	V_A	**NONE**	Analog Power Supply. This supply is tied to the ESD ring. Therefore, it must be powered up before or with any other supply.
G1, G3, G4, H2, J3, K3, L3, M3, N2, P1, P3, P4, R3, R4	V_{TC}	**NONE**	Analog Power Supply for the Track-and-Hold and Clock circuitry.
A11, A15, C18, D11, D15, D17, J17, J20, R17, R20, T17, U11, U15, U16, Y11, Y15	V_{DR}	**NONE**	Power Supply for the Output Drivers.
A8, B9, C8, V8, W9, Y8	V_E	**NONE**	Power Supply for the Digital Encoder.
D7, E3, J4, K2	VbiasI	**NONE**	Bias Voltage I-channel. This is an externally decoupled bias voltage for the I-channel. Each pin should individually be decoupled with a 100nF capacitor via a low resistance, low inductance path to GND.
F4, L2, M4, U7	VbiasQ	**NONE**	Bias Voltage Q-channel. This is an externally decoupled bias voltage for the Q-channel. Each pin should individually be decoupled with a 100nF capacitor via a low resistance, low inductance path to GND.
A1, A7, B2, B7, C2, C6, D4, D5, E4, K1, L1, T4, U4, U5, V4, V5, W2, W7, Y1, Y7, AA2thru AL11	GND	**NONE**	Analog Ground Return.
F2, G2, H3, J2, K4, L4, M2, N3, P2, R2, T2, T3, U1	GND_{TC}	**NONE**	Analog Ground Return for the Track-and-Hold and Clock circuitry.

Column	Name	Equivalent Circuit	Description
A10, A13, A17, A20, B10 B18, B19, B20, C10, C17, D10, D13, D16, E17, F17, F20, M17, M20, U10,U13, U17, V10, V17, V18, W10, W18, W19, W20, Y10, Y13, Y17, Y20	GND_{DR}	**NONE**	Ground Return for the Output Driver.
A9, B8, C9, V9, W8, Y9	GND_E	**NONE**	Ground Return for the Digital Encoder.

TABLE 4. High-Speed Digital Outputs

Column	Name	Equivalent Circuit	Description
K19/K20 L19/L20	DCLKI+/- DCLKQ+/-		Data Clock Output for the I- and Q-channel data bus. These differential clock outputs are used to latch the output data and should always be terminated with a 100Ω differential resistor. Delayed and non-delayed data outputs are supplied synchronously to this signal. In 1:2 Demux Mode or Non-Demux Mode, this signal is at ¼ or ½ the input clock rate, respectively. DCLKI+/- and DCLKQ+/- are always in phase with each other, unless one channel is powered down and do not require a pulse from DCLK_RST+/- to become synchronized.
K17/K18 L17/L18	ORI+/- ORQ+/-		Out-of-Range Output for the I- and Q-channel. This differential output is asserted logic-high while the over- or under-range condition exists, i.e. the differential signal at each respective analog input exceeds the full-scale value. Each OR results refers to the current Data, with which it is clocked out. Each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.

Column	Name	Equivalent Circuit	Description
H18/H19	DI8+/-		I- and Q-channel Digital Data Outputs. In Non-Demux Mode, this LVDS data is transmitted at the sampling clock rate. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the delayed data, i.e. the other ½ of the data which was sampled one clock cycle earlier. Compared with the DId and DQd outputs, these outputs represent the later time samples. Each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver
H19/H20	DI8+/-		
H17/H18	DI7+/-		
G19/G20	DI6+/-		
G17/G18	DI5+/-		
F18/F19	DI4+/-		
E19/E20	DI3+/-		
D19/D20	DI2+/-		
D18/E18	DI1+/-		
C19/C20	DI0+/-		
.	.		
M18/M19	DQ9+/-		
N19/N20	DQ8+/-		
N17/N18	DQ7+/-		
P19/P20	DQ6+/-		
P17/P18	DQ5+/-		
R18/R19	DQ4+/-		
T19/T20	DQ3+/-		
U19/U20	DQ2+/-		
U18/T18	DQ1+/-		
V19/V20	DQ0+/-		
A18/A19	DId9+/-		Delayed I- and Q-channel Digital Data Outputs. In Non-Demux Mode, these outputs are tri-stated. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the non-delayed data, i.e. the other ½ of the data which was sampled one clock cycle later. Compared with the DI and DQ outputs, these outputs represent the earlier time samples. Each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.
B17/C16	DId8+/-		
A16/B16	DId7+/-		
B15/C15	DId6+/-		
C14/D14	DId5+/-		
A14/B14	DId4+/-		
B13/C13	DId3+/-		
C12/D12	DId2+/-		
A12/B12	DId1+/-		
B11/C11	DId0+/-		
.	.		
Y18/Y19	DQd9+/-		
W17/V16	DQd8+/-		
Y16/W16	DQd7+/-		
W15/V15	DQd6+/-		
V14/U14	DQd5+/-		
Y14/W14	DQd4+/-		
W13/V13	DQd3+/-		
V12/U12	DQd2+/-		
Y12/W12	DQd1+/-		
W11/V11	DQd0+/-		

9.0 Absolute Maximum Ratings

(*Note 1*, *Note 2*)

Supply Voltage (V_A, V_{TC}, V_{DR}, V_E)	2.2V
Supply Difference max($V_{A\ /TC/DR\ /E}$) -min($V_{A\ /TC/DR/E}$)	0V to 100 mV
Voltage on Any Input Pin	−0.15V to (V_A +0.15V)
Voltage on V_{IN}^+, V_{IN}^- (Maintaining Common Mode)	−0.15V to 2.5V
Ground Difference max($GND_{TC/DR/E}$) -min($GND_{TC/DR/E}$)	0V to 100 mV
Input Current at Any Pin (*Note 3*)	±50 mA
Power Dissipation at $T_A \leq 85°C$ (*Note 3*)	3.4 W
ESD Susceptibility (*Note 4*)	
Human Body Model	8000V
Charged Device Model	750V
Machine Model	250V
Storage Temperature	−65°C to +150°C

10.0 Operating Ratings

(*Note 1*, *Note 2*)

Ambient Temperature Range	$-55°C \leq T_A \leq +125°C$
Supply Voltage (V_A, V_{TC}, V_E)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
V_{IN}+, V_{IN}- Voltage Range (Maintaining Common Mode)	0V to 2.15V (100% duty cycle) 0V to 2.5V (10% duty cycle)
Ground Difference max($GND_{TC/DR/E}$) -min($GND_{TC/DR/E}$)	0V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	$0.4V_{P-P}$ to $2.0V_{P-P}$

Package Thermal Resistance

Package	θ_{JA}	θ_{JB} To Board
376 Ceramic Column Grid Array	10.4°C / W	3.2°C / W

Solder process specifications in *Section 18.9 BOARD MOUNTING RECOMMENDATION*

11.0 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Setting time at	+25
13	Setting time at	+125
14	Setting time at	-55

12.0 Converter Electrical Characteristics (*Note 13*)

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V_E = +1.9V$; I- and Q-channels AC coupled, FSR Pin = High; C_L = 10 pF; Differential AC coupled Sine Wave Input Clock, f_{CLK} = 1 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = Floating; Non-extended Control Mode; Rext = Rtrim = 3300 Ω ±0.1%; Analog Signal Source Impedance = 100 Ω Differential; 1:2 Demultiplex Non-DES Mode; I- and Q-channels; Duty Cycle Stabilizer on. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted**. All other limits T_A = 25°C, unless otherwise noted. (*Note 5*, *Note 6*, *Note 12*)

TABLE 5. Static Converter Characteristics

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
INL	Integral Non-Linearity (Best fit)	D.C. Coupled, 1 MHz Sine Wave Over-ranged		±0.7		**±1.4**	LSB	1, 2, 3
DNL	Differential Non-Linearity	D.C. Coupled, 1 MHz Sine Wave Over-ranged		±0.2		**±0.5**	LSB	1, 2, 3
	Resolution with No Missing Codes					**10**	bits	1, 2, 3
V_{OFF}	Offset Error			-2.8			LSB	
V_{OFF_ADJ}	Input Offset Adjustment Range	Extended Control Mode		±45			mV	
PFSE	Positive Full-Scale Error		(*Note 8*)			**±28.0**	mV	1, 2, 3
NFSE	Negative Full-Scale Error		(*Note 8*)			**±28.0**	mV	1, 2, 3
	Out of Range Output Code	$(V_{IN}+) - (V_{IN}-) >$ + Full Scale				**1023**		1, 2, 3
		$(V_{IN}+) - (V_{IN}-) <$ – Full Scale				**0**		1, 2, 3

TABLE 6. Dynamic Converter Characteristics

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
FPBW	Full Power Bandwidth	Non-DES Mode		2.8			GHz	
		DES Mode		1.3			GHz	
C.E.R.	Code Error Rate			10^{-18}			Error/ Sample	
	Gain Flatness	D.C. to 498 MHz		±0.25			dBFS	
		D.C. to 1.0 GHz		±0.5			dBFS	
NPR	Noise Power Ratio	fc,notch = 325 MHz, notch width = 25 MHz		47.5			dB	
1:2 Demux Non-DES Mode, Extended Control Mode, FM (14:0) = 7FFFh								
ENOB	Effective Number of Bits	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{Max}		9.0	**8.4**		bits	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**7.8**		bits	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{Max}		8.9	**8.2**		bits	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**7.8**		bits	6
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{Max}		55.8	**52.2**		dB	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**48.5**		dB	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{Max}		55.4	**51.0**		dB	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**48.8**		dB	6
SNR	Signal-to-Noise Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{Max}		56.8	**53.2**		dBc	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**49.4**		dBc	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{Max}		56.1	**52.0**		dBc	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**49.4**		dBc	6
THD	Total Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A =25°C to T_{MAX}		-68		**-59.0**	dBc	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}				**-56.0**	dBc	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		-61		**-58.0**	dBc	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}				**-57.0**	dBc	6
2nd Harm	Second Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS		–75			dBc	
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		–68			dBc	
3rd Harm	Third Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS		–72			dBc	
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		–67			dBc	

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
SFDR	Spurious-Free Dynamic Range	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{Max}		63.0	**59.0**		dBc	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**53.0**		dBc	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{Max}		63.0	**57.5**		dBc	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**54.5**		dBc	6
1:2 Demux Non-DES Mode, Non-Extended Control Mode, FSR = V_A								
ENOB	Effective Number of Bits	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		8.9	**8.1**		bits	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**7.8**		bits	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		8.9	**8**		bits	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**7.7**		bits	6
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		55.3	**50.3**		dB	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**48.5**		dB	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		55.3	**49.8**		dB	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**48.0**		dB	6
SNR	Signal-to-Noise Ratio	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		55.6	**50.9**		dBc	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**49.0**		dBc	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		55.9	**50.5**		dBc	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**48.5**		dBc	6
THD	Total Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		-67.0		**-59.5**	dBc	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}				**-58.5**	dBc	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		-64.3		**-58.5**	dBc	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}				**-58.0**	dBc	6
2nd Harm	Second Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS		–75			dBc	
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		–68			dBc	
3rd Harm	Third Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS		–72			dBc	
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		–68			dBc	

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
SFDR	Spurious-Free Dynamic Range	f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		66.7	**57.5**		dBc	4, 5
		f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**53.0**		dBc	6
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = 25°C to T_{MAX}		66.7	**57.5**		dBc	4, 5
		f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS, T_A = T_{MIN}			**54.5**		dBc	6
Non-Demux Non-DES Mode, Non-Extended Control Mode, FSR = V_A								
ENOB	Effective Number of Bits	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		9.0			bits (min)	
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		56.2			dB (min)	
SNR	Signal-to-Noise Ratio	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		56.7			dBc (min)	
THD	Total Harmonic Distortion	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		-65.7			dBc (max)	
2nd Harm	Second Harmonic Distortion	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		–75			dBc	
3rd Harm	Third Harmonic Distortion	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		–68			dBc	
SFDR	Spurious-Free Dynamic Range	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		67.6			dBc (min)	
1:4 Demux DES Mode (Q-channel only), ECM, Offset/Gain Adjusted								
ENOB	Effective Number of Bits	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		8.7			bits (min)	
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		54.2			dB (min)	
SNR	Signal-to-Noise Ratio	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		55.3			dBc (min)	
THD	Total Harmonic Distortion	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		60.7			dBc (max)	
2nd Harm	Second Harmonic Distortion	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		–78			dBc	
3rd Harm	Third Harmonic Distortion	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		–67			dBc	
SFDR	Spurious-Free Dynamic Range	f_{IN} = 498 MHz, V_{IN} = -0.5 dBFS		63.6			dBc (min)	

TABLE 7. Analog Input/Output and Reference Characteristics

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
V_{IN_FSR}	Analog Differential Input Full Scale Range	FSR Pin Y3 Low		630	**560**		mV_{P-P}	4, 5, 6
						680	mV_{P-P}	4, 5, 6
		FSR Pin Y3 High		820	**750**		mV_{P-P}	4, 5, 6
						890	mV_{P-P}	4, 5, 6
		Extended Control Mode						
		FM(14:0) = 0000**h**		600			mV_{P-P}	
		FM(14:0) = 4000**h** (default)		790			mV_{P-P}	
		FM(14:0) = 7FFF**h**		980			mV_{P-P}	
C_{IN}	Analog Input Capacitance, Non-DES Mode	Differential	(*Note 9*, *Note 10*)	0.02			pF	
		Each input pin to ground		1.6			pF	
	Analog Input Capacitance, DES Mode	Differential	(*Note 9*, *Note 10*)	0.08			pF	
		Each input pin to ground		2.2			pF	
R_{IN}	Differential Input Resistance			103.5	**100**		Ω	1, 2, 3
						108	Ω	1, 2, 3
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA		1.25	**1.15**		V	1, 2, 3
						1.35	V	1, 2, 3
TC_V_{BG}	Bandgap Reference Voltage Temperature Coefficient	I_{BG} = ±100µA		50			ppm/°C	
C_{LOAD} V_{BG}	Maximum Bandgap Reference Load Capacitance			80			pF	

TABLE 8. Channel-to-Channel Characteristics

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
	Offset Match			2			LSB	
	Positive Full-Scale Match	Zero offset selected in Control Register		2			LSB	
	Negative Full-Scale Match	Zero offset selected in Control Register		2			LSB	
	Phase Matching (I, Q)	f_{IN} = 1.0 GHz		< 1			Degree	
X-TALK Q-channel	Crosstalk from I-channel (Aggressor) to Q-channel (Victim)	Aggressor = 498 MHz F.S. Victim = 100 MHz F.S.		–61			dB	
X-TALK I-channel	Crosstalk from Q-channel (Aggressor) to I-channel (Victim)	Aggressor = 498 MHz F.S. Victim = 100 MHz F.S.		–61			dB	

TABLE 9. LVDS CLK Input Characteristics

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
V_{IN_CLK}	Differential Clock Input Level	Sine Wave Clock		0.6	**0.4**		V_{P-P}	1, 2, 3
						2.0	V_{P-P}	1, 2, 3
		Square Wave Clock		0.6	**0.4**		V_{P-P}	1, 2, 3
						2.0	V_{P-P}	1, 2, 3
C_{IN_CLK}	Sampling Clock Input Capacitance	Differential	(*Note 9*, *Note 10*)	0.1			pF	
		Each input to ground		1			pF	
R_{IN_CLK}	Sampling Clock Input Resistance			100			Ω	

TABLE 10. Digital Control and Output Pin Characteristics

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
Digital Control Pins, (Cal, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$)								
V_{IH}	Logic High Input Voltage	DES, CalDly, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$			**0.7 x V_A**		V	1, 2, 3
V_{IL}	Logic Low Input Voltage	DES, CalDly, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$				**0.3 x V_A**	V	1, 2, 3
I_T	Input Current	V_{IN} = GND, V_{IN} = V_A		±1			µA	
C_{IN_DIG}	Input Capacitance	Each input to ground	(*Note 10*, *Note 11*)	1.5			pF	
Digital Output Pins (Data, DCLKI, DCLKQ, ORI, ORQ)								
V_{OD}	LVDS Differential Output Voltage	V_{BG} = Floating, OVS = V_A		520	**300**		mV_{P-P}	1, 2, 3
						700	mV_{P-P}	1, 2, 3
		V_{BG} = Floating, OVS = GND		374	**160**		mV_{P-P}	1, 2, 3
						560	mV_{P-P}	1, 2, 3
		V_{BG} = V_A, OVS = V_A		568	**340**		mV_{P-P}	1, 2, 3
						760	mV_{P-P}	1, 2, 3
		V_{BG} = V_A, OVS = GND		400	**190**		mV_{P-P}	1, 2, 3
						600	mV_{P-P}	1, 2, 3
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels			±1			mV	
V_{OS}	Output Offset Voltage	V_{BG} = Floating		0.8			V	
		V_{BG} = V_A		1.2			V	
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels			±1			mV	
I_{OS}	Output Short Circuit Current	V_{BG} = Floating; D+ and D– connected to 0.8V		±3.8			mA	
Z_O	Differential Output Impedance			100			Ω	
V_{OH}	Logic High Output Level	CalRun, SDO I_{OH} = –400 µA	(*Note 10*)	1.65	**1.5**		V	1, 2, 3

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
V_{OL}	Logic Low Output Level	CalRun, SDO I_{OH} = 400 µA	(*Note 10*)	0.15		**0.3**	V	1, 2, 3
Differential DCLK Reset Pins (DCLK_RST)								
V_{CMI_DRST}	DCLK_RST Common Mode Input Voltage			1.25 ±0.15			V	
V_{ID_DRST}	Differential DCLK_RST Input Voltage			0.6			VP-P	
R_{IN_DRST}	Differential DCLK_RST Input Resistance		(*Note 10*)	100			Ω	

TABLE 11. Power Supply Characteristics (1:2 Demux Mode)

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
I_A	Analog Supply Current	PDI = PDQ = Low		890		**951**	mA	1, 2, 3
		PDI = Low; PDQ = High		505		**551**	mA	1, 2, 3
		PDI = High; PDQ = Low		505		**551**	mA	1, 2, 3
		PDI = PDQ = High		2			mA	
I_{TC}	Track-and-Hold and Clock Supply Current	PDI = PDQ = Low		358		**376**	mA	1, 2, 3
		PDI = Low; PDQ = High		220		**241**	mA	1, 2, 3
		PDI = High; PDQ = Low		220		**241**	mA	1, 2, 3
		PDI = PDQ = High		1			mA	
I_{DR}	Output Driver Supply Current	PDI = PDQ = Low		210		**271**	mA	1, 2, 3
		PDI = Low; PDQ = High		111		**141**	mA	1, 2, 3
		PDI = High; PDQ = Low		111		**141**	mA	1, 2, 3
		PDI = PDQ = High		10			µA	
I_E	Digital Encoder Supply Current	PDI = PDQ = Low		60		**101**	mA	1, 2, 3
		PDI = Low; PDQ = High		30.5		**56**	mA	1, 2, 3
		PDI = High; PDQ = Low		30.5		**56**	mA	1, 2, 3
		PDI = PDQ = High		10			µA	
P_C	Power Consumption	PDI = PDQ = Low		2.9		**3.22**	W	1, 2, 3
		PDI = Low; PDQ = High		1.64		**1.88**	W	1, 2, 3
		PDI = High; PDQ = Low		1.64		**1.88**	W	1, 2, 3
		PDI = PDQ = High		6			mW	

TABLE 12. AC Electrical Characteristics

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
Input Clock (CLK)								
$f_{CLK\ (max)}$	Maximum Input Clock Frequency					**1.0**	GHz	9, 10, 11
$f_{CLK\ (min)}$	Minimum Input Clock Frequency	Non-DES Mode			**200**		MHz	9, 10, 11
		DES Mode		250			MHz	9, 10, 11
	Input Clock Duty Cycle	$f_{CLK(min)} \leq f_{CLK} \leq f_{CLK}$ (max)		50	**20**		%	
						80	%	
t_{CL}	Input Clock Low Time			500	**200**		ps (min)	
t_{CH}	Input Clock High Time			500	**200**		ps (min)	
	DCLK Duty Cycle			50			% (min)	
							% (max)	
Data Clock (DCLKI, DCLKQ)								
t_{SR}	Setup Time DCLK_RST±			45			ps	
t_{HR}	Hold Time DCLK_RST±			45			ps	
t_{PWR}	Pulse Width DCLK_RST±			5			Input Clock Cycles (min)	
t_{SYNC_DLY}	DCLK Synchronization Delay	90° Mode		4			Input Clock Cycles	
		0° Mode		5				
t_{LHT}	Differential Low-to-High Transition Time	10% to 90%, C_L = 2.5 pF		220			ps	
t_{HLT}	Differential High-to-Low Transition Time	10% to 90%, C_L = 2.5 pF		220			ps	
t_{SU}	Data-to-DCLK Set-Up Time	DDR Mode, 90° DCLK		850			ps	
t_H	DCLK-to-Data Hold Time	DDR Mode, 90° DCLK		850			ps	
t_{OSK}	DCLK-to-Data Output Skew	50% of DCLK Transition to 50% of Data Transition		±75			ps	

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
Data Input to Output								
t_{AD}	Sampling (Aperture) Delay	Input CLK+ Fall to Acquisition of Data		1.1			ns	
t_{AJ}	Aperture Jitter			0.2			ps (rms)	
t_{OD}	Input Clock-to Data Output Delay (in addition to t_{LAT})	50% of Input Clock transition to 50% of Data transition		2.4			ns	
t_{LAT}	Latency in 1:2 Demux Non-DES Mode	DI, DQ Outputs	(*Note 10*)			**34**	Input Clock Cycles	4, 5, 6
		DId, DQd Outputs				**35**		4, 5, 6
	Latency in 1:4 Demux DES Mode	DI Outputs	(*Note 10*)			**34**	Input Clock Cycles	4, 5, 6
		DQ Outputs				**34.5**		4, 5, 6
		DId Outputs				**35**		4, 5, 6
		DQd Outputs				**35.5**		4, 5, 6
	Latency in Non-Demux Non-DES Mode	DI Outputs	(*Note 10*)			**34**	Input Clock Cycles	4, 5, 6
		DQ Outputs				**34**		4, 5, 6
	Latency in Non-Demux DES Mode	DI Outputs	(*Note 10*)			**34**	Input Clock Cycles	4, 5, 6
		DQ Outputs				**34.5**		4, 5, 6
t_{ORR}	Over Range Recovery Time	Differential V_{IN} step from ±1.2V to 0V to get accurate conversion		1			Input Clock Cycle	
t_{WU}	PD Low to Rated Accuracy Conversion (Wake-Up Time)	Non-DES Mode		500			ns	
		DES Mode		1			µs	
Serial Port Interface								
f_{SCLK}	Serial Clock Frequency			15			MHz	
	Serial Clock Low Time				**30**		ns	9, 10, 11
	Serial Clock High Time				**30**		ns	9, 10, 11
t_{SSU}	Serial Data to Serial Clock Rising Setup Time			2.5			ns (min)	
t_{SH}	Serial Data to Serial Clock Rising Hold Time			1			ns (min)	
t_{SCS}	$\overline{SCS}$ to Serial Clock Rising Setup Time			2.5			ns	
t_{HCS}	$\overline{SCS}$ to Serial Clock Falling Hold Time			1.5			ns	
t_{BSU}	Bus Turn-around Time			10			ns	

Symbol	Parameter	Conditions	Notes	Typical	Min	Max	Units	Sub-groups
Calibration								
t_{CAL}	Calibration Cycle Time	Non-ECM		$2.4x10^7$			Clock Cycles	
		ECM CSS = 0b		$2.3x10^7$				
		ECM; CSS = 1b						
		CMS(1:0) = 00b		$0.8x10^7$			Clock Cycles	
		CMS(1:0) = 01b		$1.5x10^7$				
		CMS(1:0) = 10b (ECM default)		$2.4x10^7$				
t_{CAL_L}	CAL Pin Low Time	See *Figure 10*	(*Note 10*)		**1280**		Clock Cycles	9, 10, 11
t_{CAL_H}	CAL Pin High Time	See *Figure 10*	(*Note 10*)		**1280**		Clock Cycles	9, 10, 11

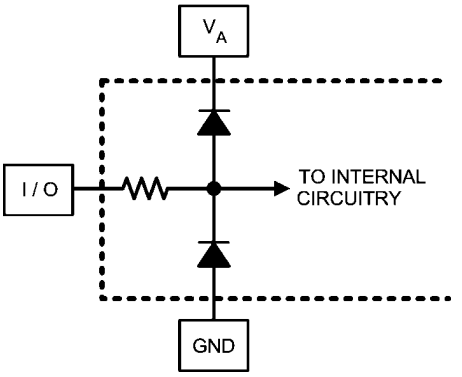
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no guarantee of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = GND_{DR} = GND_E = GND_{TC} = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supply limit; (i.e. less than GND or greater than V_A), the current at that pin should be limited to 50 mA. In addition, over voltage at a pin must adhere to maximum voltage limits. Simultaneously over voltage at multiple pins require adherence to the maximum package power dissipation limits.

Note 4: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms. Charged device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Note 5: The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



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Note 6: To guarantee accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.

Note 7: Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See *Figure 4*. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

Note 9: The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.22 pF differential and 1.06 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 10: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 11: The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 12: The maximum clock frequency for Non-Demux Mode is 1 GHz.

Note 13: Pre and post irradiation limits are identical to those listed in the “DC ” and “AC" Parameters Electrical Characteristics, except that they are tested at Room Temperature.

13.0 Specification Definitions

APERTURE (SAMPLING) DELAY is the amount of delay, measured from the sampling edge of the CLK input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample-to-sample. Aperture jitter can be effectively considered as noise at the input.

CODE ERROR RATE (C.E.R.) is the probability of error and is defined as the probable number of word errors on the ADC output per unit of time divided by the number of words seen in that amount of time. A C.E.R. of 10^{-18} corresponds to a statistical error in one word about every four (4) years.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. It is measured at sample rate = 500 MSPS with a 1MHz input sine wave.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and states that the converter is equivalent to a perfect ADC of this many (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops to 3 dB below its low frequency value for a full-scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors. The Positive Gain Error is the Offset Error minus the Positive Full-Scale Error. The Negative Gain Error is the Negative Full-Scale Error minus the Offset Error. The Gain Error is the Negative Full-Scale Error minus the Positive Full-Scale Error; it is also equal to the Positive Gain Error plus the Negative Gain Error.

INTEGRAL NON-LINEARITY (INL) is a measure of worst case deviation of the ADC transfer function from an ideal straight line drawn through the ADC transfer function. The deviation of any given code from this straight line is measured from the center of that code value step. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^N$$

where V_{FS} is the differential full-scale amplitude V_{IN} as set by the FSR input and "N" is the ADC resolution in bits, which is 10 for the ADC10D1000.

LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) DIFFERENTIAL OUTPUT VOLTAGE (V_{ID} and V_{OD}) is two times the absolute value of the difference between the V_D+ and V_D - signals; each measured with respect to Ground.

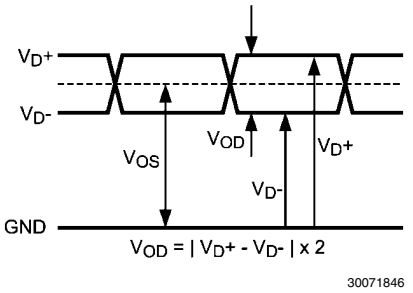


FIGURE 3. LVDS Output Signal Levels

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D- pins output voltage with respect to ground; i.e., [(V_D+) +(V_D-)]/2. See *Figure 3*.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential $-V_{IN}/2$ with the FSR pin low. For the ADC10D1000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

NOISE POWER RATIO (NPR) is the ratio of the sum of the power inside the notched bins to the sum of the power in an equal number of bins outside the notch, expressed in dB.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 511.5.

OUTPUT DELAY (t_{OD}) is the time delay (in addition to Pipeline Delay) after the falling edge of CLK+ before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of input clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential $+V_{IN}/2$. For the ADC10D1000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) PSRR1 (D.C. PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding DC.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding DC.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

14.0 Transfer Characteristic

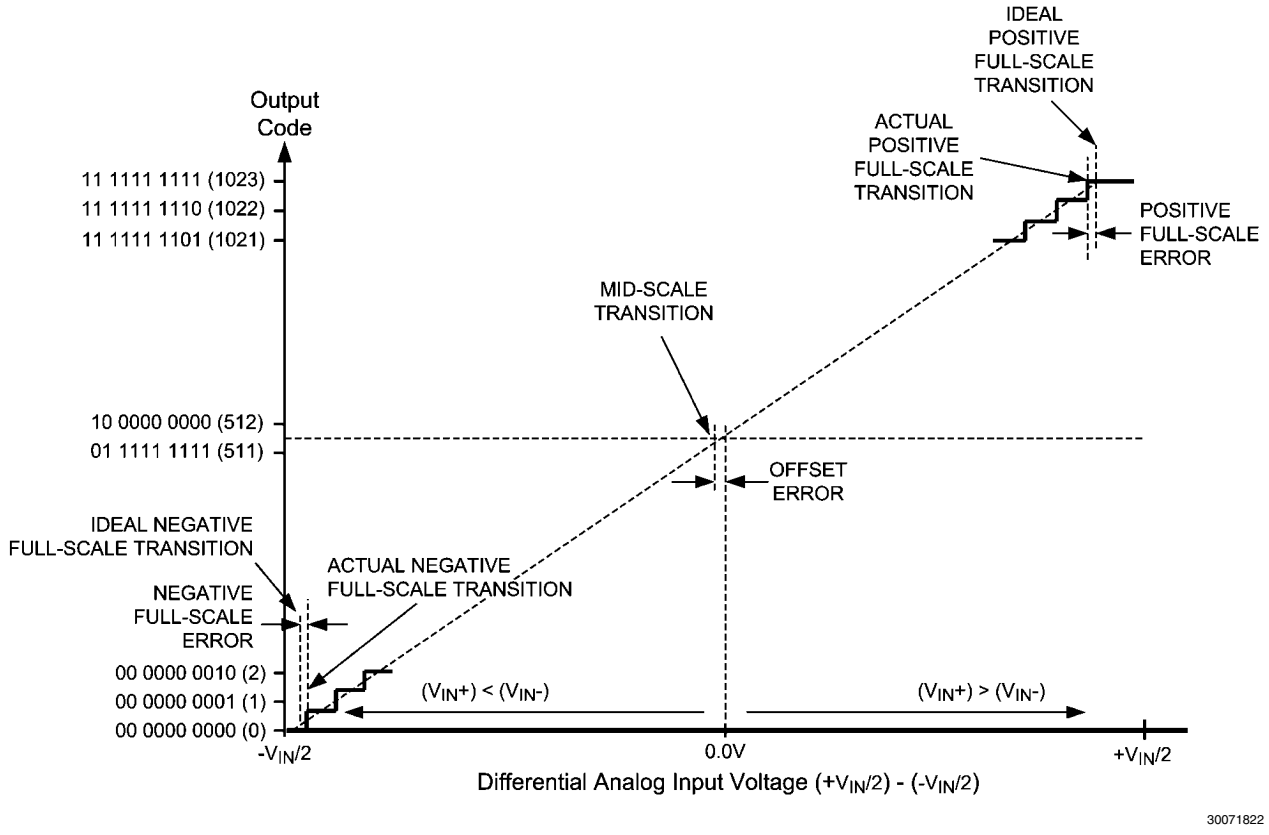


FIGURE 4. Input / Output Transfer Characteristic

15.0 Timing Diagrams

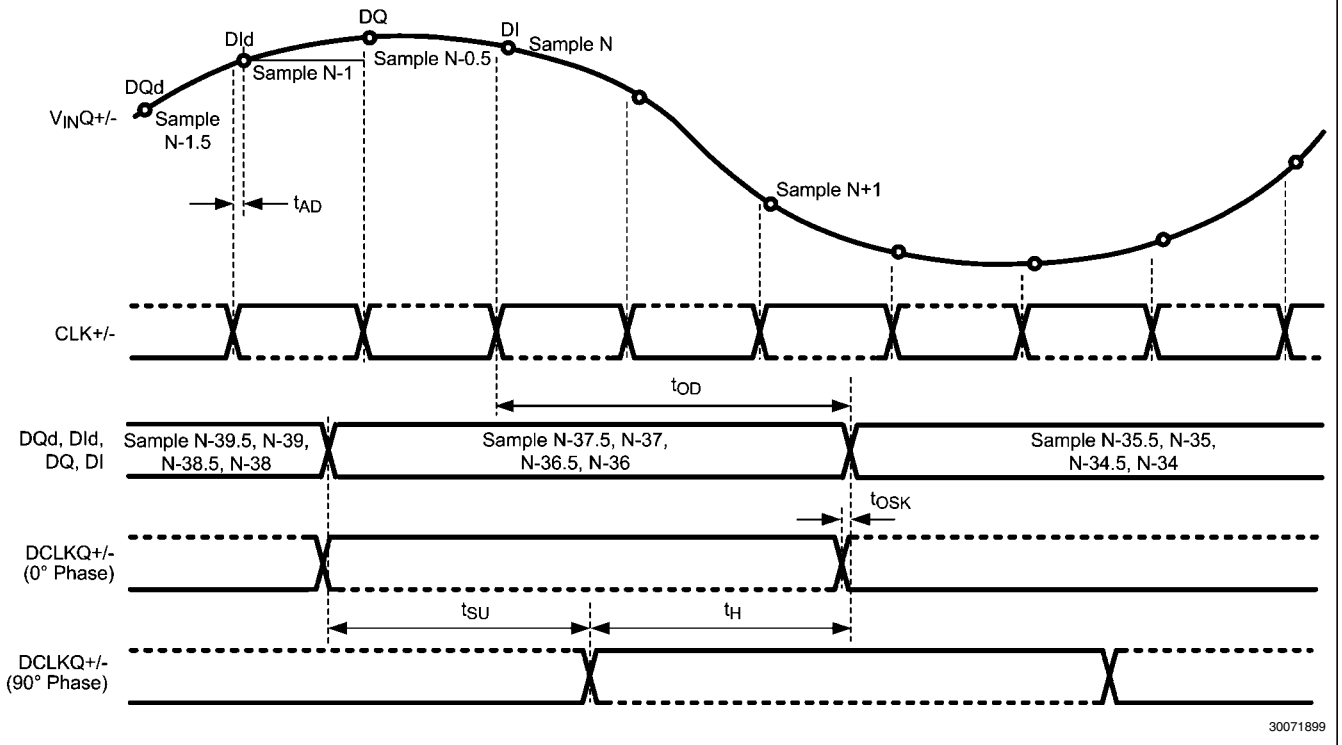


FIGURE 5. Clocking in 1:4 Demux DES Mode

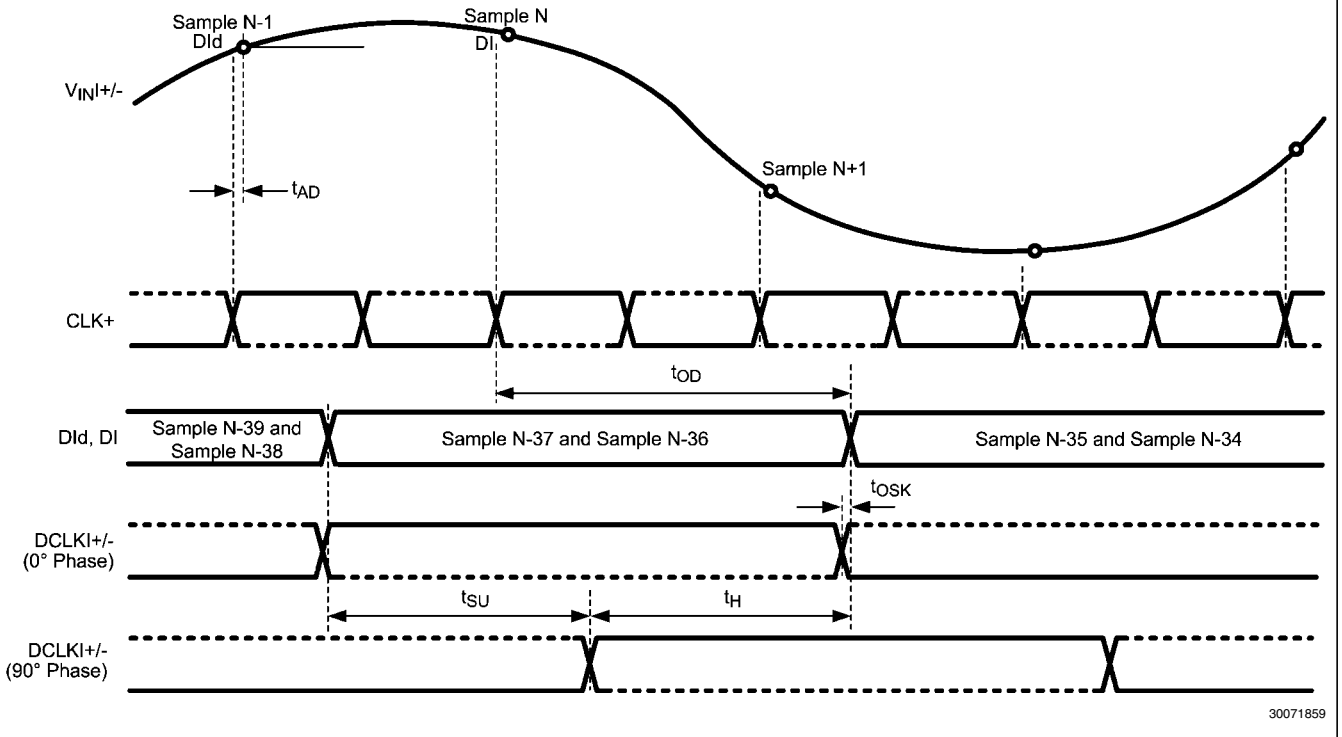


FIGURE 6. Clocking in 1:2 Demux Non-DES Mode*

* The timing here is shown for the I-channel only. However, the Q-channel functions precisely the same as the I-channel, with VinQ+/-, DCLKQ+/-, DQd and DQ instead of VinI+/-, DCLKI+/-, DId and DI. Both I- and Q-channel use the same CLK+/-.

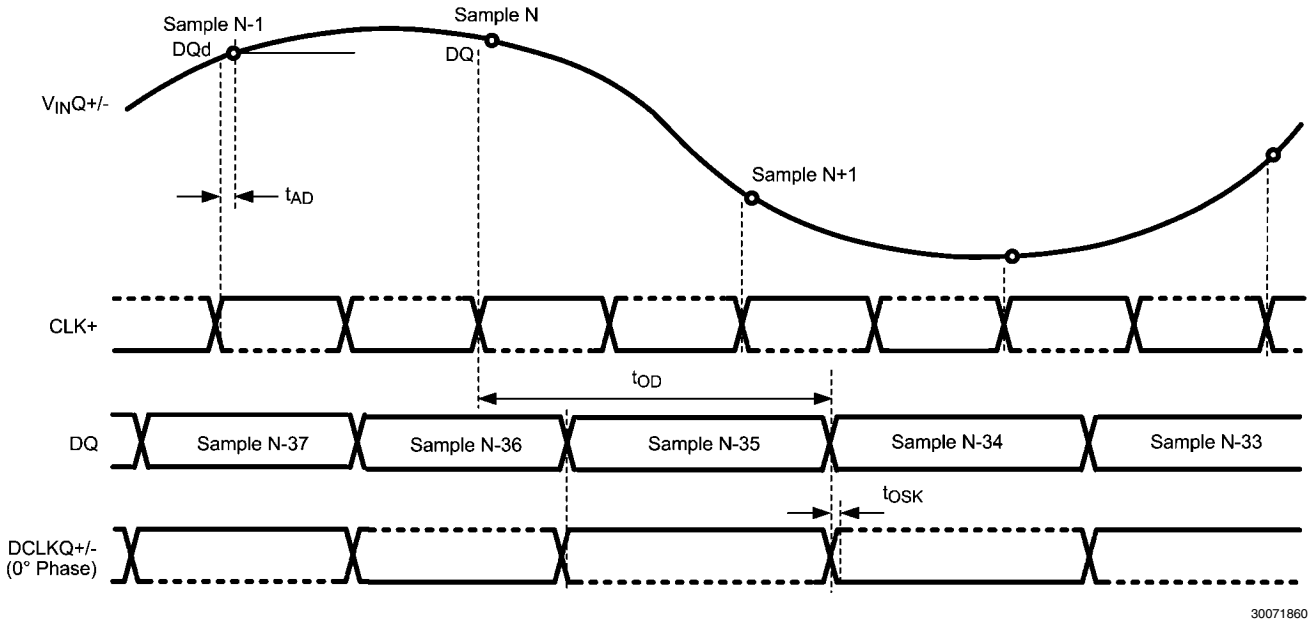


FIGURE 7. Clocking in Non-Demux Mode Non-DES Mode**

** The timing here is shown for the Q-channel only. However, for the Non-Demux Non-DES Mode, both I- and Q-channels may be used as input. For this case, the I-channel functions precisely the same as the Q-channel, with VinI+/-, DCLKI+/-, and DI instead of VinQ+/-, DCLKQ+/-, and DQ. Both I- and Q-channel use the same CLK+/-.

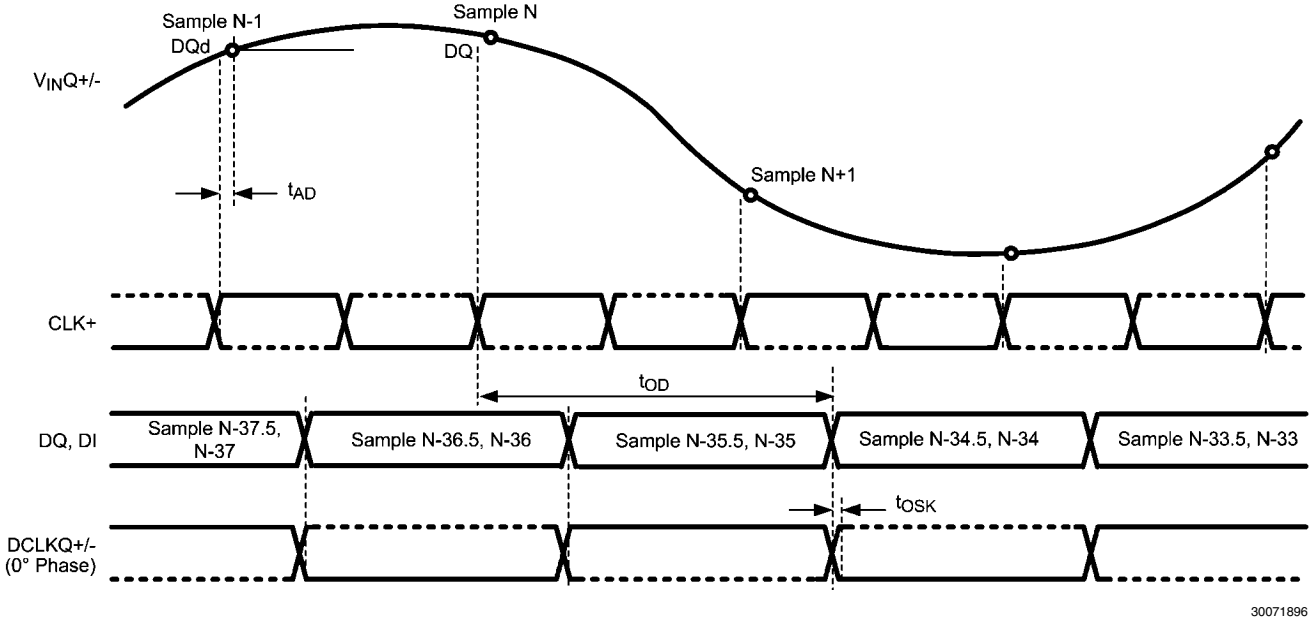


FIGURE 8. Clocking in Non-Demux Mode DES Mode

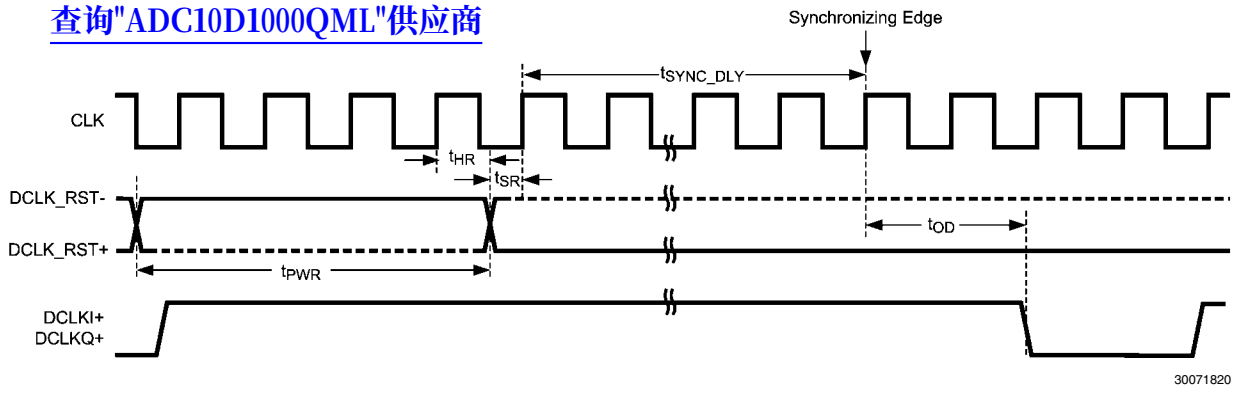


FIGURE 9. Data Clock Reset Timing

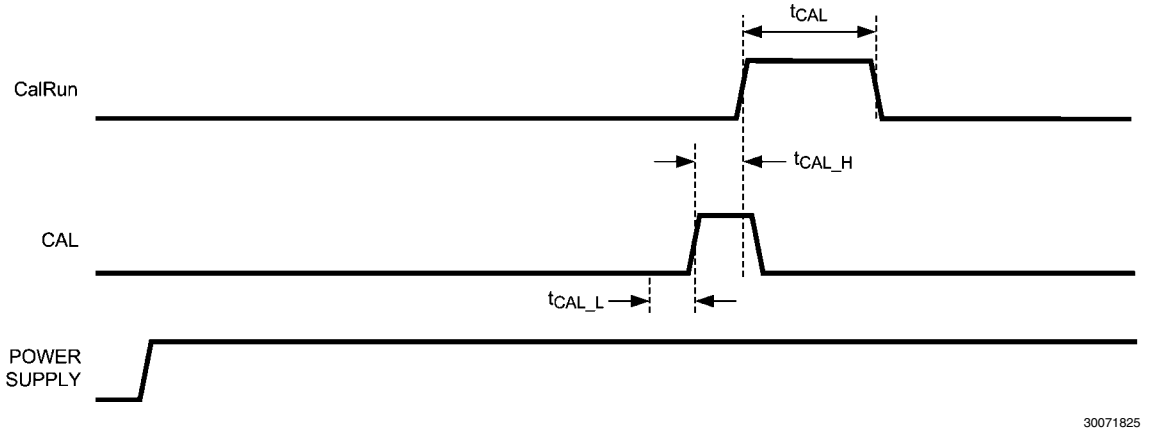


FIGURE 10. On-Command Calibration Timing

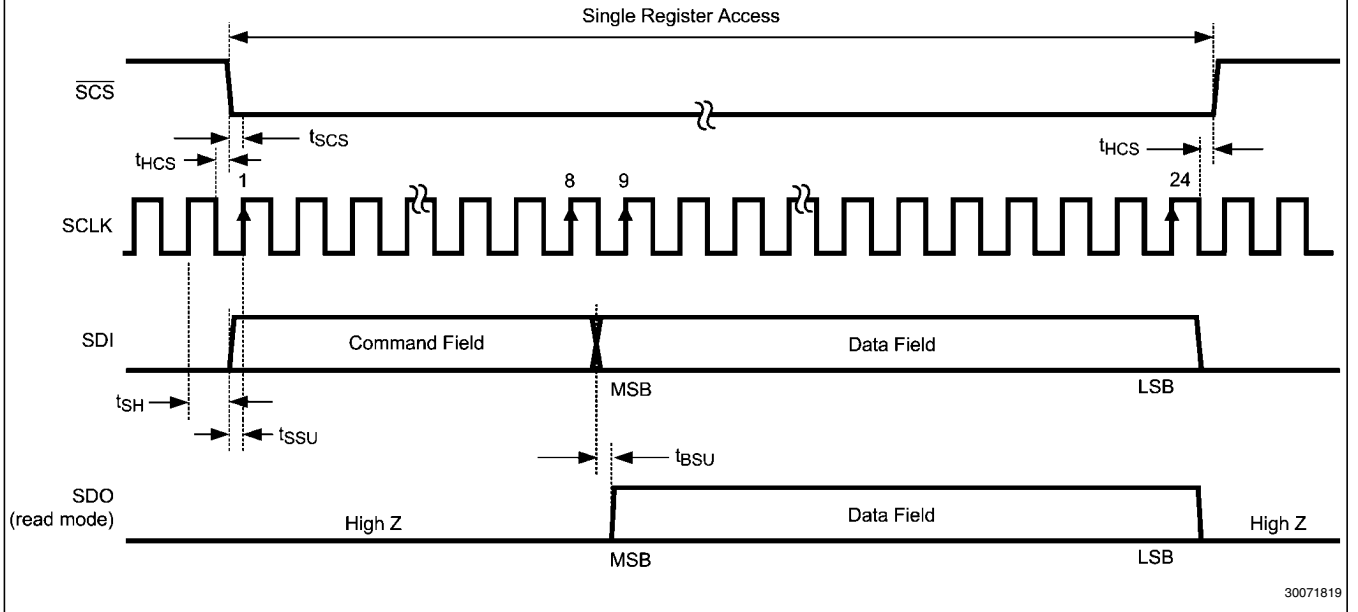
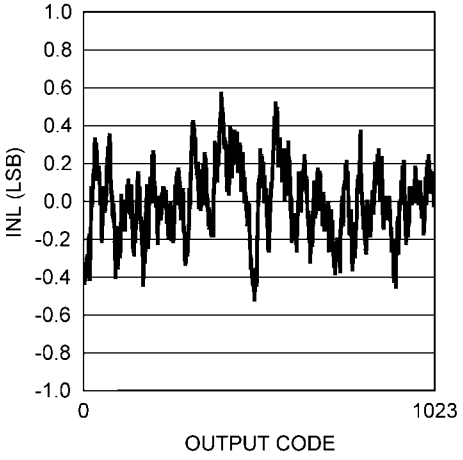


FIGURE 11. Serial Interface Timing

16.0 Typical Performance Plots

$V_A = V_{DR} = V_{TC} = V_E = 1.9V$, $f_{CLK} = 1000$ MHz, $f_{IN} = 498$ MHz, $T_A = 25°C$, I-channel and Q-channel, unused channel terminated to AC ground and 1:2 Demux Non-DES Mode (1:1 Demux Mode has similar performance), unless otherwise stated. NPR plots Notch $f_C = 325$ MHz and Notch width = 25 MHz.

INL vs. CODE



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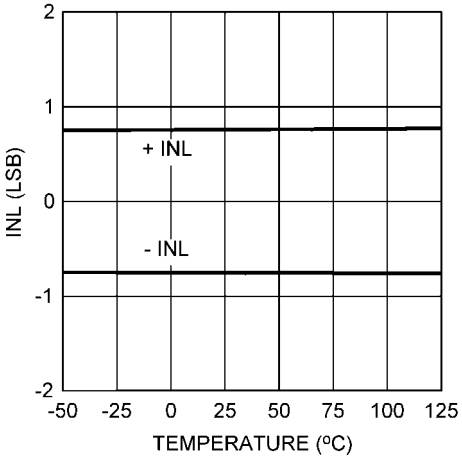
INL vs. TEMPERATURE



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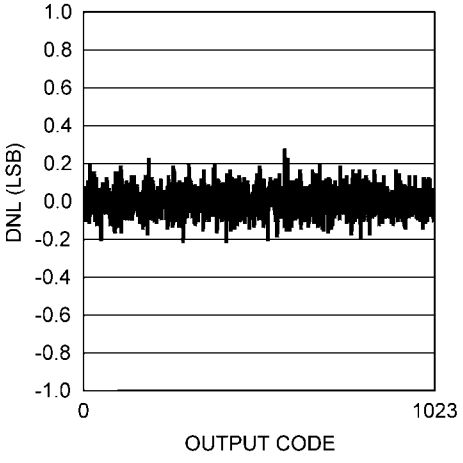
DNL vs. CODE



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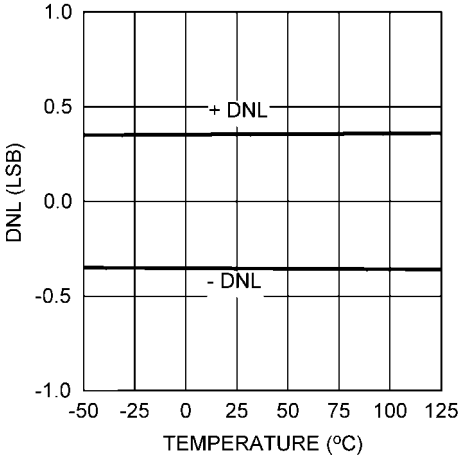
DNL vs. TEMPERATURE



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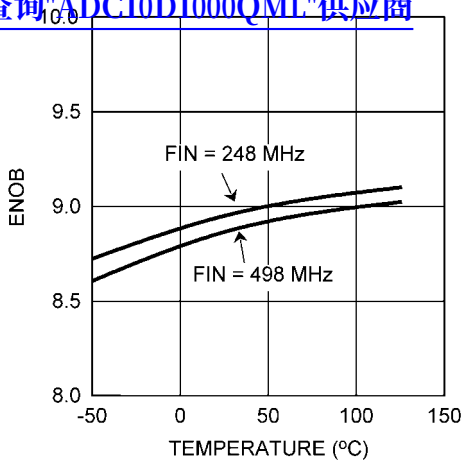
ENOB vs. TEMPERATURE



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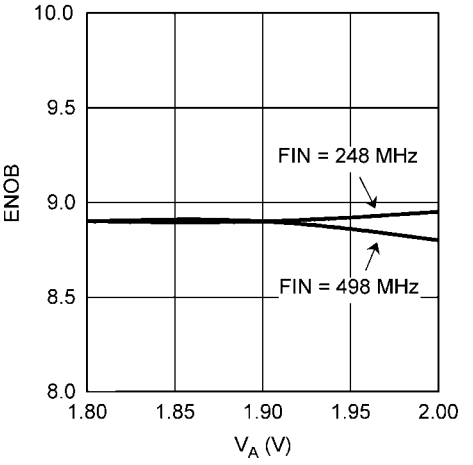
ENOB vs. SUPPLY VOLTAGE



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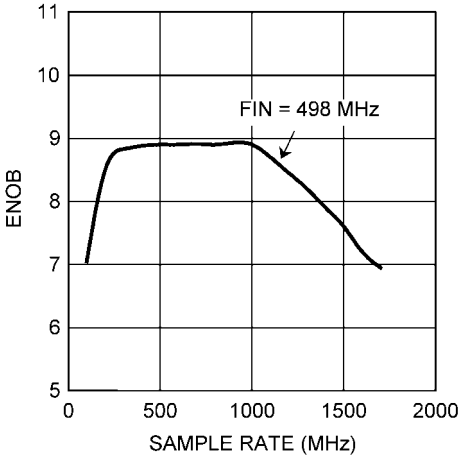
ENOB vs. CLOCK FREQUENCY



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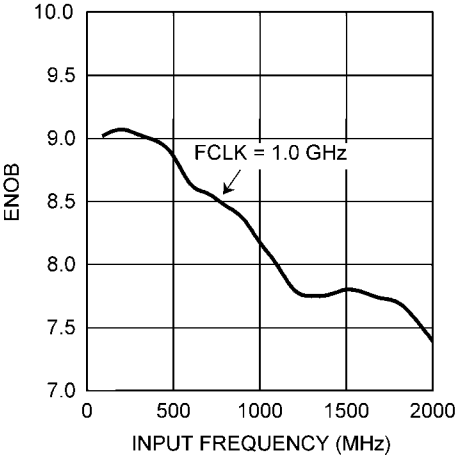
ENOB vs. INPUT FREQUENCY



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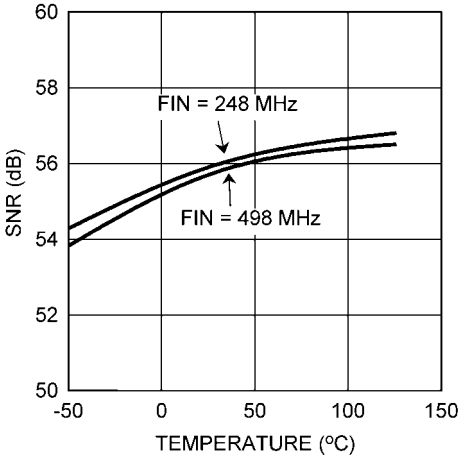
SNR vs. TEMPERATURE



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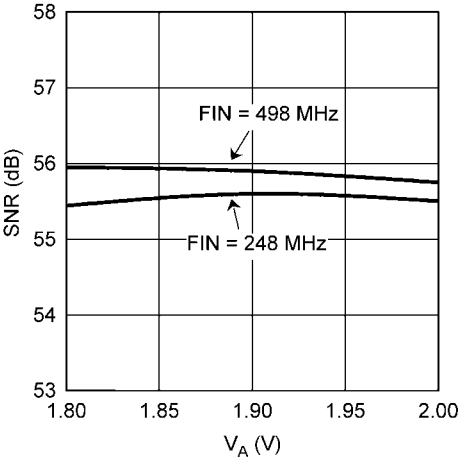
SNR vs. SUPPLY VOLTAGE



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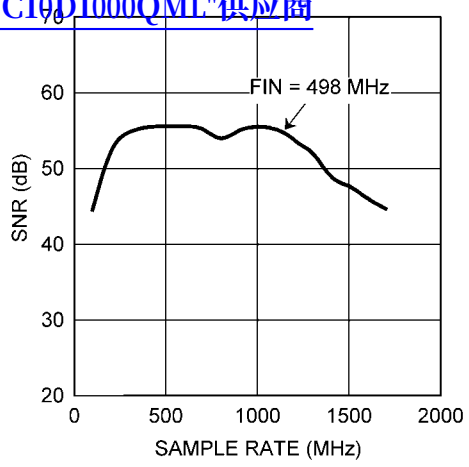
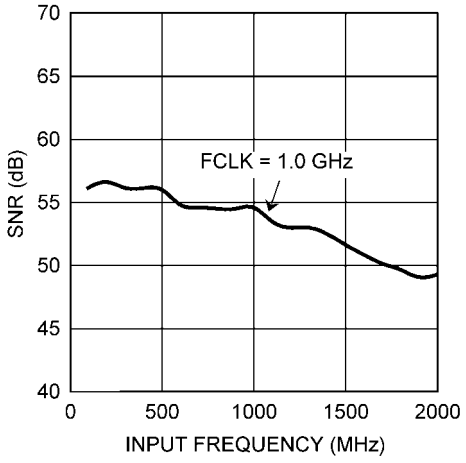
SNR vs. CLOCK FREQUENCY



30071871

SNR vs. INPUT FREQUENCY



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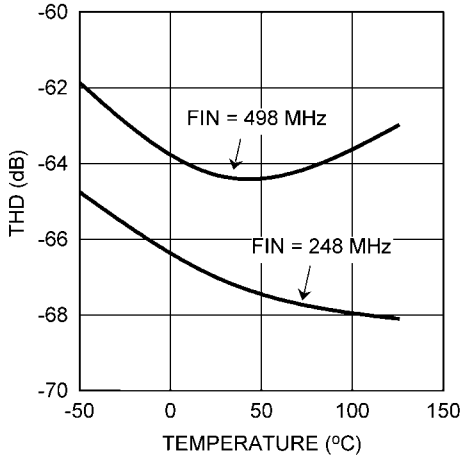
THD vs. TEMPERATURE



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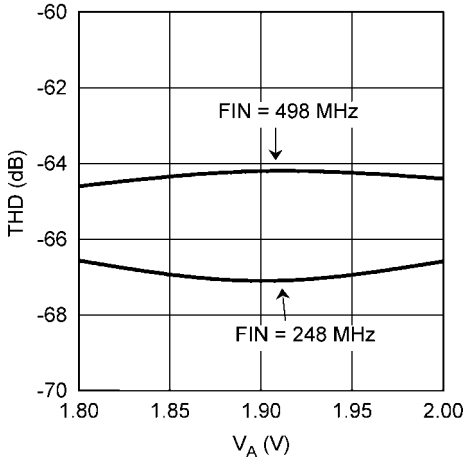
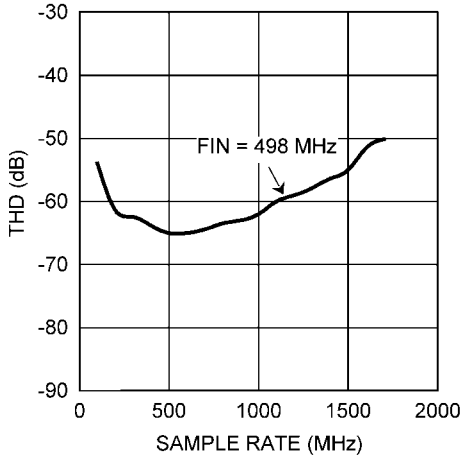
THD vs. SUPPLY VOLTAGE



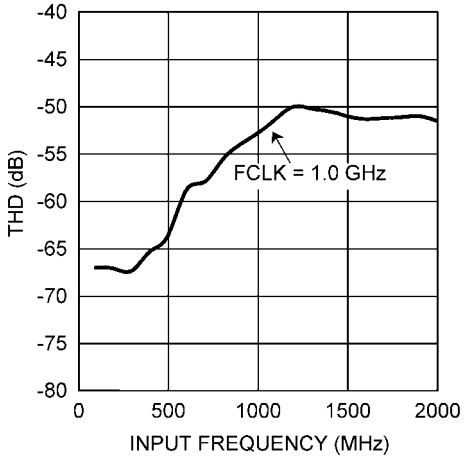
30071874

THD vs. CLOCK FREQUENCY



30071875

THD vs. INPUT FREQUENCY



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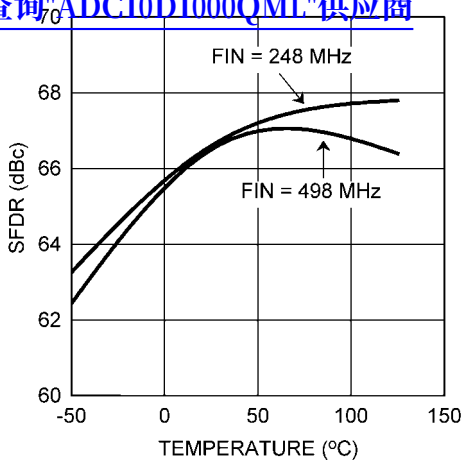
SFDR vs. TEMPERATURE



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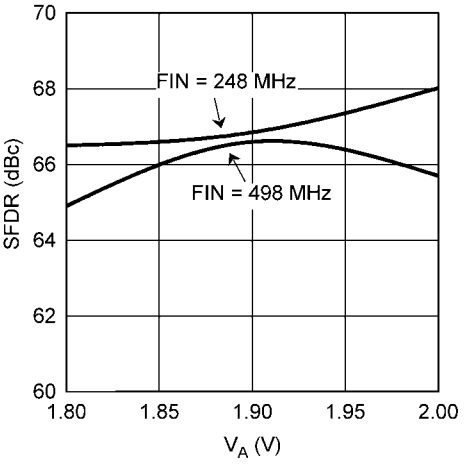
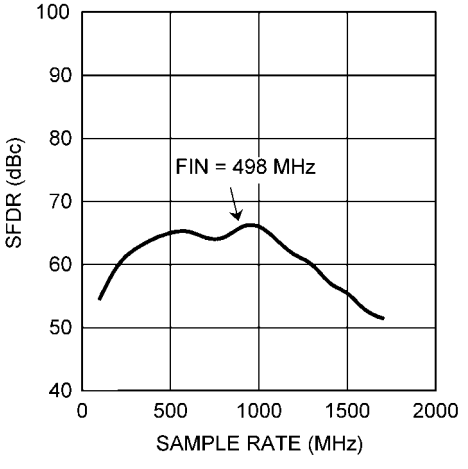
SFDR vs. SUPPLY VOLTAGE



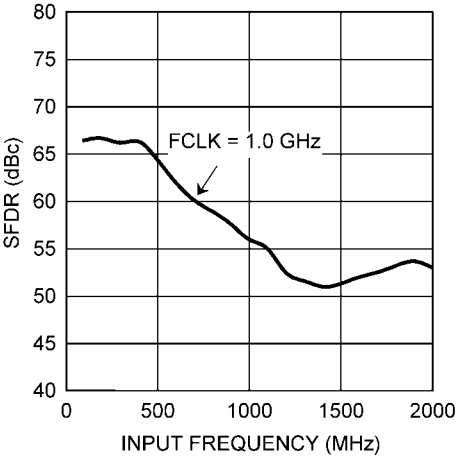
30071878

SFDR vs. CLOCK FREQUENCY



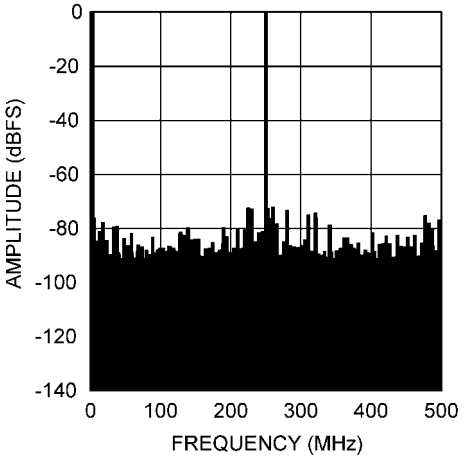
30071879

SFDR vs. INPUT FREQUENCY



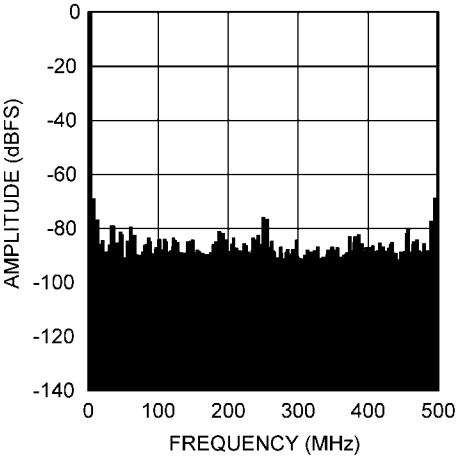
30071880

SPECTRAL RESPONSE AT FIN = 248 MHz



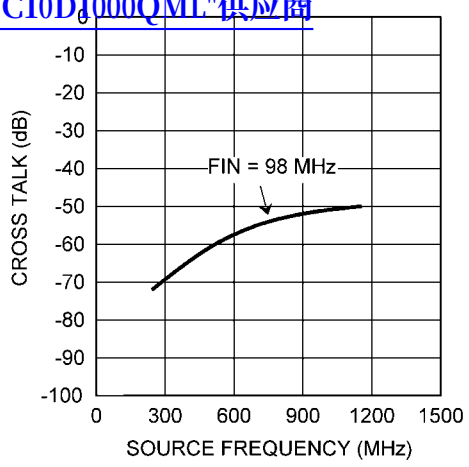
30071881

SPECTRAL RESPONSE AT FIN = 498 MHz



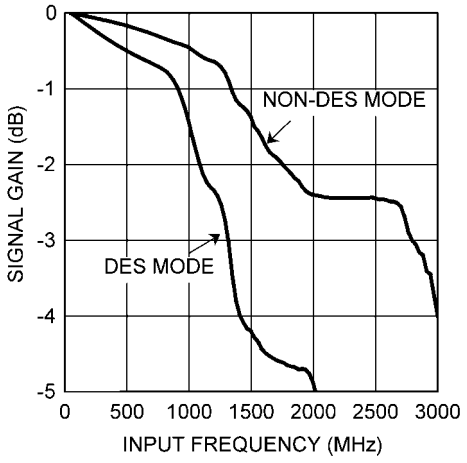
30071882

CROSSTALK vs. SOURCE FREQUENCY



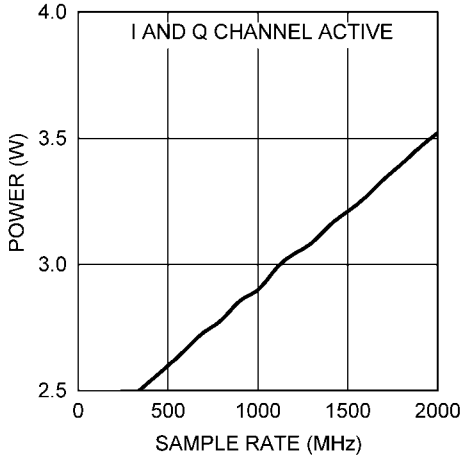
30071883

FULL POWER BANDWIDTH



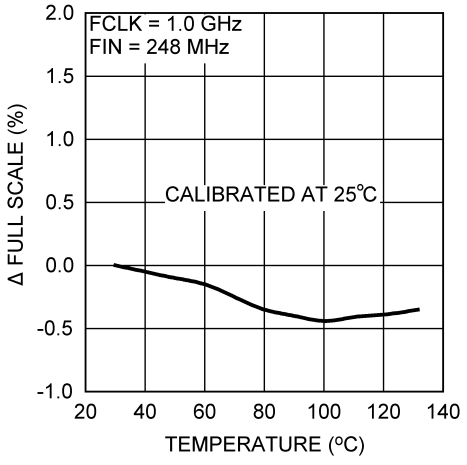
30071884

POWER CONSUMPTION vs. CLOCK FREQUENCY



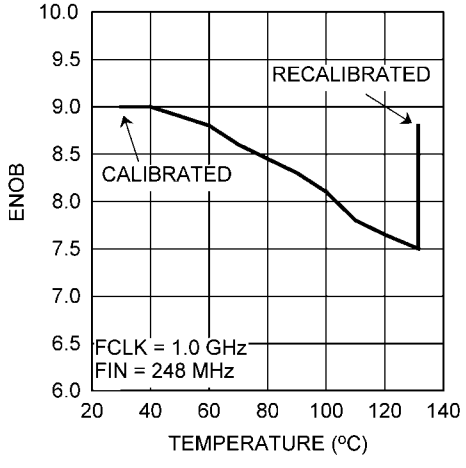
30071885

GAIN vs. TEMPERATURE FS PERCENT CHANGE



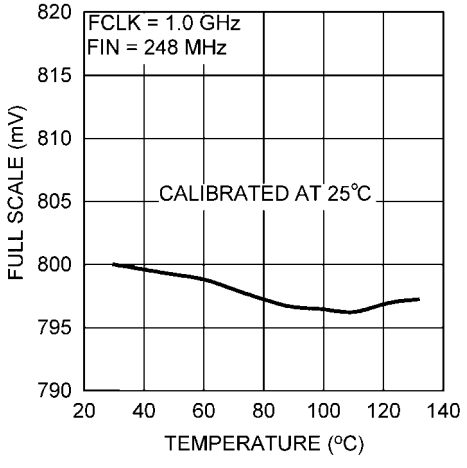
30071886

GAIN vs. TEMPERATURE ENOB



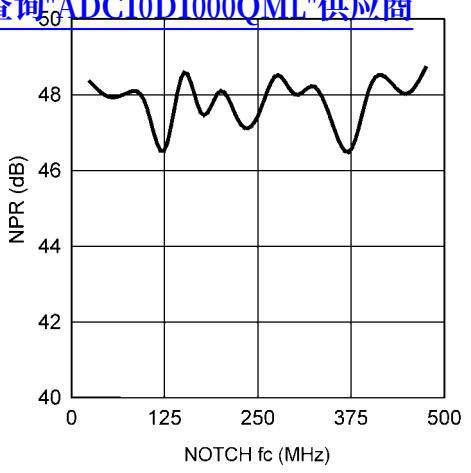
30071887

GAIN vs. TEMPERATURE FS



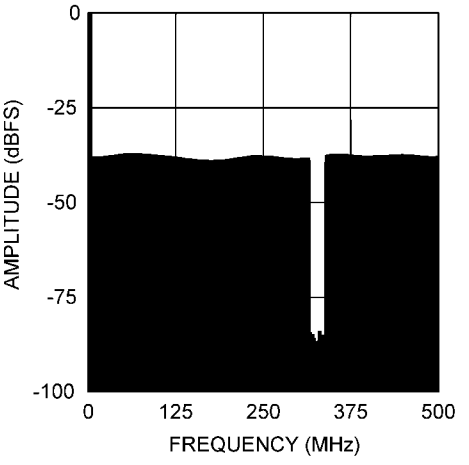
30071888

NPR vs. f_C NOTCH



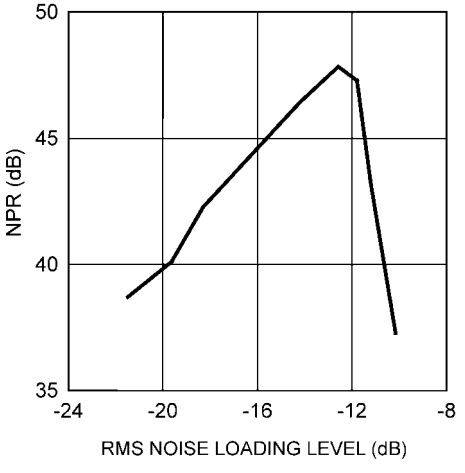
30071889

AMPLITUDE vs. FREQUENCY



30071890

NPR vs. RMS NOISE LOADING LEVEL



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17.0 Functional Description

The ADC10D1000 is a versatile A/D converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section. This section covers an overview and the control modes; Extended Control Mode (ECM) and Non Extended Control Mode (Non-ECM).

17.1 OVERVIEW

The ADC10D1000 uses a calibrated folding and interpolating architecture that achieves a high 9.0 Effective Number of Bits (ENOB). The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to correcting other non-idealities, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter. The calibration registers are radiation hard and will not be upset by a heavy ion strike up to 120 MeV-cm²/mg.

The analog input signal that is within the converter's input voltage range is digitized to ten bits at speeds of 200 MHz to 1300 MHz, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at the I- or Q-channel will cause the Out-of-Range I-channel or Q-channel output (ORI or ORQ), respectively, to output a logic-high signal.

The device may be operated in one of two control modes: Extended Control Mode (ECM) or Non-Extended Control Mode (Non-ECM). In Non-ECM, the features of the device may be accessed via simple pin control. In ECM, an expanded feature set is available via the Serial Interface. Important new features include AutoSync for mulit-chip synchronization, programmable 15-bit input full-scale range and independant programmable 12-bit plus sign offset adjustment.

Each channel has a selectable output demultiplexer which feeds two LVDS buses. If the 1:2 Demux Mode is selected, the output data rate is reduced to half the input sample rate on each bus. When Non-Demux Mode is selected, the output data rate on each channel is at the same rate as the input sample clock and only one 10-bit bus per channel is active.

17.2 POWER-ON RESET

The ADC10D1000's power-on reset has been disabled to ensure single effect functional interrupts do not occur during space operation. Therefore, the calibration routine at power-on is not reliable for the space version of the ADC10D1000. This means a manual calibration is always required after the parts is power-on and is stable. Specifically, the part must either be in Non-Extended Control mode or in Extended Control Mode with the configuration registers reset or written to the correct values, and then a manual calibration must be run before the ADC can be used to digitize data correctly. See section *Section 17.4.3 Calibration Feature* for more information on Calibration.

17.3 CONTROL MODES

The ADC10D1000 may be operated in one of two control modes: Non-extended Control Mode (Non-ECM) or Extended Control Mode (ECM). In the simpler Non-ECM (also sometimes referred to as Pin Control Mode), the user affects available configuration and control of the device through the control pins. The ECM provides additional configuration and control options through a serial interface and a set of 16 registers.

17.3.1 Non-Extended Control Mode

In Non-extended Control Mode (Non-ECM), the Serial Interface is not active and all available functions are controlled via various pin settings. Non-ECM is selected by setting $\overline{ECE}$ (Pin B3) to logic high. Seven dedicated control pins provide a wide range of control for the ADC10D1000 and facilitate its operation. These control pins provide Demux Mode selection, DDR Phase selection, Calibration event initiation, Power Down I-channel, Power Down Q-channel, Test Pattern Mode selection, and Full-Scale input Range selection. In addition to this, a one dual-purpose control pin provides for LVDS output common-mode voltage selection. See *Table 13* for a summary.

TABLE 13. Non-ECM Pin Summary

Pin Name	Logic-Low	Logic-High	Floating
NDM	Demux Mode	Non-demux Mode	Not allowed
DDRPh	0° Mode	90° Mode	Not allowed
CAL	See *Section 17.3.1.3 Calibration Pin (CAL)*		Not allowed
PDI	I-channel active	Power down I-channel	Not allowed
PDQ	Q-channel active	Power down Q-channel	Not allowed
TPM	Non-Test Pattern Mode	Test Pattern Mode	Not allowed
FSR	Lower FS input range	Higher FS input range	Not allowed
V_{BG}*	Not allowed	Higher LVDS common-mode voltage	Lower LVDS common-mode voltage

*Dual purpose pin.

17.3.1.1 Non-Demultiplexed Mode Pin (NDM)

The Non-Demultiplexed Mode (NDM) Pin selects whether the ADC10D1000 is in Demux Mode (logic-low) or Non-Demux Mode (logic-high). In Non-demux Mode, the data from the input is produced at the data-rate at a single 10-bit output bus. In Demux Mode, the data from the input is produced at half the data-rate at twice the number of output buses. For Non-DES Mode, each I- or Q-channel will produce its data on one or two buses for Non-demux or Demux Mode, respectively. For DES Mode, the Q-channel will produce its data on two or four buses for Non-demux or Demux Mode, respectively.

This feature is pin-controlled only and remains active during both Non-ECM and ECM. See *Table 13* for more information.

17.3.1.2 Dual Data Rate Phase Pin (DDRPh)

The Dual Data Rate Phase (DDRPh) Pin selects whether the ADC10D1000 is in 0° Mode (logic-low) or 90° Mode (logic-high). In Dual Data Rate (DDR) Mode, the Data may transition either with the DCLK transition (0° Mode) or halfway between DCLK transitions (90° Mode). The Data is always in DDR Mode on the ADC10D1000. The DDRPh Pin selects 0° Mode or 90° Mode for both the I-channel: DI- and DId-to-DCLKI

phase relationship and for the Q-channel: DQ- and DQd-to-DCLKQ phase relationship.

To use this feature in ECM, use the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14). See *Configuration Register 1* for more information.

17.3.1.3 Calibration Pin (CAL)

The Calibration (CAL) Pin must be used to initiate an on-command calibration event. The effect of calibration is to maximize the dynamic performance. To initiate an on-command calibration via the CAL pin, bring the CAL pin high for a minimum of t_{CAL_H} input clock cycles after it has been low for a minimum of t_{CAL_L} input clock cycles. The CAL pin should be held high when not in use to help insure no undesired calibrating in space environment. In ECM mode this pin remains active and is Logically OR'd with the CAL bit.

To use this feature in ECM, use the CAL bit in the Configuration Register (Addr: 0**h**; Bit: 15). See *Section 17.4.3 Calibration Feature* for more information.

17.3.1.4 Power Down I-channel Pin (PDI)

The Power Down I-channel (PDI) Pin selects whether the I-channel is powered down (logic-high) or active (logic-low). The digital data output pins (both positive and negative) are put into a high impedance state when the I-channel is powered down. Upon return to the active state, the pipeline will contain meaningless information and must be flushed. The supply currents (typicals and limits) are available for the I-channel powered down or active and may be found in *Table 11*. It is recommended that the user thoroughly understand how the PDI feature functions in relationship with the Calibration feature and control them appropriately for his application.

This pin remains active in ECM. In ECM, either this pin or the PDI bit (Addr: 0**h**; Bit: 11) in the Control Register may be used to power-down the I-channel. See *Section 17.4.4 Power Down* Power Down for more information.

17.3.1.5 Power Down Q-channel Pin (PDQ)

The Power Down Q-channel (PDQ) Pin selects whether the Q-channel is powered down (logic-high) or active (logic-low). This pin functions similarly to the PDI pin, except that it applies to the Q-channel. The PDI and PDQ pins function independently of each other to control whether each I- or Q-channel is powered down or active.

This pin remains active in ECM. In ECM, either this pin or the PDQ bit (Addr: 0**h**; Bit: 10) in the Control Register may be used to power-down the I-channe. See *Section 17.4.4 Power Down* for more information.

17.3.1.6 Test Pattern Mode Pin (TPM)

The Test Pattern Mode (TPM) Pin selects whether the output of the ADC10D1000 is a test pattern (logic-high) or the converted input (logic-low). The ADC10D1000 can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In TPM, the ADC is disengaged and a test pattern generator is connected to the outputs, including ORI and ORQ. See *Section 17.4.2.6 Test Pattern Mode* for more information.

17.3.1.7 Full-Scale Input Range Pin (FSR)

The Full-Scale Input Range (FSR) Pin selects whether the full-scale input range for both the I- and Q-channel is higher (logic-high) or lower (logic-low). The input full-scale range is specified as V_{IN} in *Table 7*. In Non-ECM, the full-scale input range for each I- and Q-channel may not be set independently, but it is possible to do so in ECM. In ECM, the full-scale input range may be set with 15-bits of precision; see FS_ADJ in *Table 7*. The device must be calibrated following a change in FSR to obtain optimal performance.

To use this feature in ECM, use the Configuration Register (Addr: 3**h** and B**h**). See *Section 17.4.1 Input Control and Adjust* for more information.

17.3.1.8 LVDS Output Common-mode Pin (V_{BG})

The V_{BG} Pin serves a dual purpose and may either provide the bandgap output voltage or select whether the LVDS output common-mode voltage is higher (logic-high) or lower (floating). The LVDS output common-mode voltage is specified as V_{OS} and may be found in *Table 10*. This pin is always active, in both ECM and Non-ECM. See *Section 17.4.2 Output Control and Adjust* for more information.

17.3.2 Extended Control Mode

In Extended Control Mode (ECM), all available functions are controlled via the Serial Interface. In addition to this, several of the control pins remain active. See *Table 16* for details. ECM is selected by setting $\overline{ECE}$ (Pin B3) to logic-low.

The space version of the ADC10D1000 does not include a Power-on Reset. Therefore, when powered up in ECM, the registers will be in an unknown, random state. There are two ways to set the ECM registers: toggling the $\overline{ECEb}$ pin, and writing the registers. If the device is programmed into Non-ECM (by setting $\overline{ECEb}$ logic high), the registers are programmed to their default values. So, if the $\overline{ECEb}$ pin is set to logic high, then set to logic low (ECM), the device will be in ECM and the registers will have their default values. The second method is to simply explicitly write the default (or otherwise desired) values to the register in ECM. This is the recommended method.

Four pins on the ADC10D1000 control the Serial Interface; $\overline{SCS}$, SCLK, SDI and SDO. This section covers the Serial Interface. The *Section 19.0 Register Definitions* are located at the end of the datasheet so that they are easy to locate.

17.3.2.1 The Serial Interface

The ADC10D1000 offers a Serial Interface that allows access to the sixteen control registers within the device. The Serial Interface is a generic 4-wire (optionally 3-wire) synchronous interface that is compatible with SPI type interfaces that are used on many micro-controllers and DSP controllers. Each serial interface access cycle is exactly 24 bits long. A register-read or register-write can be accomplished in one cycle. The signals are defined in such a way that the user can opt to simply join SDI and SDO signals in his system to accomplish a single, bidirectional SDI/O signal. A summary of the pins for this interface may be found in *Table 14*. See *Figure 11* for the timing diagram and *Table 12* for timing specification details. Control register contents are retained when the device is put into power-down mode.

TABLE 14. Serial Interface Pins

Pin	Name
C4	$\overline{SCS}$ (Serial Chip Select bar)
C5	SCLK (Serial Clock)
B4	SDI (Serial Data In)
A3	SDO (Serial Data Out)

$\overline{SCS}$: Each assertion (logic-low) of this signal starts a new register access, i.e. the SDI command field must be ready. The user is required to de-assert this signal after the 24th clock. If the $\overline{SCS}$ is de-asserted before the 24th clock, no data read/write will occur. If the $\overline{SCS}$ is asserted longer than 24 clocks, data write will occur normally through the SDI input upon the 24th clock and the SDO output will hold the D0 bit until $\overline{SCS}$ is de-asserted. Setup and hold times, t_{SCS} and t_{HCS}, with respect to the SCLK must be observed.

SCLK: This signal is used to register the input data (SDI) on the rising edge; and to source the output data (SDO) on the falling edge. The user may disable the clock and hold it in the low-state. There is no minimum frequency requirement for SCLK; see f_{SCLK} in *Table 12* for more details.

SDI: Each register access requires a specific 24-bit pattern at this input, consisting of a command field and a data field. When in read mode, the data field is high impedance in case the bidirectional SDI/O option is used. Setup and hold times, t_{SH} and t_{SSU}, with respect to the SCLK must be observed.

SDO: This output is normally tri-stated and is driven only when $\overline{SCS}$ is asserted, the first 8 bits of command data have been received and it is a READ operation. The data is shifted out, MSB first, starting with the 8th clock's falling edge. At the end of the access, when $\overline{SCS}$ is de-asserted, this output is tri-stated once again. If an invalid address is accessed, the data sourced will consist of all zeroes. Setup and hold times, t_{SH} and t_{SSU}, with respect to the SCLK must be observed. If it is a READ operation, there will be a bus turnaround time, t_{BSU}, from when the last bit of the command field was read in until when the first bit of the data field is written out.

Table 15 shows the Serial Interface bit definitions.

TABLE 15. Command and Data Field Definitions

Bit No.	Name	Comments
1	Read/Write (R/W)	1**b** indicates a read operation 0**b** indicates a write operation
2-3	Reserved	Bits must be set to 10**b**
4-7	A<3:0>	16 registers may be addressed. The order is MSB first
8	X	This is a "don't care" bit
9-24	D<15:0>	Data written to or read from addressed register

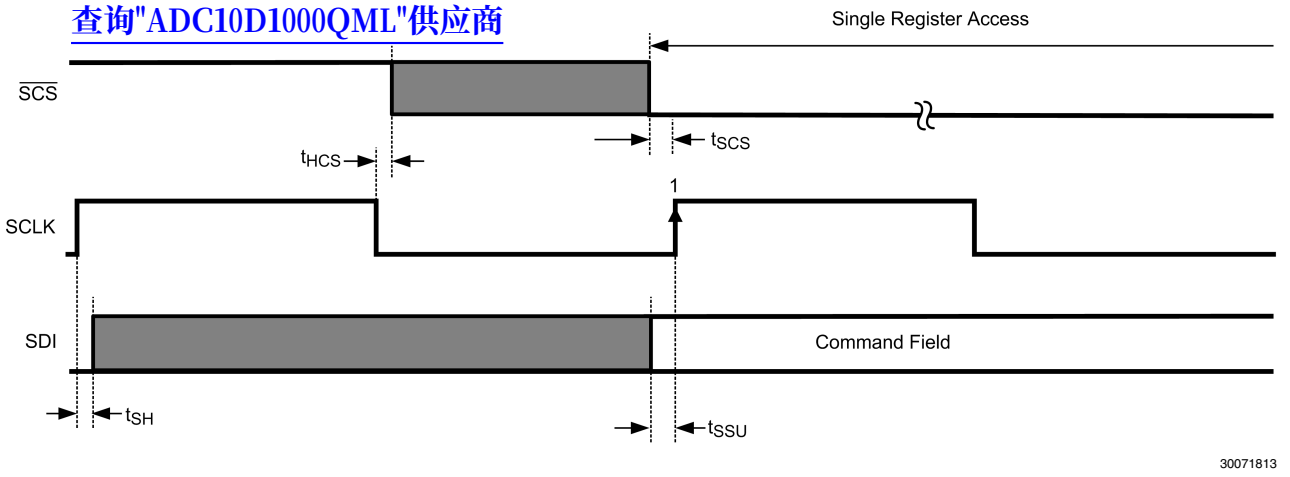


FIGURE 12. Serial Interface Timing (Zoom Start)***

***SCSb transition from High to Low must occur t_{HCS} after the falling edge of SCLK, and t_{SCS} before the rising edge of SCLK.

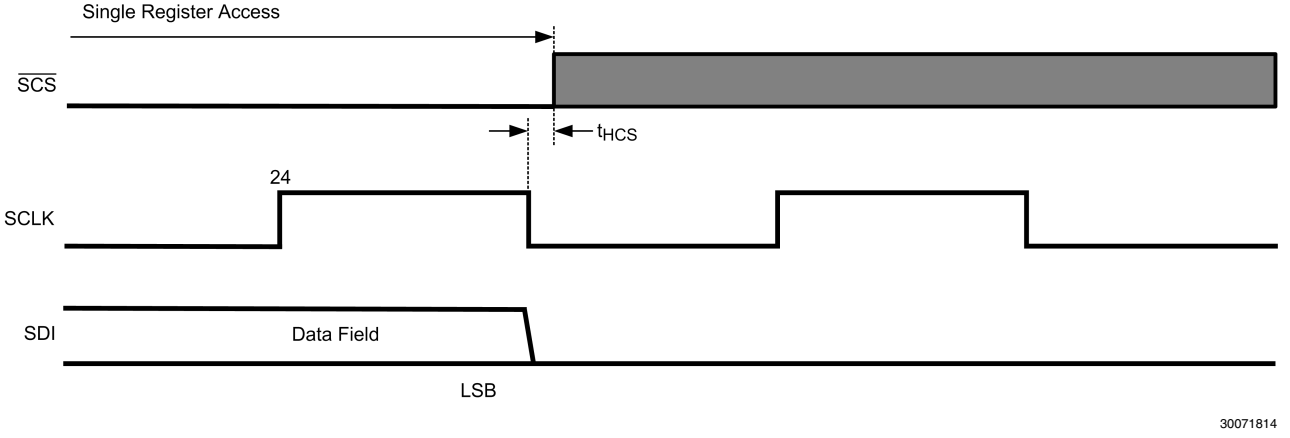


FIGURE 13. Serial Interface Timing (Zoom End)****

******SCSb transition from Low to High must occur t_{HCS} after the 24th SCLK cycle during a low cycle.

The serial data protocol is shown for a read and write operation in *Figure 14* and *Figure 15*, respectively.

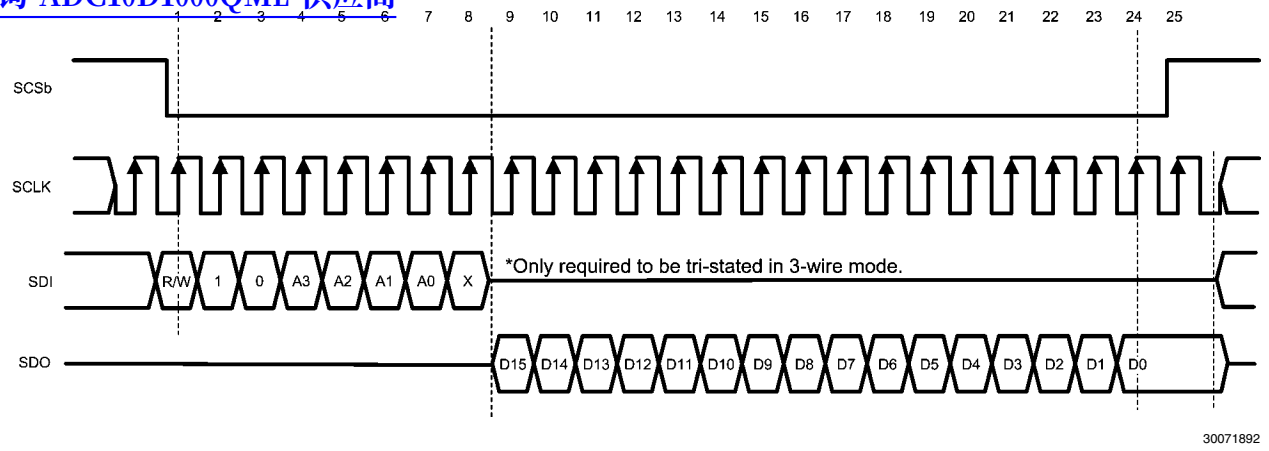


FIGURE 14. Serial Data Protocol - Read Operation

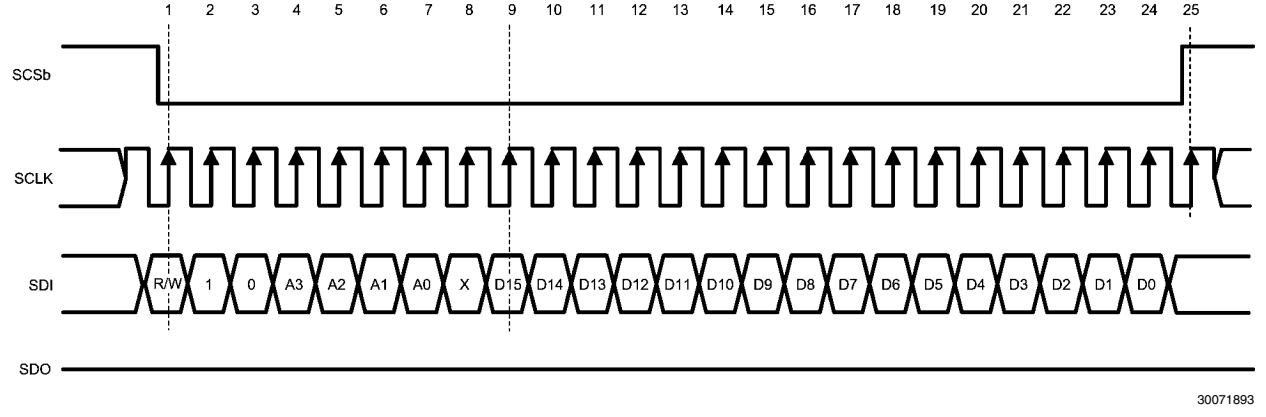


FIGURE 15. Serial Data Protocol - Write Operation

17.4 FEATURES

The ADC10D1000QML offers many features that make the device convenient to use in a wide variety of applications. *Table 16* is a summary of the features available, as well as details for the control mode chosen.

TABLE 16. Features and Modes

Feature	Non-ECM	Control Pin Active in ECM	ECM	Default ECM State
Input Control and Adjust				
Input Full-scale Adjust Setting	Selected via FSR (Pin Y3)	No	Selected via the Config Reg (Addr: 3**h** and B**h**)	mid FSR value
Input Offset Adjust Setting	Not Available	Not Applicable	Selected via the Config Reg (Addr: 2**h** and A**h**)	Offset = 0mV
LC Filter on Clock	Not Available	Not Applicable	Selected via the Config Reg (Addr: D**h**)	LC Filter off
Sampling Clock Phase Adjust	Not Available	Not Applicable	Selected via the Config Reg (Addr: C**h** and D**h**)	Phase adjust disable
DES/Non-DES Mode Selection	Not Available	No	Selected via DES bit (Addr: C**h** and D**h**	Non-DES Mode
Output Control and Adjust				
DDR Clock Phase Selection	Selected via DDRPh (Pin W4)	No	Selected via DPS in the Config Reg (Addr: 0**h**; Bit: 14)	0° Mode
LVDS Differential Output Voltage Amplitude Selection	Higher amplitude only	Not Applicable	Selected via OVS in the Config Reg (Addr: 0**h**; Bit: 13)	Higher amplitude
LVDS Common-Mode Output Voltage Amplitude Selection	Selected via V_{BG} (Pin B1)	Yes	Not available	Higher amplitude
Output Formatting Selection	Offset Binary only	Not Applicable	Selected via 2SC in the Config Reg (Addr: 0**h**; Bit: 4)	Offset Binary
Test Pattern Mode at Output	Selected via TPM (Pin A4)	No	Selected via TPM in the Config Reg (Addr: 0**h**; Bit: 12)	TPM not active
Demux/Non-Demux Mode Selection	Selected via NDM (Pin A5)	Yes	Not available	N/A
AutoSync	Not Available	Not Applicable	Selected via the Config Reg (Addr: E**h**)	Master Mode, RCOut1/2 disabled
DCLK RST	Not Available	Not Applicable	Select via the Config Reg (Addr: E**h**)	DLCK Reset disabled
Calibration				
On-command Calibration Event	Selected via CAL (Pin D6)	Yes	Selected via CAL in the Config Reg (Addr: 0**h**; Bit: 15)	N/A (CAL = 0)
Power-Down				
Power down I-channel	Selected via PDI (Pin U3)	Yes	Selected via PDI in the Config Reg (Addr: 0**h**; Bit: 11)	I-channel operational
Power down Q-channel	Selected via PDQ (Pin V3)	Yes	Selected via PDQ in the Config Reg (Addr: 0**h**; Bit: 10)	Q-channel operational

17.4.1 Input Control and Adjust

There are several features and configurations for the input of the ADC10D1000. This section covers Input Full Scale Range adjust, Input Offset adjust, DES/Non-DES Mode, sampling clock phase adjust, and LC filter on the sampling Clock.

17.4.1.1 Input Full-Scale Range Adjust

The input full-scale range for the ADC10D1000 may be adjusted via Non-ECM or ECM. In Non-ECM, a control pin selects a higher or lower value; see *Section 17.3.1.7 Full-Scale Input Range Pin (FSR)* . See V_{IN} in *Table 7* for electrical specification details. In ECM, the input full-scale range may be selected with 15-bits of precision. See FS_ADJ also in *Table 7* for details. Note that the higher and lower full-scale input range settings in Non-ECM do not correspond to the maximum and minimum full-scale input range settings in ECM. It is necessary to execute a manual calibration following any change of the input full-scale range. See *Section 19.0 Register Definitions* for information about the registers.

17.4.1.2 Input Offset Adjust

The input offset adjust for the ADC10D1000 may be adjusted with 12-bits of precision plus sign via ECM. See *Section 19.0 Register Definitions* for information about the registers.

17.4.1.3 DES/Non-DES Mode

The ADC10D1000 is available in Dual-Edge Sampling (DES) or Non-DES Mode. The DES Mode allows for the ADC10D1000's Q-channel input to be sampled by both channels' ADCs. One ADC samples the input on the rising edge of the input clock and the other ADC samples the same input on the falling edge of the input clock. A single input is thus sampled twice per input clock cycle, resulting in an overall sample rate of twice the input clock frequency, e.g. 2.0 GSPS with a 1.0 GHz input clock. See*Section 17.3.1.1 Non-Demultiplexed Mode Pin (NDM)* for information on how to select the desired mode.

For the DES Mode, only the Q-channel may be used for the input. This may be selected in ECM by using the DES bit (Addr: 0**h**, Bit 7) to select the DES Mode and the DESQ bit (Addr: 0**h**, Bit: 6) to select the Q-channel as input.

In this mode, the outputs must be carefully interleaved in order to reconstruct the sampled signal. If the device is programmed into the 1:4 Demux DES Mode, the data is effectively demultiplexed by 1:4. If the input clock is 1.0 GHz, the effective sampling rate is doubled to 2.0 GSPS and each of the 4 output buses has an output rate of 500 MHz. All data is available in parallel. To properly reconstruct the sampled waveform, the four words of parallel data that are output with each DCLK must be correctly interleaved. The sampling order is as follows, from the earliest to the latest: DQd, DId, DQ, DI. See *Figure 5*. If the device is programmed into the Non-demux DES Mode, two bytes of parallel data are output with each edge of the DCLK in the following sampling order, from the earliest to the latest: DQ, DI. See *Figure 8*.

The performance of the ADC10D1000 in DES mode depends on how well the two channels are interleaved, i.e that the clock samples each channel with precisely a 50% duty cycle, each channel has the same offset (nominally code 511/512), and each channel has the same full scale range. The ADC10D1000 also includes an automatic clock phase background adjustment in DES Mode to automatically and continuously adjust the clock phase of the I- and Q-channels. This feature removes the need to adjust the clock phase setting manually and provides optimal performance in the DES Mode. A difference exists in the typical offset between the I and Q channels, which can be removed via the offset adjust feature in ECM, to optimize DES mode performance. To adjust the I and Q channel offset, measure a histogram of the digital data and adjust the offset via the control register until the histogram is centered at code 511/512. Similarly, the full scale range of each channel may be adjusted for optimal performance.

17.4.1.4 Sampling Clock Phase Adjust

The sampling clock (CLK) phase may be delayed internally to the ADC up to 825 ps in ECM. This feature is intended to help the system designer remove small imbalances in clock distribution traces at the board level when multiple ADCs are used, or simplify complex system functions such as beam steering for phase array antennas. A clock-jitter cleaner is available only when the CLK phase adjust feature is used. This adjustment delays all clocks, including the DCLKs and output data, the user is strongly advised to use the minimal amount of adjustment and verify the net benefit of this feature in the system before relying on it.

17.4.1.5 LC Filter on Input Clock

A LC bandpass filter is available on the ADC10D1000 sampling clock to clean jitter on the incoming clock. This feature is available when the CLK phase adjust is also used. This feature was designed to minimize the dynamic performance degradation resulting from additional clock jitter as much as possible. This feature is available in ECM via the LCF (LC Filter) bits in the Control Register (Addr: D**h**, Bits 7:0).

If the clock phase adjust feature is enabled, the sampling clock passes through additional gate delay, which adds jitter to the clock signal. The LC filter helps to remove this additional jitter, so it is only available when the clock phase adjust feature is also enabled. To enable both features, use SA (Addr: D**h**, Bit 8). The LCF bits are thermometer encoded and may be used to set a filter center frequency ranging from 0.8 GHz to 1.5 GHz; See *Table 17*.

TABLE 17. LC Filter Code vs. f_C

LCF (7:0)	LCF(7:0)	f_C (GHz)
0	0000 0000**b**	1.5
1	0000 0001**b**	1.4
2	0000 0011**b**	1.3
3	0000 0111**b**	1.2
4	0000 1111**b**	1.1
5	0001 1111**b**	1.0
6	0011 1111**b**	0.92
7	0111 1111**b**	0.85
8	1111 1111**b**	0.8

The LC Filter is a second-order bandpass filter, which has the following simulated bandwidth for a center frequency, f_c at 1GHz, See *Table 18*

TABLE 18. LC Filter Bandwidth at 1GHz

Bandwidth [dB]	-3	-6	-9	-12
Bandwidth [MHz]	±135	±235	±360	±525

17.4.2 Output Control and Adjust

There are several features and configurations for the output of the ADC10D1000 so that it may be used in many different applications. This section covers DDR clock phase, LVDS

output differential and common-mode voltage, output formatting, Demux/Non-demux Mode and Test Pattern Mode.

17.4.2.1 DDR Clock Phase

The ADC10D1000 output data is always delivered in Double Data Rate (DDR). With DDR, the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK; see *Figure 16*. The DCLK-to-Data phase relationship may be either 0° or 90°. For 0° Mode, the Data transitions on each edge of the DCLK. Any offset from this timing is t_{OSK}; see *Table 12* for details. For 90° Mode, the DCLK transitions in the middle of each Data cell. Setup and hold times for this transition, t_{SU} and t_H, may also be found in *Table 12*. The DCLK-to-Data phase relationship may be selected via the DDRPh Pin in Non-ECM (see *Section 17.3.1.2 Dual Data Rate Phase Pin (DDRPh)*) or the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14) in ECM.

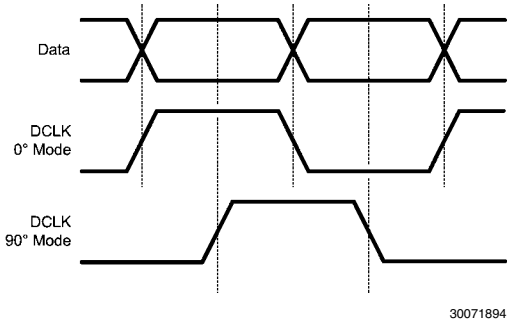


FIGURE 16. DDR DCLK-to-Data Phase Relationship

17.4.2.2 LVDS Output Differential Voltage

The ADC10D1000 is available with a selectable higher or lower LVDS output differential voltage. This parameter is V_{OD} and may be found in *Table 10*. The desired voltage may be selected via OVS Bit (Addr: 0**h**, Bit 13); see *Section 19.0 Register Definitions* for more information. In non-extended control mode only higher V_{OD} is available.

17.4.2.3 LVDS Output Common-Mode Voltage

The ADC10D1000 is available with a selectable higher or lower LVDS output common-mode voltage. This parameter is V_{OS} and may be found in *Table 10*. See *Section 17.3.1.8 LVDS Output Common-mode Pin (V_{BG})* for information on how to select the desired voltage.

17.4.2.4 Output Formatting

The formatting at the digital data outputs may be either offset binary or two's complement. The desired formatting must be set via the ECM; see *Section 19.0 Register Definitions* for more information.

17.4.2.5 Demux/Non-demux Mode

The ADC10D1000 may be in one of two demultiplex modes: Demux Mode or Non-Demux Mode (also sometimes referred to as 1:1 Demux Mode). In Non-demux Mode, the data from the input is simply output at the sampling rate at which it was sampled on one 10-bit bus. In Demux Mode, the data from the input is output at half the sampling rate, on twice the number of buses. See *Figure 1*. Demux/Non-demux Mode may only be selected by the NDM pin; see *Section 17.3.1.1 Non-Demultiplexed Mode Pin (NDM)*. In Non-DES Mode, the output data from each channel may be demultiplexed by a factor of 1:2 (1:2 Demux Non-DES Mode). In DES Mode, the output data from both channels interleaved may be demultiplexed (1:4 Demux DES Mode) or not demultiplexed (Non-Demux DES Mode).

17.4.2.6 Test Pattern Mode

The ADC10D1000 can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In Test Pattern Mode, the ADC is disengaged and a test pattern generator is connected to the outputs, including ORI and ORQ. The test pattern output is the same in DES Mode or Non-DES Mode. Each port is given a unique 10-bit word, alternating between 1's and 0's. When the part is programmed into the Demux Mode, the test pattern's order will be as described in *Table 19*.

TABLE 19. Test Pattern by Output Port in 1:2 Demux Mode

Time	Qd	Id	Q	I	ORQ	ORI	Comments
T0	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	Pattern Sequence **n**
T1	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T2	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T3	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T4	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T5	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	Pattern Sequence **n+1**
T6	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T7	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T8	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T9	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T10	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	Pattern Sequence **n+2**
T11	3FF**h**	3FE**h**	3FD**h**	3FB**h**	1**b**	1**b**	
T12	000**h**	001**h**	002**h**	004**h**	0**b**	0**b**	
T13	...	...	...	...	...	...	

When the part is programmed into the Non-demux Mode, the test pattern's order is as described in *Table 20*.

TABLE 20. Test Pattern by Output Port in Non-Demux Mode

Time	I	Q	ORI	ORQ	Comments
T0	001**h**	000**h**	0**b**	0**b**	Pattern Sequence **n**
T1	001**h**	000**h**	0**b**	0**b**	
T2	3FE**h**	3FF**h**	1**b**	1**b**	
T3	3FE**h**	3FF**h**	1**b**	1**b**	
T4	001**h**	000**h**	0**b**	0**b**	
T5	3FE**h**	3FF**h**	1**b**	1**b**	
T6	001**h**	000**h**	0**b**	0**b**	
T7	3FE**h**	3FF**h**	1**b**	1**b**	
T8	3FE**h**	3FF**h**	1**b**	1**b**	
T9	3FE**h**	3FF**h**	1**b**	1**b**	
T10	001**h**	000**h**	0**b**	0**b**	Pattern Sequence **n+1**
T11	001**h**	000**h**	0**b**	0**b**	
T12	3FE**h**	3FF**h**	1**b**	1**b**	
T13	3FE**h**	3FF**h**	1**b**	1**b**	
T14	...	...	...	...	

17.4.3 Calibration Feature

The ADC10D1000 must be calibrated to achieve specified performance. The calibration procedure is exactly the same regardless of how it was initiated or when it is run. The DCLK outputs will be present during all phases of the calibration process. All data and over-range output bits are held at logic low during calibration. Calibration should be performed in the planned mode of operation. Calibration trims the analog input differential termination resistor, the CLK input resistor, and sets internal bias currents which affects the Linearity of the converter. This minimizes full-scale error, offset error, DNL and INL, resulting in maximizing the dynamic performance as measured by: SNR, THD, SINAD (SNDR) and ENOB.

17.4.3.1 Calibration Pins

Table 21 is a summary of the pins used for calibration. See *Section 8.0 Column Descriptions and Equivalent Circuits* for complete pin information and *Figure 10* for the timing diagram.

TABLE 21. Calibration Pins

Pin	Name	Function
D6	CAL (Calibration)	Initiate calibration event; see *Section 17.3.1.3 Calibration Pin (CAL)*
B5	CalRun (Calibration Running)	Indicates when calibration is running
C1/D2	Rtrim+/- (Input termination trim resistor)	External resistor used to calibrate analog and CLK inputs
C3/D3	Rext+/- (External Reference resistor)	External resistor used to calibrate internal linearity

17.4.3.2 How to Initiate a Calibration Event

The calibration event must be initiated by holding the CAL pin low for at least t_{CAL_L} clock cycles, and then holding it high for at least another t_{CAL_H} clock cycles, as defined in *Table 12*. The minimum t_{CAL_L} and t_{CAL_H} input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. The time taken by the calibration procedure is specified as t_{CAL}. In ECM, either the CAL bit (Addr: 0**h**; Bit: 15) or the CAL pin may be used to initiate a calibration event.

17.4.3.3 On-command Calibration

An on-command calibration must be run after power up and whenever the FSR is changed. It is recommended to execute an on-command calibration whenever the settings or conditions to the device are altered significantly, in order to obtain optimal parametric performance. Some examples include: changing the FSR via either ECM or Non-ECM, power-cycling either channel, and switching into or out of DES Mode. For best performance, it is also recommended that an on-command calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly, relative to the specific system performance requirements.

Due to the nature of the calibration feature, it is recommended to avoid unnecessary activities on the device while the calibration is taking place. For example, do not read or write to the Serial Interface or use the DCLK Reset feature while calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Also, it is recommended to not apply a strong narrow-band signal to the analog inputs during calibration because this may impair the accuracy of the calibration; broad spectrum noise is acceptable.

17.4.3.4 Calibration Adjust

The calibration event itself may be adjusted, for sequence and mode. This feature can be used if a shorter calibration time than the default is required; see t_{CAL} in *Table 12*. However, the performance of the device, when using a shorter calibration time than the default setting, is not guaranteed.

The calibration sequence may be adjusted via CSS (Addr: 4h, Bit 14). The default setting of CSS = 1b executes both R_{IN} and $R_{IN_}$CLK Calibration (using Rtrim) and internal linearity Calibration (using Rext). Executing a calibration with CSS = 0b executes only the internal linearity Calibration. The first time that Calibration is executed, it must be with CSS = 1b to trim R_{IN} and $R_{IN_}$CLK. However, once the device is at its operating temperature and R_{IN} has been trimmed at least one time, it will not drift significantly. To save time in subsequent calibrations, trimming R_{IN} and $R_{IN_}$CLK may be skipped, i.e. by setting CSS = 0b.

The mode may be changed, to save calibration execution time for the internal linearity Calibration. See t_{CAL} in *Table 12*. Adjusting CMS(1:0) will select three different pre-defined calibration times. A larger amount of time will calibrate each channel more closely to the ideal values, but choosing shorter times will not significantly impact the performance. The fourth setting, CMS(1:0) = 11b, is not available.

17.4.3.5 Calibration and Power-Down

If PDI and PDQ are simultaneously asserted during a calibration cycle, the ADC10D1000 will immediately power down. The calibration cycle will continue when either or both channels are powered back up, but the calibration will be compromised due to the incomplete settling of bias currents directly after power up. Therefore, a new calibration should be executed upon powering the ADC10D1000 back up. In general, the ADC10D1000 should be re-calibrated when either or both channels are powered back up, or after one channel is powered down. For best results, this should be done after the device has stabilized to its operating temperature.

17.4.4 Power Down

On the ADC10D1000, the I- and Q-channels may be powered down individually. This may be accomplished via the control pins, PDI and PDQ, or via ECM. In ECM, the PDI and PDQ pins are logically OR'd with the Control Register setting. See *Section 17.3.1.4 Power Down I-channel Pin (PDI)* and *Section 17.3.1.5 Power Down Q-channel Pin (PDQ)* for more information.

18.0 Applications Information

18.1 THE ANALOG INPUTS

The ADC10D1000 will continuously convert any signal which is present at the analog inputs, as long as a CLK signal is also provided to the device. This section covers important aspects related to the analog inputs including: acquiring the input, the reference voltage and FSR, out-of-range indication, AC coupled signals, and single-ended input signals.

18.1.1 Acquiring the Input

Data is acquired at the rising edge of CLK+ in Non-DES Mode and both the falling and rising edge of CLK+ in DES Mode. The digital equivalent of that data is available at the digital outputs a constant number of input clock cycles later for the DI, DQ, DId and DQd output buses, depending on the demultiplex mode which was chosen. See Pipeline Delay in *Table 12*. In addition to the Pipeline Delay, there is a constant output delay, t_{OD}, before the data is available at the outputs. See t_{OD} in *Table 12* and the Timing Diagrams.

For Demux Mode, the signal which is sampled at the input will appear at the output after a certain latency, as shown in *Table 22*.

TABLE 22. Input Channel Samples Produced at Data Outputs in Demultiplexed Mode

Data Outputs	Non-DES Mode	DES Mode (Q-channel only)
DI	I-channel sampled with rise of CLK, 34 cycles earlier.	Q-channel sampled with rise of CLK, 34 cycles earlier.
DQ	Q-channel sampled with rise of CLK, 34 cycles earlier.	Q-channel sampled with fall of CLK, 34.5 cycles earlier.
DId	I-channel sampled with rise of CLK, 35 cycles earlier.	Q-channel sampled with rise of CLK, 35 cycles earlier.
DQd	Q-channel sampled with rise of CLK, 35 cycles earlier.	Q-channel sampled with fall of CLK, 35.5 cycles earlier.

For Non-demux Mode, *Table 23* is similarly shown.

TABLE 23. Input Channel Samples Produced at Data Outputs in Non-Demux Mode

Data Outputs	Non-DES Mode	DES Mode (Q-channel only)
DI	I-channel sampled with rise of CLK, 34 cycles earlier.	Q-channel sampled with rise of CLK, 34 cycles earlier.
DQ	Q-channel sampled with rise of CLK, 34 cycles earlier.	Q-channel sampled with fall of CLK, 34.5 cycles earlier.
DId	No output; high impedance.	No output; high impedance.
DQd	No output; high impedance.	No output; high impedance.

18.1.2 The Reference Voltage and FSR

The full-scale analog differential input range (V_{IN_FSR}) of the ADC10D1000 is derived from an internal 1.254V bandgap reference. In Non-ECM, this full-scale range has two settings controlled by the FSR pin; (see *Section 17.3.1.7 Full-Scale Input Range Pin (FSR)*. The FSR Pin operates on both I- and Q-channels. In ECM, the full-scale range may be independently set for each channel via Addr: 3**h** and B**h** with 15 bits of precision; see *Section 19.0 Register Definitions*. The best SNR is obtained with a higher full-scale input range, but better distortion and SFDR are obtained with a lower full-scale input range. It is not possible to use an external analog reference voltage to modify the full-scale range, and this adjustment should only be done digitally, as described.

A buffered version of the internal 1.254V bandgap reference voltage is made available at the V_{BG} pin for the user. The V_{BG} pin can drive a load of up to 80 pF and source or sink up to ±100 µA. It should be buffered if more current than this is required. The pin remains as a constant reference voltage regardless of what full-scale range is selected and may be used for a system reference. V_{BG} is a dual-purpose pin and it may also be used to select a higher LVDS output common-mode voltage; see *Section 17.4.2.3 LVDS Output Common-Mode Voltage*.

18.1.3 Out-Of-Range Indication

Differential input signals are digitized to 10 bits, based on the full-scale range. Signal excursions beyond the full-scale range (greater than $+V_{IN}/2$ or less than $-V_{IN}/2$) will be clipped at the output. An input signal which is above the FSR will result in all 1's at the output and an input signal which is below the FSR will result in all 0's at the output. When the conversion result is clipped for the I-channel input, the Out-of-Range I-channel (ORI) output is activated such that ORI+ goes high and ORI- goes low for the time that the signal is out of range. This output is active as long as accurate data on either or both of the buses would be outside the range of 000**h** to 3FF**h**. The Q-channel has a separate ORQ which functions similarly.

18.1.4 AC-coupled Input Signals

The AC-coupled analog inputs require a precise common-mode voltage. This voltage, V_{CMO}, is generated on-chip. For the ADC10D1000 used in a typical application, this may be accomplished by on-board capacitors shown in *Figure 17*

As a result, an analog input channel that is not used (e.g. in DES Mode) should be connected to AC ground, i.e. through capacitors to ground . Do not connect an unused analog input directly to ground.

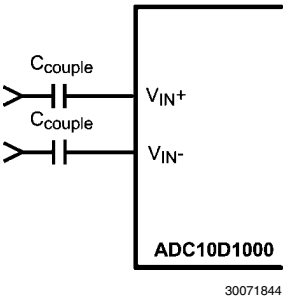


FIGURE 17. AC-coupled Differential Input

The analog inputs for the ADC10D1000 are internally buffered, which simplifies the task of driving these inputs and the RC pole which is generally used at sampling ADC inputs is not required. If the user desires to place an amplifier circuit before the ADC, care should be taken to choose an amplifier with adequate noise and distortion performance, and adequate gain at the frequencies used for the application.

18.1.5 Single-Ended Input Signals

It is possible for the ADC10D1000 to accept single-ended signals. The best way to handle single-ended signals is to first convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-transformer, as shown in *Figure 18*.

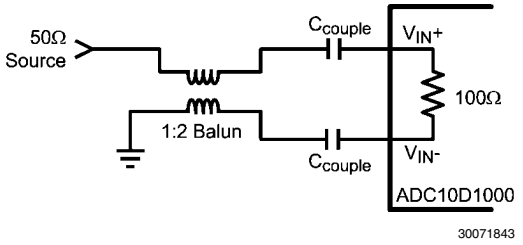


FIGURE 18. Single-Ended to Differential Conversion Using a Balun

When selecting a balun, it is important to understand the input architecture of the ADC. The impedance of the analog source should be matched to the ADC10D1000's on-chip 100Ω differential input termination resistor. The range of this termination resistor is specified as R_{IN} in *Table 7*.

18.2 THE CLOCK INPUTS

The ADC10D1000 has a differential clock input, CLK+ and CLK-, which must be driven with an AC-coupled, differential clock signal. This provides the level shifting to the clock to be driven with LVDS, PECL, LVPECL, or CML levels. The clock inputs are internally terminated to 100Ω differential and self-biased. This section covers coupling, frequency range, level, duty-cycle, jitter, and layout considerations.

18.2.1 CLK Coupling

The clock inputs of the ADC10D1000 must be capacitively coupled to the clock pins as indicated in *Figure 19*.

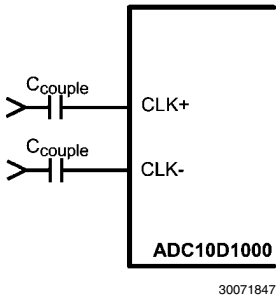


FIGURE 19. Differential Input Clock Connection

The choice of capacitor values will depend on the clock frequency, capacitor component characteristics, and other system factors.

18.2.2 CLK Frequency

Although the ADC10D1000 is tested and its performance is guaranteed with a differential 1.0 GHz clock, it will typically function well with input clock frequency range; see f_{CLK}(min) and f_{CLK}(max) in *Table 12*. Operation up f_{CLK}(max) is possible if the maximum ambient temperatures indicated are not exceeded. Operating at sample rates above f_{CLK}(max) for the given ambient temperature may result in reduced device reliability and product lifetime. This is due to the fact that higher sample rates results in higher power consumption and die temperatures. If the $f_{CLK} \leq$ 300MHz, enable LFS in control register (Addr: **0h** Bit 8).

18.2.3 CLK Level

The input clock amplitude is specified as V_{IN_CLK} in *Table 9*. Input clock amplitudes above this may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 511/512 when both input pins are at the same potential. Insufficient input clock levels will result in poor dynamic performance. Both of these results may be avoided by keeping the clock input amplitude within the specified limits of V_{IN_CLK}.

18.2.4 CLK Duty Cycle

The duty cycle of the input clock signal can affect the performance of any A/D Converter. The ADC10D1000 features a duty cycle clock correction circuit which can maintain performance over the 20%-to-80% specified clock duty cycle range. This feature is enabled by default and provides improved ADC clocking, especially in the Dual-Edge Sampling (DES) Mode.

18.2.5 CLK Jitter

High speed, high performance ADCs such as the ADC10D1000 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)} / V_{FSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN}))$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{FSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input.

$t_{J(MAX)}$ is the square root of the sum of the squares (RSS) sum of the jitter from all sources, including: the ADC input clock, system, input signals and the ADC itself. Since the effective jitter added by the ADC is beyond user control, it is recommended to keep the sum of all other externally added jitter to a mimimum.

18.2.6 CLK Layout

The ADC10D1000 clock input is internally terminated with a trimmed 100Ω resistor. The differential input clock line pair should have a characteristic impedance of 100Ω and (when using a balun), be terminated at the clock source in that (100Ω) characteristic impedance.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Otherwise, other signals can introduce jitter into the input clock signal. Also, the clock signal can also introduce noise into the analog path if it is not properly isolated.

18.3 THE LVDS OUTPUTS

The Data, ORI, ORQ, DCLKI and DCLKQ outputs are LVDS. The electrical specifications of the LVDS outputs are compatible with typical LVDS receivers available on ASIC and FPGA chips; but they are not IEEE or ANSI communications standards compliant due to the low +1.9V supply used on this chip. These outputs should be terminated with a 100Ω differential resister placed as closely to the receiver as possible.

This section covers common-mode and differential voltage, and data rate.

18.3.1 Common-mode and Differential Voltage

The LVDS outputs have selectable common-mode and differential voltage, V_{OS} and V_{OD}; see *Table 10*. See *Section 17.4.2 Output Control and Adjust* for more information.

Selecting the higher V_{OS} will also increase V_{OD} by up to 40mV. The differential voltage, V_{OD}, may be selected for the higher or lower value. For short LVDS lines and low noise systems, satisfactory performance may be realized with the lower V_{OD}. This will also result in lower power consumption. If the LVDS lines are long and/or the system in which the ADC10D1000 is used is noisy, it may be necessary to select the higher V_{OD}.

18.3.2 Output Data Rate

The data is produced at the output at the same rate as it is sampled at the input. The minimum recommended input clock rate for this device is $f_{CLK(MIN)}$; see *Table 12*. However, it is possible to operate the device in 1:2 Demux Mode and capture data from just one 10-bit bus, e.g. just DI (or DId) although both DI and DId are fully operational. This will decimate the data by two and effectively halve the data rate.

18.4 SYNCHRONIZING MULTIPLE ADC10D1000S IN A SYSTEM

The ADC10D1000 has two features to assist the user with synchronizing multiple ADCs in a system; AutoSync and DCLK Reset. The AutoSync feature is new and designates one ADC10D1000 as the Master ADC and other ADC10D1000s in the system as Slave ADCs. The DCLK Reset feature performs the same function as the AutoSync feature, but is the first generation solution to synchronizing multiple ADCs in a system; it is disabled by default. For the application in which there are multiple Master and Slave ADC10D1000s in a system, AutoSync may be used to synchronize the Slave ADC10D1000(s) to each respective Master ADC10D1000 and the DCLK Reset may be used to synchronize the Master ADC10D1000s with each other.

18.4.1 AutoSync Feature

AutoSync is a new feature which continuously synchronizes the outputs of multiple ADC10D1000s in a system. It may be used to synchronize the DCLK and data outputs of one or more Slave ADC10D1000s to one Master ADC10D1000. Several advantages of this feature include: no special synchronization pulse required, any upset in synchronization is recovered upon the next DCLK cycle, and the Master/Slave ADC10D1000s may be arranged as a binary tree so that any upset will quickly propagate out of the system.

An example system is shown below in *Figure 20* which consists of one Master ADC and two Slave ADCs. For simplicity, only one DCLK is shown; in reality, there is DCLKI and DCLKQ, but they are always in phase with one another.

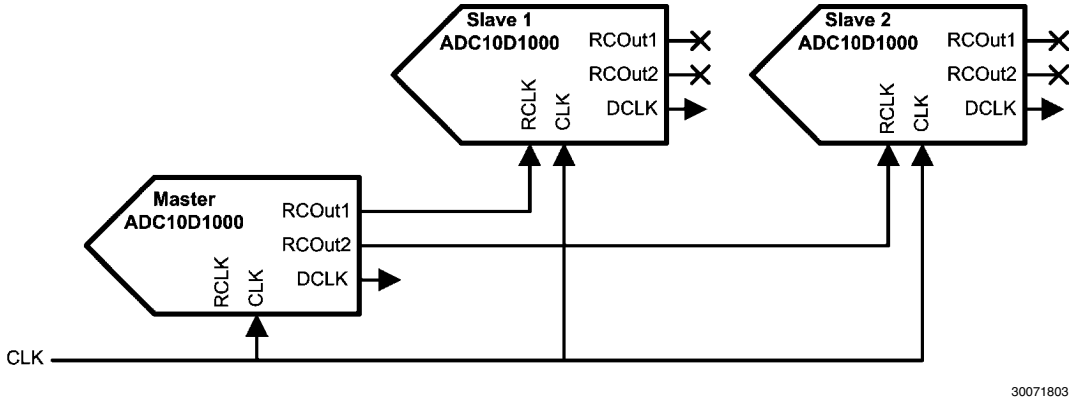


FIGURE 20. AutoSync Example

In order to synchronize the DCLK (and Data) outputs of multiple ADCs, the DCLKs must transition at the same time, as well as be in phase with one another. The DCLK at each ADC is generated from the CLK after some latency, plus t_{OD} minus t_{AD}. Therefore, in order for the DCLKs to transition at the same time, the CLK signal must reach each ADC at the same time. To tune out any differences in the CLK path to each ADC, the t_{AD} adjust feature may be used. However, using the t_{AD} adjust feature will also affect when the DCLK is produced at the output. If the device is in Demux Mode, then there are four possible phases which each DCLK may be generated on because the typical CLK = 1GHz and DCLK = 250 MHz for this case. The RCLK signal controls the phase of the DCLK, so that each Slave DCLK is on the same phase as the Master DCLK

The AutoSync feature may only be used via the Control Registers.

18.4.2 DCLK Reset Feature

The DCLK reset feature is available via ECM, but is disabled by default. DCLKI and DCLKQ are always synchronized, by design, and do not require a pulse from DCLK_RST to become synchronized.

The DCLK_RST signal must observe certain timing requirements, which are shown in *Figure 9* of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These timing specifications are listed as t_{PWR}, t_{RS} and t_{RH} and may be found in *Table 12*.

The DCLK_RST signal can be asserted asynchronously to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state (logic-high) in Demux Mode: in Non-Demux Mode, the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted, there are

t_{SYNC_DLY} CLK cycles of systematic delay and the next CLK rising edge synchronizes the DCLK output with those of other ADC10D1000s in the system. For 90° Mode (DDRPh = logic-high), the synchronizing edge occurs on the rising edge of CLK, 4 cycles after the first rising edge of CLK after DCLK_RST is released. For 0° Mode (DDRPh = logic-low), this is 5 cycles instead. The DCLK output is enabled again after a constant delay of t_{OD}.

For both Demux and Non-Demux Modes, there is some uncertainty about how DCLK comes out of the reset state for the first DCLK_RST pulse. For the second (and subsequent) DCLK_RST pulses, the DCLK will come out of the reset state in a known way. Therefore, if using the DCLK Reset feature, it is recommended to apply one "dummy" DCLK_RST pulse before using the second DCLK_RST pulse to synchronize the outputs. This recommendation applies each time the device or channel is powered-on.

When the DCLK_RST function is not going to be used it is recommended to pull the DCLK+ pin to AGND through a 261Ω resister and to pull the DCLK– pin to V_A through a 261Ω resister (See *Figure 21*). This will provide noise ammunity and prevent false resets.

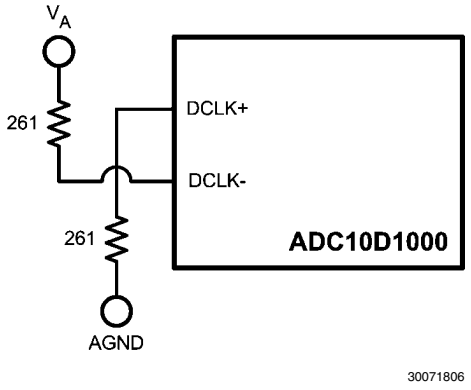


FIGURE 21. DCLK RST +/-

When using DCLK-RST to synchronize multiple ADC10D1000s, it is required that the Select Phase bits in the Control Register (Addr: E**h**, Bits 3,4) be the same for each Slave ADC10D1000.

18.5 SUPPLY/GROUNDING, LAYOUT AND THERMAL RECOMMENDATIONS

18.5.1 Power Planes

All supply buses for the ADC should be sourced from a common linear voltage regulator. This ensures that all power buses to the ADC are turned on and off simultaneously. This single source will be split into individual sections of the power plane, with individual decoupling and connection to the different power supply buses of the ADC. Due to the low voltage but relatively high supply current requirement, the optimal solution may be to use a switching regulator to provide an intermediate low voltage, which is then regulated down to the final ADC supply voltage by a linear regulator. Please refer to the documentation provided for the ADC10D1000RB for additional details on specific regulators that are recommended for this configuration

Power for the ADC should be provided through a broad plane which is located on one layer adjacent to the ground plane(s). Placing the power and ground planes on adjacent layers will provide low impedance decoupling of the ADC supplies, especially at higher frequencies. The output of a linear regulator should feed into the power plane through a low impedance multi-via connection. The power plane should be split into individual power peninsulas near the ADC. Each peninsula should feed a particular power bus on the ADC, with decoupling for that power bus connecting the peninsula to the ground plane near each power/ground pin pair. Using this technique can be difficult on many printed circuit CAD tools. To work around this, zero ohm resistors can be used to connect the power source net to the individual nets for the different ADC power buses. As a final step, the zero ohm resistors can be removed and the plane and peninsulas can be connected manually after all other error checking is completed.

18.5.1.1 Bypass Capacitors

The general recommendation is to have one 100nF capacitor for each power/ground pin pair. The capacitors should be surface mount multi-layer ceramic chip capacitors similar to Panasonic part number ECJ-0EB1A104K.

18.5.1.1.1 Ground Plane

Grounding should be done using continuous full ground planes to minimize the impedance for all ground return paths, and provide the shortest possible image/return path for all signal traces.

18.5.1.1.2 Power Supply Example

The ADC10D1000RB uses continuous ground planes (except where clear areas are needed to provide appropriate impedance management for specific signals), see *Figure 22*. Power is provided on one plane, with the 1.9V ADC supply being split into multiple zones or peninsulas for the specific power buses of the ADC. Decoupling capacitors are connected between these power bus peninsulas and the adjacent power planes using vias. The capacitors are located as close to the individual power/ground pin pairs of the ADC as possible. In most cases, this means the capacitors are located on the opposite side of the PCB to the ADC.

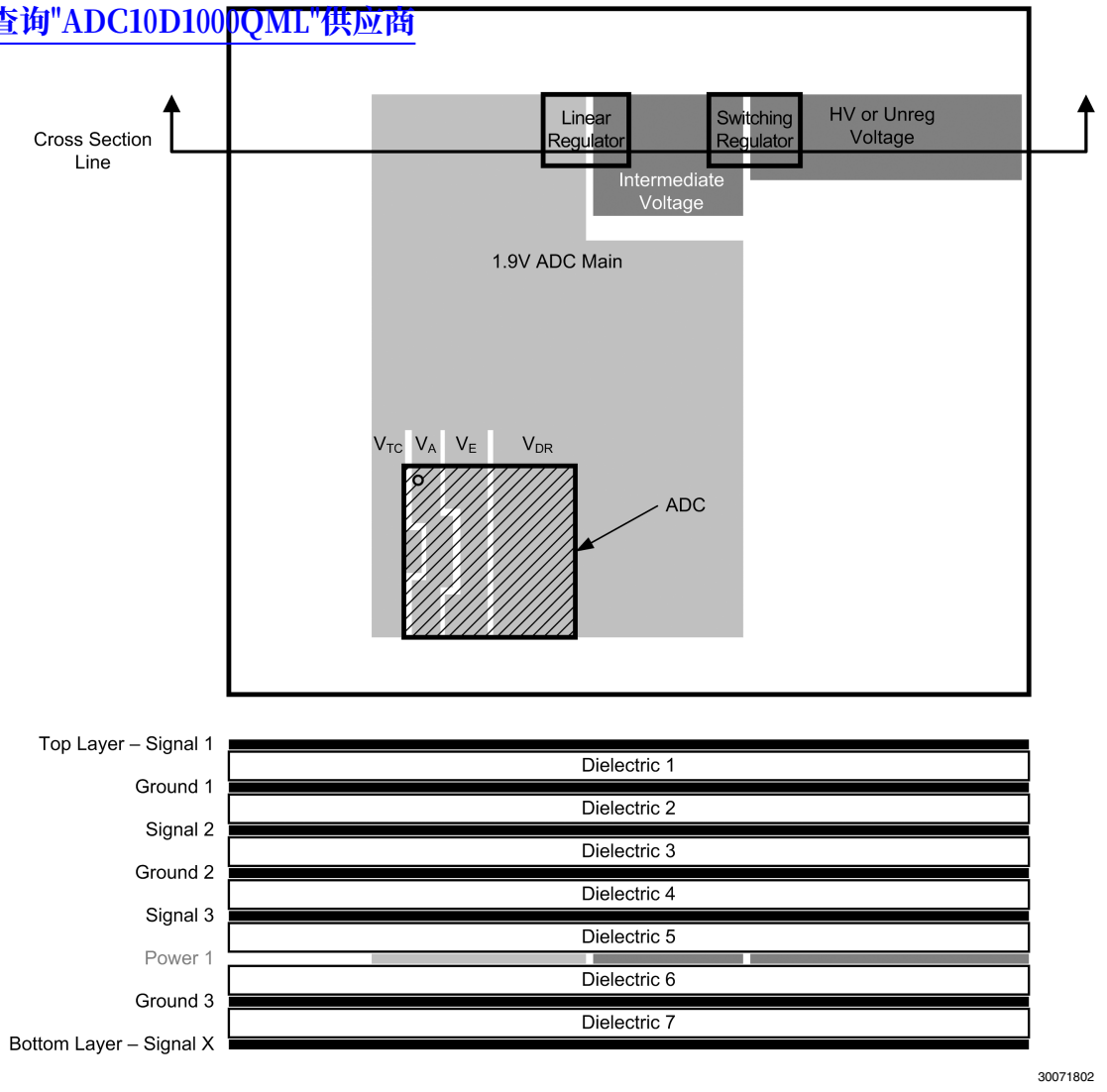


FIGURE 22. Power and Grounding Example

18.6 THERMAL MANAGEMENT

The Ceramic Column Grid Array (CCGA) package is a modified Ceramic Land Grid Array with an added heat sink. The signal columns on the outer edge are 1.27mm pitch, while the columns in the center attached to the heat sink are 1mm. The smaller pitch for the center columns is to improve the thermal resistance. The center columns of the package are attached to the back of the die through a heat sink. Connecting these columns to the PCB ground planes with a low thermal resistance path is the best way to remove heat from the ADC. These pins should also be connected to the ground planes through low impedance path for electrical purposes.

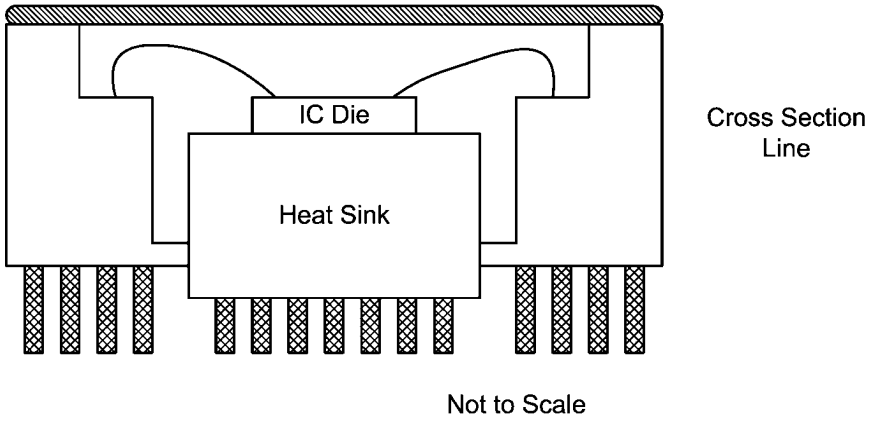


FIGURE 23. CCGA Conceptual Drawing

18.7 TEMPERATURE SENSOR DIODE

The ADC10D1000 has a diode temperature sensor that can be connected to pins Tdiode+/- which may be used to monitor the die temperature. National also provides a family of temperature sensors for this application which monitor different numbers of external devices, See *Table 24*.

TABLE 24. Temperature Sensor Recommendation

Number of External Devices Monitored	Recommended Temperature Sensor
1	LM95235
2	LM95213
4	LM95214

The LM95235/13/14 is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) interface that can monitor the temperature of one/two/four remote diodes as well as its own temperature. The LM95235/13/14 can be used to accurately monitor the temperature of up to one/two/four external devices such as the ADC10D1000, a FPGA, other system components, and the ambient temperature.

The LM95235/13/14 reports temperature in two different formats for +127.875°C range and 0°/255°C range. The LM95235/13/14 has a Sigma-Delta ADC core which provides the first level of noise immunity. For improved performance in a noise environment, the LM9535/13/14 includes programmable digital filters for Remote Diode temperature readings. When the digital filters are invoked, the resolution for the Remote Diode readings increases to 0.03125°C. For maximum flexibility and best accuracy, the LM95235/13/14 includes offset registers that allow calibration of other diode types.

Diode fault detection circuitry in the LM95235/13/14 can detect the absence or fault state of a remote diode: whether D+ is shorted to the power supply, D- or ground, or floating.

In the following typical application, the LM95213 is used to monitor the temperature of an ADC10D1000 as well as a FPGA. See *Figure 24*

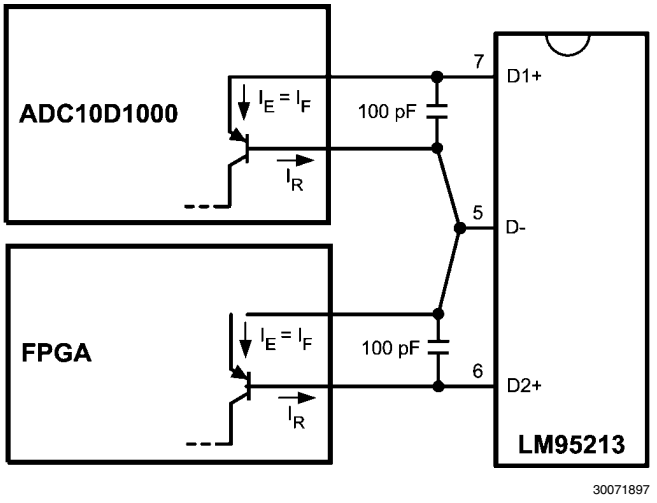


FIGURE 24. Typical Temperature Sensor Application

18.8 RADIATION ENVIRONMENTS

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

18.8.1 Total Ionizing Dose

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the Ordering Information table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883, Test Method 1019. Wafer level TID data is available with lot shipments.

18.8.2 Single Event Latch-Up and Functional Interrupt

One time single event latch-up (SEL) and single event functional interrupt (SEFI) testing was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LETth) shown in the Key Specifications table on the front page is the maximum LET tested. A test report is available upon request.

18.8.3 Single Event Upset

A report on single event upset (SEU) is available upon request.

18.9 BOARD MOUNTING RECOMMENDATION

A typical thermal profile is used to establish re-flow under the package and ensure all joints meet profile specifications, See *Table 25*.

TABLE 25. Solder Profile Specification

Range Up °C/sec	≤ 4°C/sec
Peak Temp (Tpk) °C	210°C ≤Tpk ≤ 215°C
Max Peak Temp °C	≤ 220°C
Ramp down °C/sec	≤ 5°C/sec

The 220°C peak temperature is driven by the requirement to limit the dissolution of lead from the high-melt column to the eutectic solder. To much lead increases the effective melting point of the board side joint and makes it much more difficult to remove the part if module rework is required.

Cool down rates and methods affect CCGA assemble yield and reliability. Picking up boards or opening the oven while solder joints are in molten state can disturb the solder joint. Boards should not be picked up until the solder joints have fully solidified. Board warping may potentially cause CCGA lifting off pads during cooling and this condition can also cause column cracking when severe. This warping is a result of a high differential cooling rate between the top and bottom of the board. Both conditions can be prevented by using even top and bottom cooling.

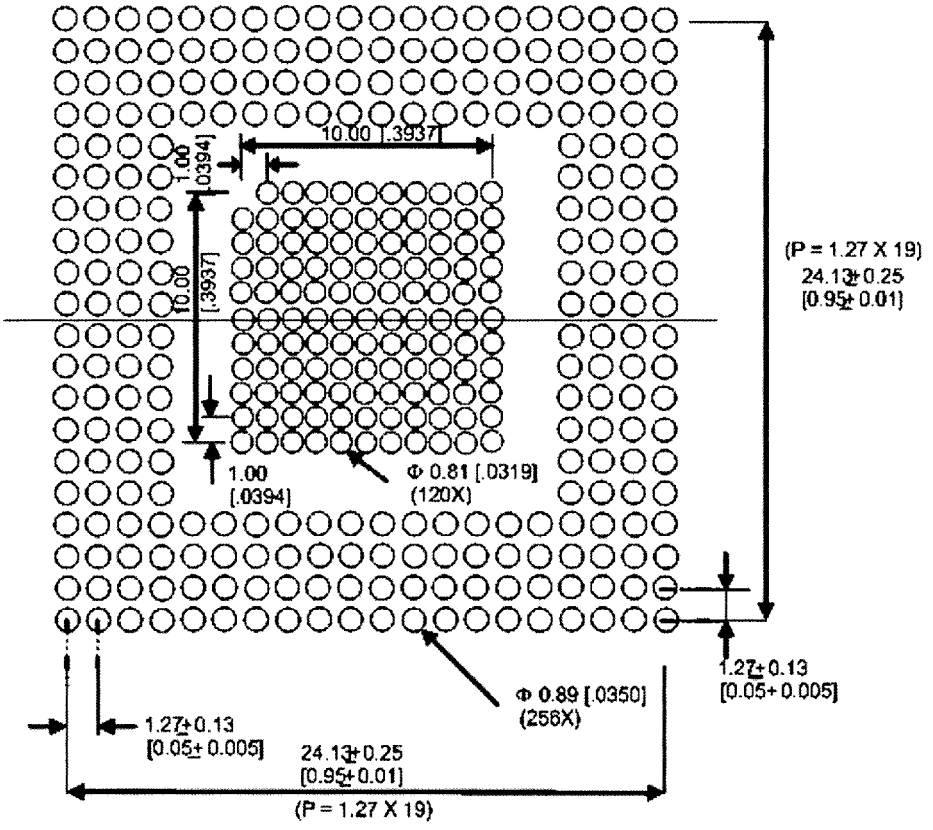


FIGURE 25. Landing Pattern Recommendation

19.0 Register Definitions

Eight read/write registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Non-extended Control Mode. The ADC10D1000 does not have a Power-On Reset. The user can write the registers with the desired values, or in Extended Control Mode set $\overline{ECE}$**b** Logic high setting resisters to the default values.

TABLE 26. Register Addresses

A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0**h**	Configuration Register 1
0	0	0	1	1**h**	Res
0	0	1	0	2**h**	I-channel Offset
0	0	1	1	3**h**	I-channel FSR
0	1	0	0	4**h**	Res
0	1	0	1	5**h**	Res
0	1	1	0	6**h**	Res
0	1	1	1	7**h**	Res
1	0	0	0	8**h**	Res
1	0	0	1	9**h**	Res
1	0	1	0	A**h**	Q-channel Offset
1	0	1	1	B**h**	Q-channel FSR
1	1	0	0	C**h**	Aperture Delay Coarse Adjust
1	1	0	1	D**h**	Aperture Delay Fine Adjust and LC Filter Adjust
1	1	1	0	E**h**	AutoSync
1	1	1	1	F**h**	Res

Configuration Register 1

Addr: 0**h** (0000**b**)																Default Values: 2000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAL	DPS	OVS	TPM	PDI	PDQ	Res	LFS	DES	DESQ	Res	2SC	Res			
DV	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15 CAL: Calibration Enable. When this bit is set 1**b**, an on-command calibration cycle is initiated. This bit is not reset automatically upon completion of the cal cycle. Therefore, the user must reset this bit to 0**b** and then set it to 1**b** again to initiate another calibration event. This bit is logically OR'd with the CAL Pin; both bit and pin must be set to **0b** before either is used to execute a calibration.

Bit 14 DPS: DDR Phase Select. Set this bit to 0**b** to select the 0° Mode DDR Data-to-DCLK phase relationship and to 1**b** to select the 90° Mode. This bit has no effect when the device is in Non-Demux Mode.

Bit 13 OVS: Output Voltage Select. This bit sets the differential voltage level for the LVDS outputs including Data, OR, RCOut1, RCOut2 and DCLK. 0**b** selects the lower level and 1**b** selects the higher level. See V_{OD} in *Table 10* for details.

Bit 12 TPM: Test Pattern Mode. When this bit is set to 1**b**, the device will continually output a fixed digital pattern at the digital Data and OR outputs. When set to 0**b**, the device will continually output the converted signal, which was present at the analog inputs. See *Section 17.4.2.6 Test Pattern Mode* for details about the TPM pattern.

Bit 11 PDI: Power-down I-channel. When this bit is set to 0**b**, the I-channel is fully operational, but when it is set to 1**b**, the I-channel is powered-down. The I-channel may be powered-down via this bit or the PDI Pin, which is active, even in ECM.

Bit 10 PDQ: Power-down Q-channel. When this bit is set to 0**b**, the Q-channel is fully operational, but when it is set to 1**b**, the Q-channel is powered-down. The Q-channel may be powered-down via this bit or the PDQ Pin, which is active, even in ECM.

Bits 9 Reserved. Must be set to 0**b**.

Bits 8 LFS: Low Frequency Select. If the sampling Clock (CLK) is at or below 300MHz, set this bit to 1**b**.

Bit 7 DES: Dual-Edge Sampling Mode select. When this bit is set to 0b, the device will operate in the Non-DES Mode; when it is set to 1b, the device will operate in the DES Mode. See *Section 17.4.1.3 DES/Non-DES Mode* for more information about DES/Non-DES Mode.

Bit 6 DESQ: DES Q-channel select. When the device is in DES Mode, this bit should be set to 1**b** selecting the Q-channel.

Bit 5 Reserved

Bit 4 2SC: Two's Complement output. For the default setting of 0**b**, the data is output in Offset Binary format; when set to 1**b**, the data is output in Two's Complement format.

Bits 3:0 Reserved. Must be set to 0**b**.

Reserved

Addr: 1**h** (0001**b**)																Default Values: 2A00**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

Bits 15:0 Reserved. Must be set as shown.

I-channel Offset Adjust

Addr: 2**h** (0010**b**)																Default Values: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			OS	OM(11:0)											
DV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:13 Reserved. Must be set to 0**b**.

Bit 12 OS: Offset Sign. The default setting of 0**b** incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bet to 1**b** incurs a negative offset of the set magnitude.

Bits 11:0 OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0**d** to 45 mV for OM(11:0) = 4095**d** in steps of ~11 µV. Monotonicity is guaranteed by design only for the 9MSBs.

Code	**Offset [mV]**
0000 0000 0000 (default)	0
1000 0000 0000	22.5
1111 1111 1111	45

I-channel Full Scale Range Adjust

Addr: 3**h** (0011**b**)																Default Values: 4000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res.	FM(14:0)														
DV	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15 Reserved. Must be set to 0**b**.

Bits 14:0 FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 630 mV (0**d**) to 980 mV (32767**d**) with the default setting at 820 mV (162384**d**). Monotonicity is guaranteed by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in EC, i.e. FSR values above 820 mV. See *Table 7* for characterization details.

Code	**FSR [mV]**
000 0000 0000 0000	630
100 0000 0000 0000 (default)	820
111 1111 1111 1111	980

Calibration Adjust

Addr: 4**h** (0100**b**) Default Values: DA7F**h**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	CSS	Reserved				CMS		Reserved							
DV	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	1

Bits 15 Reserved. Must be set as shown.

Bit 14 CSS: Calibration Sequence Select. The default 1b selects the following calibration sequence: reset all previously calibrated elements to nominal values, do R_{IN} Calibration, do internal linearity Calibration. Setting CSS = 0b selects the following calibration sequence: do not reset RIN to its nominal value, skip R_{IN} calibration, do internal linearity Calibration. The calibration must be completed at least one time with CSS = 1b to calibrate R_{IN}. Subsequent calibrations may be run with CSS = 0b (skip R_{IN} calibration) or 1b (full R_{IN} and internal linearity Calibration).

Bits 13:10 Reserved. Must be set as shown.

Bits 9:8 CMS (1:0): Calibration Mode Select. These bits affect the length of time taken to calibrate the internal linearity. See t_{CAL} in *Table 12*.

Bits 7:0 Reserved. Must be set as shown

Reserved

Addr: 5**h** (0101**b**) Default Values: XXXX**h**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bits 15:0 Reserved. Do not write.

Reserved

Addr: 6**h** (0110**b**) Default Values: 1C70**h**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0

Bits 15:0 Reserved. Must be set as shown.

Reserved

Addr: 7**h** (0111**b**) Default Values: 0000**h**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0 Reserved. Must be set as shown.

Reserved

Addr: 8**h** (1000**b**) Default Values: 0000**h**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0 Reserved. Must be set as shown.

Reserved

Addr: 9**h** (1001**b**)																Default Values: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0 Reserved. Must be set as shown.

Q-channel Offset Adjust

Addr: A**h** (0110**b**)																Default Values: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved			OS	OM(11:0)											
DV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:13 Reserved. Must be set to 0**b**.

Bit 12 OS: Offset Sign. The default setting of 0**b** incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bet to 1**b** incurs a negative offset of the set magnitude.

Bits 11:0 OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0d to 45 mV for OM(11:0) = 4095**d** in steps of -11 µV. Monotonicity is guaranteed by design only for the 9MSBs.

Code	**Offset [mV]**
0000 0000 0000 (default)	0
1000 0000 0000	22.5
1111 1111 1111	45

Q-channel Full-Scale Range Adjust

Addr: B**h** (0111**b**)																Default Values: 4000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	FM(14:0)														
DV	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15 Reserved. Must be set to 0**b**.

Bits 14:0 FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 630 mV (0**d**) to 980 mV (32767**d**) with the default setting at 820 mV (16384**d**). Monotonicity is guaranteed by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in ECM, i.e. FSR values above 820 mV. See *Table 7* for characterization details.

Code	**FSR [mV]**
000 0000 0000 0000	630
100 0000 0000 0000 (default)	820
111 1111 1111 1111	980

Aperture Delay Coarse Adjust

Addr: C**h** (1100**b**)																Default Values: 0004**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM(11:0)												STA	DCC	Reserved	
DV	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 15:4 CAM(11:0): Coarse Adjust Magnitude. This 12-bit value determines the amount of delay that will be applied to the input CLK signal. The range is 0 ps delay for CAM(11:0) = 0**d** to a maximum delay of 825 ps for CAM(11:0) = 2431**d** (±95 ps due to PVT variation) in steps of ~340 fs. For code CAM(11:0) = 2432**d** and above, the delay saturates and the maximum delay applies. Additional, finer delay steps are available in register D**h**. Either STA (Bit 3) or SA (Addr: D**h,** Bit 8) must be selected to enable this function.

Bit 3 STA: Select t_{AD} Adjust. Set this bit to 1**b** to enable the t_{AD} adjust feature. When using this feature, make sure that SA (Addr: D**h**, Bit 8) is set to 0**b**.

Bit 2 DCC: Duty Cycle Correct. This bit can be set to 0**b** to disable the automatic duty-cycle stabilizer feature of the chip. This feature is enabled by default.

Bits 1:0 Reserved. Must be set to 0**b**.

Aperture Delay Fine Adjust and LC Filter Adjust

Addr: D**h** (1101**b**)																Default Values: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FAM(5:0)						Res	SA	LCF(7:0)							
DV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:10 FAM(5:0): Fine Aperture Adjust Magnitude. This 6-bit value determines the amount of additional delay that will be applied to the input CLK when the Clock Phase Adjust feature is enabled via STA (Addr: C**h**, Bit 3) or SA (Addr: D**h**, Bit 8). The range is straight binary from 0 ps delay for FAM(5:0) = 0**d** to 2.3 ps delay for FAM(5:0) = 63**d** (±300 fs due to PVT variation) in steps of ~36 fs.

Bit 9 Reserved. Must be set to 0**b**.

Bit 8 SA: Select t_{AD} and LC filter Adjust. Set this bit to 1**b** to enable the t_{AD} and LC filter adjust features. Using this bit is the same as enabling STA (Addr: C**h**, Bit3), but also enables the LC filter to clean the clock jitter.

Bits 7:0 LCF(7:0): LC tank select Frequency. Use these bits to select the center frequency of the LC filter on the Clock inputs. The range is from 0.8 GHz (255**d**) to 1.5 GHz (0**d**). Note that the tuning range is not binary encoded, and the eight bits are thermometer encoded, i.e. the mid value of 1.1 GHz tuning is achieved with LCF(7:0) = 0000 1111**b**.

Addr: E**h** (1110**b**)																Default Values: 0003**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRC(9:0)										Res.	SP(1:0)		ES	DOC	DR
DV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits 15:6 DRC(9:0): Delay Reference Clock (9:0). These bits may be used to increase the delay on the input reference clock when synchronizing multiple ADCs. The minimum delay is 0s (0**d**) to 1000 ps (629**d**). The delay remains the maximum of 1000 ps for any codes above or equal to 639**d**.

Bit 5 Reserved. Must be set to 0**b**.

Bits 4:3 SP(1:0): Select Phase. These bits select the phase of the reference clock which is latched. The codes correspond to the following phase shift:

00 = 0°

01 = 90°

10 = 180°

11 = 270°

Bit 2 ES: Enable Slave. Set this bit to 1**b** to enable the Slave Mode of operation. In this mode, the internal divided clocks are synchronized with the reference clock coming from the master ADC. The master clock is applied on the input pins RCLK+/-. If this bit is set to 0**b**, then the device is in Master Mode.

Bit 1 DOC: Disable Output reference Clocks. Setting this bit to 0**b** sends a CLK/4 signal on RCOut1 and RCOut2. The default setting of 1**b** disables these output drivers. This bit functions as described, regardless of whether the device is operating in Master or Slave Mode, as determined by ES (Bit 2).

Bit 0 DR: Disable Reset. The default setting of 0**b** leaves the DCLK_RST functionality disabled. Set this bit to 1**b** to enable DCLK_RST functionality.

Reserved

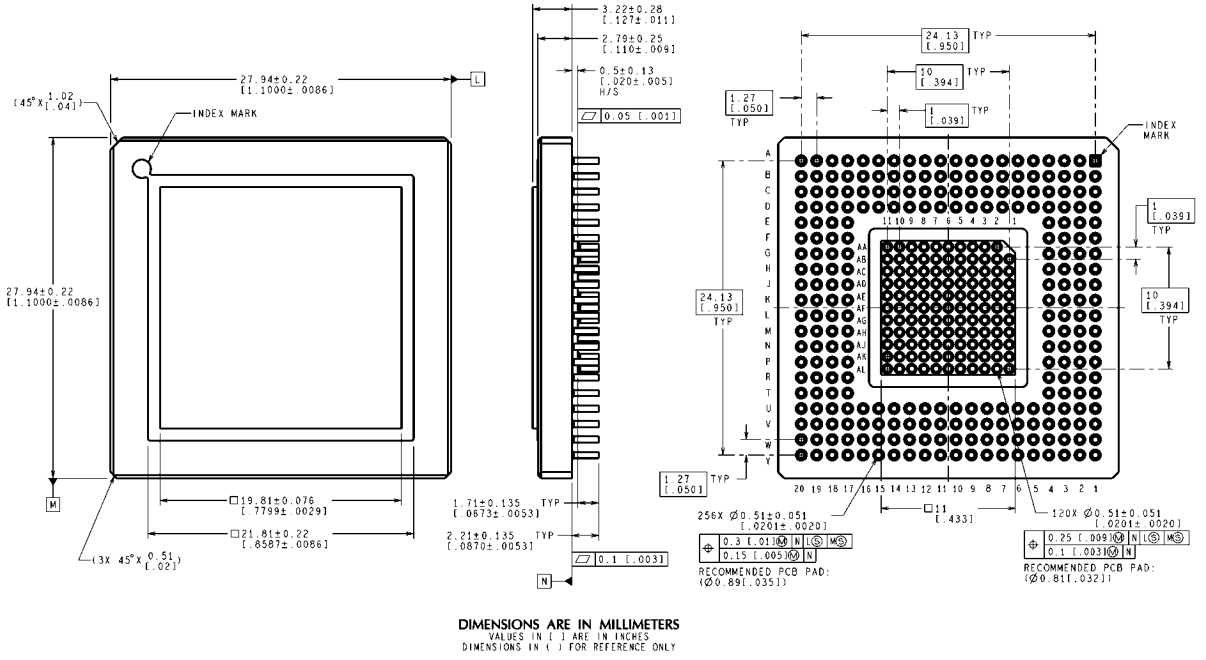
Addr: F**h** (1111**b**)																Default Values: XXXX**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved															
DV	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bits 15:0 Reserved. Do not write.

20.0 Revision History

Date Released	Revision	Section	Changes
02/11/09	A	Initial Release	New Product Data Sheet Release **(ECN SENT FOR APPROVAL 02/05/09 - Edit #: 16)**
03/18/09	B	Connection Diagram, Table 3. Section 8.0 - DCLK_RST+/- diagram, Section 18.0, paragraph 18.4.2.	Following Pin names corrected V_A, GND and GND_{DR}. Section 8.0 - Update DCLK_RST+/- diagram, Section 18.0 - paragraph added to 18.4.2 and new figure. Revision A will be Archived.
4/20/09	C	Features, Key Specifications, Table 10 Electricals.	Moved reference to radiation to Features from Key Specifications. Table 10 Electricals: V_{OH} typo limit move to Min., Added parameters V_{CMI_DRST}, V_{ID_DRST}, R_{IN_DRST}. Revision B will be Archived.
05/28/09	D	Absolute Maximum Ratings and Operating Ratings, Electrical Section Table 12, Section 19 Reserved Addr: Fh	Absolute Maximum Ratings added Voltage on V_{IN}^+, V_{IN}^-. Operating Ratings changed V_{IN}^+, V_{IN}^- Voltage Range. Range. Remove Note 10 reference from Table 12 t_{OSK}, Correction to Reserved Addr: Fh. Revision C will be Archived.
09/11/09	E	Electrical Section Table 12 Calibration (Tcal), 17.0 Section, 19.0 Section (top register 4h) Addr: 4h (0100b) POR state: DA7Fh	Added Conditions to Tcal parameter, 17.0 Section New paragraph 17.4.3.4 and renumbered, Changed table 4h and title from Reserved to Calibration Adjust in 19.0 Section. Revision D will be Archived.
05/10/2010	F	Ordering Information Table, Table 6, Table 10 Electrical Section. Sections 15.0, 17.0, 17.4.3, 19.0 Configuration Register 1 Bit 6	Added reference to MPR and CVAL NSPN. Table 6 section 1:2 Demux Non-DES Mode, Extended Control Mode, FM (14:0) = 7FFFh SNR Limit and 1:2 Demux Non-DES Mode, Non-Extended Control Mode, FSR = VA. Table 10 Digital Control Pins. Update Figure 11, Added New Figure 12 and 13, Renumbered previous Figure 12 and 13 to Figure 14 and 15 etc. Changed paragraph 17.4.3. Configuration Register 1– Bit 6 paragraph. Revision E will be Archived.

21.0 Physical Dimensions inches (millimeters) unless otherwise noted



CCC376A (Rev D)

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JEDEC REGISTRATION MS-034, VARIATION BAL-2.

376 Ceramic Column Grid Array Package
NS Package Number CCC376A

Notes

Notes

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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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