DALLAS SEMICONDUCTOR MAXIM

DS26518DK
Octal T1/E1/J1 Transceiver Demo Kit Daughter Card

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26518DK is an easy-to-use evaluation board for the DS26518 octal T1/E1/J1 transceiver. The DS26518DK is a stand-alone system. The board comes complete with a transceiver, transformers, termination resistors, configuration switches, network connectors, processor, RS-232 USB interface, and power adapter. Dallas' ChipView software gives point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status, as well as multiple clock and signal routing configurations.

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DEMO KIT CONTENTS

DS26518DK Daughter Card
5.0V Power Adapter
Coax Cable Adapters
USB Cable
CD_ROM Including:
- ChipView Software
- DS26518DK Data Sheet
- DS26518 Data Sheet

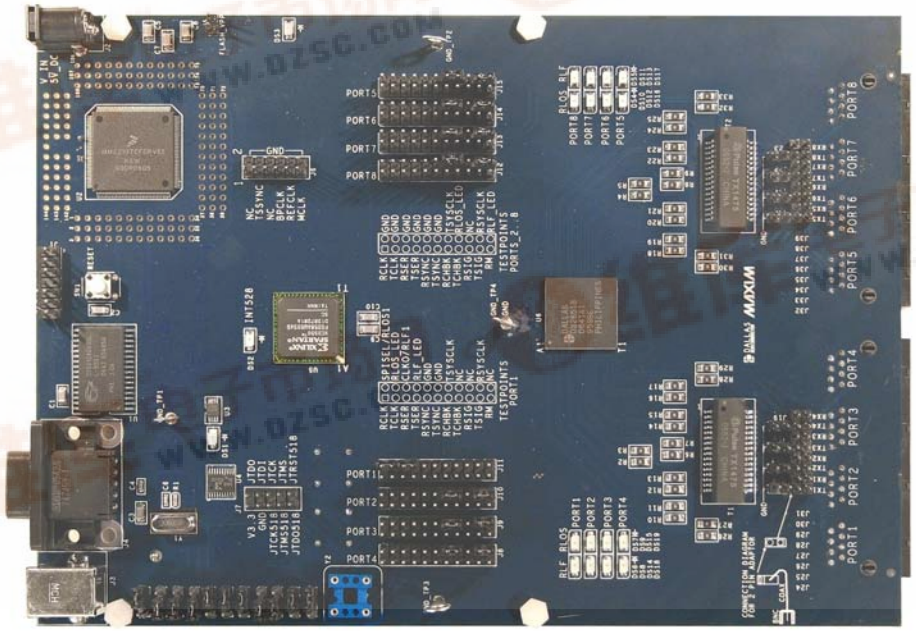
DS26518 Errata Sheet (if applicable)

FEATURES

- **Demonstrates Key Functions of DS26518 T1/E1/J1 SCT**
- **Includes Transceiver, Transformers, Network Connectors, Termination Passives and Coaxial Cables**
- **Stand-Alone Demo Kit**
- **On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS26518Register Set**
- **Software-Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing**
- **All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal and Interrupt Status as well as Indications for Multiple Clock and Signal Routing Configurations**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

ORDERING INFORMATION

PART	DESCRIPTION
DS26518DK	Demo kit daughter card for DS26518



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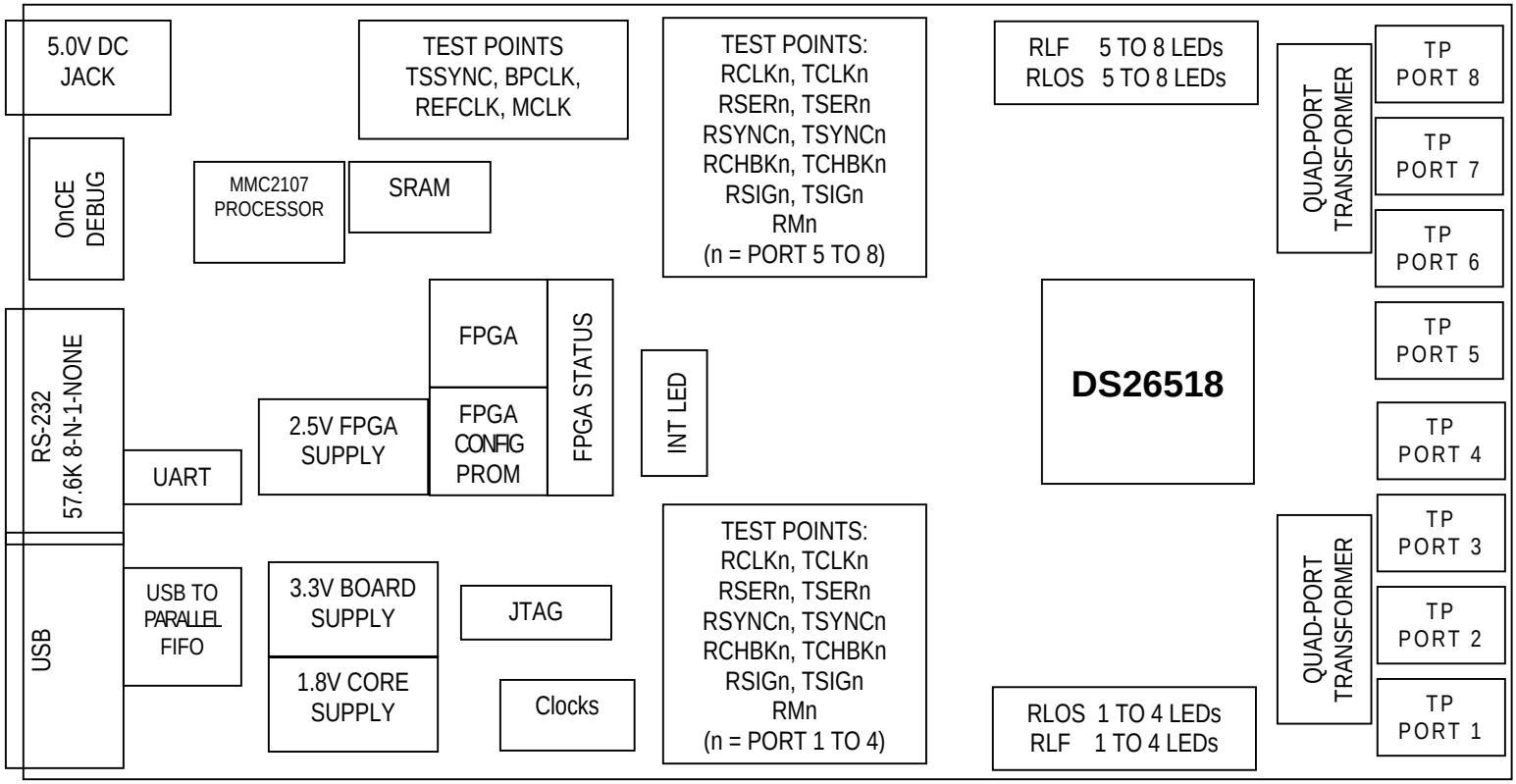
1. BOARD FLOORPLAN



2. PCB VERSIONS

There is one circuit board version for the DS26518 demo kit. The part number should read “DS26518DK01A0.”

3. PCB ERRATA

DS26518DK01A0 11/11/2006:
There are no errata for this board.

4. BASIC OPERATION

This demo kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/DS26518DK QuickView data sheet for these files.

4.1 Hardware Configuration

- Supply 5.0V to the plug-in jack.
- Configure the jumpers as detailed in Table 5-1. For quick setup steps listed below configure the device for Motorola parallel port mode (this is determined by jumpers JP1-to-JP4 and JP8, JP9).

4.1.1 General

Upon power-up, the RLOS LEDs (red) will be lit, the INT LED (red) will not be lit, and the FPGA Status LED (DS1 green) will be lit.

4.2 Quick Setup (Register View)

1) From the **Programs** menu, launch the host application named *ChipView.exe*. Run the ChipView application. If the default installation options were used, click the **Start** button on the Windows toolbar and select **Programs** → **ChipView** → **ChipView**.
2) The PC loads ChipView, offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select REGISTER VIEW.
3) The program will request a definition file. Navigate to the .def files in the T1 or E1 folder, then select the *_DS26518DK01A0_FPGA.def*. Note: Through the *Links* section, this will also load the DS26518 global .def file along with eight LIU .def files and eight framer .def files.
4) The **Register View Screen** will appear, showing the register names, acronyms, and values for the DS26518.
5) Predefined register settings for several functions are available as initialization files.
   - .ini files are loaded by selecting the menu **File→Memory Config File→Load Mfg File**.
   - Load the .mfg file *Load_AllSlices_E1_75.mfg*.
6) After loading the .mfg file, the following may be observed:
   - The DS26518 is in E1 mode and begins transmitting AIS.
   - The RLOS LEDs extinguish upon external loopback. RLF will remain lit.

4.2.1 Miscellaneous

1) Clock frequencies and port-to-port connection are provided by a register-mapped FPGA that is on the DS26518 daughter card.
2) The definition file for this FPGA is named *DS26518DC_FPGA.def*. See Table 6-2 for the FPGA register map definitions. A drop-down menu on the right of the screen allows for switching between definition files.
3) All files referenced above are available for download as described in the section marked “BASIC OPERATION.”
4) Configuration files for basic T1 BERT operation are provided in the folder named “T1_bert.”
5) SPI mode definition and configuration files are provided in the “additional_def_files” section. The DS26518 must be in SPI mode when using these files (set jumpers JP1–JP4 and JP8 per Table 5-1).

6) Files with DS26518 annotations are provided in the “additional_def_files” section. These files indicate bit level differences between the DS26518 and the DS26518. In these files the DS26518 bit name is provided in parentheses, followed by the DS26518 bit name.

5. TEST POINTS AND CONNECTORS

The DS26518DK has several connectors, test points, oscillators, and jumpers. Table 5-1 provides a description of these signals, given approximately in order of appearance on the PCB, from left to right then top to bottom (with the board held so that the RS-232 connector is on the top edge).

Jumpers JP1 to JP11 do not have a pin 1 identifier on the top of the PCB. For these jumpers pin1 is identified by the square pad that is visible on the PCB’s solder side. JP1 to JP11 pin 1 is on the left side of the PCB when the board is held so that the RS-232 connector is on the top edge.

Table 5-1. Test Points and Connectors

SILKSCREEN REFERENCE	FUNCTION	DEFAULT SETTING	SCHEMATIC PAGE	DESCRIPTION
J3	USB Connector	User Decision	16	Used for Communication with Host PC. When USB is used, the RS-232 port should not be used. Drivers for the USB device are provided on the CD that ships with the demo kit.
J02	RS-232 Connector	Connected to Host PC	16	Used for Communication with Host PC. Basic setting is 57.6K baud, 8 bits, no stop bit, 1 parity bit (57.6, 8, N, 1). When RS-232 is used, the USB port should not be used.
J1	OnCe BDM Connector	—	16	OnCE Debug Connector for MMC2107 Processor
J2	Power Supply V_{DD}	5.0V	17	System V_{DD}. Always connected to power supply.
SW1	System Reset	—	15	System Reset. Connects to all device reset pins.
JP1	CS Selection	Jumpered Pins 2+3	2	DS26518 Chip-Select Selection. Pins 2+3 are used for parallel port mode. Pins 1+2 are used for SPI mode.
JP2	D0/MISO Selection	Jumpered Pins 1+2	2	DS26518 Data Bus Configuration. Used to select between data bit 0 (pins 1+2) and SPI MISO (pins 2+3).
JP3	D1/MOSI	Jumpered Pins 1+2	2	DS26518 Data Bus Configuration. Used to select between data bit 1 (pins 1+2) and SPI MOSI (pins 2+3).
JP4	D2/SPICK	Jumpered Pins 1+2	2	DS26518 Data Bus Configuration. Used to select between data bit 2 (pins 1+2) and SPI SCK (pins 2+3).
JP5	SPI SWAP Bias	Jumpered Pins 2+3	9	DS26518 SPI SWAP (only relevant in SPI mode). Pull high to match processor defaults.
JP6	SPI CPHA Bias	Jumpered Pins 2+3	9	DS26518 SPI Clock Phase (only relevant in SPI mode). Pull to the same value as SPI_CPOL to match processor defaults.
JP7	SPI CPOL Bias	Jumpered Pins 2+3	9	DS26518 SPI Clock Polarity (only relevant in SPI mode). Pull to the same value as SPI_CPHA to match processor defaults.
JP8	SPI SEL Bias	Jumpered Pins 1+2	9	DS26518 SPI/Parallel Port Selection. Pins 1+2 are used for parallel port, pins 2+3 are used for SPI mode.
JP9	BTS Bias	Jumpered Pins 2+3	9	DS26518 Bus Type Selection. High for Motorola mode.

SILKSCREEN REFERENCE	FUNCTION	DEFAULT SETTING	SCHEMATIC PAGE	DESCRIPTION
JP10	TXENABLE	Jumpered Pins 2+3	9	DS26518 Transmit Enable. Low for tri-state.
JP11	DIGIO ENABLE	Jumpered Pins 2+3	9	DS26518 Digital I/O Enable. Low for tri-state.
DS1	CFG OK	On (Green)	12	System Configuration LED. On when the system has been successfully configured.
J5	Flash VPP	Not Installed		Flash VPP Jumper. Installed during erase and program of the MMC2107
J7	JTAG testpoints	—	13	Test Points for DS26518 JTAG. Here the DS26518 is the only device in the chain. JTAG for the FPGA is provided on the same connector to facilitate chain concatenation.
DS2	INT DS26518	Off (Not Red)	12	DS26518 Interrupt Status LED. On when the DS26518 interrupt is active.
J6	TestPoints	—	10	DS26518 Test Points for TSSYNC, BPCLK, REFCLK and MCLK
DS3	LED	On (Green)		Power OK LED
Y2	Oscillator	Not Populated	12	Spare Oscillator
YB2 (bottom side)	Oscillator	16.348MHz	12	Provides E1 Base Rate. The FPGA divides this clock by 8 to obtain 2.048MHz.
YB1 (bottom side)	Oscillator	1.544MHz	12	Provides T1 Base Rate
J8, J9, J10, J12, J13, J14, J15	Test Points Ports 2 to 8	—	10, 11	DS26518 Test Points for RCLK, TCLK, RSER, TSER, RSYNC, TSYNC, RCHBK, TCHBK, RSIG, TSIG, RM, TSYSCLK, RLOS, RSYSCLK, RLF_LED
J11	Test Points Port 1	—	10	DS26518 Test Points. Similar to the test points for ports 2 to 8. Several pins for port 1 have functions slightly different than the other ports. These pins are: AL_FLOS, RLOS, RLF_LTC, TSYSCLK, RSYSCLK.
DS6, DS8, DS14, DS18, DS5, DS11, DS13, DS17	LED	(Red)	10	DS26518 RLF LEDs
DS7, DS9, DS15, DS19, DS4, DS10, DS12, DS16	LED	(Red)	10	DS26518 RLOS LEDs
J16 to J23	Jumper GND	Not installed	5 to 8	DS26518 Transmit Ground Strap. Used to ground the TRING side of TTIP/TRING. Used for E1 mode with BNC connectors.
J24 to J39	TIP/RING Jumper	Coax Connector	5 to 8	DS26518 Test Points for TTIP/TRING and RTIP/RRING. A custom 2-pin to BNC cable is provided for this connection.
JB1, JB2 (bottom side)	RJ45	RJ45	5 to 8	DS26518 RJ45 connectors

6. ADDRESS MAP

Address space begins at 0x81000000. All offsets given in the following tables are relative to 0x81000000.

Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named “DS26518DC_FPGA.def.”

Table 6-1. Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Board Identification and Clock/Signal Routing
0X4000 to 0X40EF	DS26518	DS26518 Framer 1 Rx Registers
0X40F0 to 0X40FF	DS26518	DS26518 Global Registers
0X4100 to 0X41EF	DS26518	DS26518 Framer 1 Tx Registers
0X41F0 to 0X41FF	DS26518	DS26518 Reserved Registers
0X4200 to 0X4FFF	DS26518	DS26518 Framer 2 to 8 Registers
0X5000 to 0X50FF	DS26518	DS26518 LIU 1 to 8 Registers
0X5100 to 0X517F	DS26518	DS26518 BERT 1 to 8 Registers
0X5180 to 0X5FFF	DS26518	DS26518 Reserved Registers

6.1 SPI Mode

The DS26518 addresses shown in Table 6-1 are for parallel port mode. When SPI mode is selected the DS26518 base address begins at 0x00. For SPI mode ChipView requires a separate set of definition files, which are provided along with the def files for parallel port mode. Table 5-1 details the default bias levels for SPI configuration pins. To change these settings, the processor’s SPI settings must also change. The processor SPI settings can be changed in ChipView’s terminal mode using the **SPISG S** function.

6.2 FPGA Register Map

Table 6-2. FPGA Register Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	CSR	Control	DS26518 MCLK and REFCLKIO Source
0X0012 0X0022 0X0032 0X0042 0X0052 0X0062 0X0072 0X0082	SYSCLK_TRn (n = 8 to 1)	Control	DS26518 Tx and Rx SYSCLK Source, Ports 8 to 1
0X0013	SYNCTSS	Control	DS26518 TSSYNC Source

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0014 0X0024 0X0034 0X0044 0X0054 0X0064 0X0074 0X0084	TCSRn (n = 8 to 1)	Control	DS26518 TCLK Source, Ports 8 to 1
0X0015 0X0025 0X0035 0X0045 0X0055 0X0065 0X0075 0X0085	TSYNCSn (n = 8 to 1)	Control	DS26518 TSYNC Source, Ports 8 to 1
0X0016 0X0026 0X0036 0X0046 0X0056 0X0066 0X0076 0X0086	RSYNCSRn (n = 8 to 1)	Control	DS26518 RSYNC Source Select, Ports 8 to 1
0X0017 0X0027 0X0037 0X0047 0X0057 0X0067 0X0077 0X0087	TSERSRn (n = 8 to 1)	Control	DS26518 TSER Source, Ports 8 to 1

6.3 ID Registers

BID: BOARD ID (Offset = 0X0000)

BID is read-only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read-only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read-only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read-only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read-only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read-only and displays the current assembly revision.

PREV: PLD REVISION (Offset = 0X0007)

PREV is read-only and displays the current PLD firmware revision.

6.4 Control Registers

Register Name: **CSR**
Register Description: **DS26518 MCLK and REFCLKIO Source**
Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	RCSRC1	RCSRC0	—	—	—	—	MSRC1	MSRC0
Default	1	1	—	—	—	—	0	1

Bits 7 and 6: DS26518 REFCLKIO Source (RCSRC[1:0]). REFCLKIO connection is defined in Table 6-3.

Bits 1 and 0: DS26518 MCLK Source (MSRC[1:0]. MCLK connection is defined in Table 6-4.

Table 6-3. REFCLKIO Source Definition

RCSRC[1: 0]	REFCLKIO CONNECTION
00	Drive REFCLKIO with 1.544MHz clock.
01	Drive REFCLKIO with 2.048MHz clock.
1x	Tri-state REFCLKIO.

Table 6-4. MCLK Source Definition

MSRC[1:0]	MCLK CONNECTION
00	Drive MCLK with 1.544MHz clock.
01	Drive MCLK with 2.048MHz clock.
1x	Tri-state MCLK.

Register Name: **SYSCLK_TR**
Register Description: **DS26518 TSYSCLK and RSYSCLK Source**
Register Offset: **0x0012, 0x0022, 0x0032, 0x0042, 0x0052, 0x0062, 0x0072, 0x0082**

Bit #	7	6	5	4	3	2	1	0
Name	RT	RS1	RS0	—	—	TT	TS1	TS0
Default	0	1	0	—	—	0	0	1

Bits 7 to 5: DS26518 Port 4 RSYSCLK Source (RT, RS[1:0]). The source for RSYSCLK is defined as shown in Table 6-5.

Bits 2 to 0: DS26518 Port 1 TSYSCLK Source (TT, TS[1:0]). The source for TSYSCLK is defined as shown in Table 6-6.

Table 6-5. RSYSCLK Source Definition

RT, RS[1:0]	RSYSCLK CONNECTION
1xx	Tri-state RSYSCLK.
000	Drive RSYSCLK with 1.544MHz clock.
001	Drive RSYSCLK with 2.048MHz clock.
010	Drive RSYSCLK with 8.192MHz clock.
011	Drive RSYSCLK with DS26518 port BPCLK.

Table 6-6. TSYSCLK Source Definition

TT, TS[1:0]	TSYSCLK CONNECTION
1xx	Tri-state TSYSCLK.
000	Drive TSYSCLK with 1.544MHz clock.
001	Drive TSYSCLK with 2.048MHz clock.
010	Drive TSYSCLK with 8.192MHz clock.
011	Drive TSYSCLK with DS26518 port BPCLK.

Register Name: **SYNCTSS**
Register Description: **DS26518 TSSYNC Source**
Register Offset: **0x0013**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TSRC3	TSRC2	TSRC1	TSRC0
Default	—	—	—	—	0	0	0	0

Bit 3 to 0: DS26518 TSSYNC Source Select (TSRC[3:0]). The source for TSSYNC is defined in Table 6-7.

Table 6-7. TSSYNC Source Definition

TSRC[3:0]	TSSYNC SOURCE DEFINITION
0000	Not using transmit-side elastic store, tri-state FPGA pin connected to TSSYNC (weak pulldown).
0001	Drive TSSYNC with RSYNC1.
0010	Drive TSSYNC with RSYNC2.
0011	Drive TSSYNC with RSYNC3.
0100	Drive TSSYNC with RSYNC4.
0101	Drive TSSYNC with RSYNC5.
0110	Drive TSSYNC with RSYNC6.
0111	Drive TSSYNC with RSYNC7.
1000	Drive TSSYNC with RSYNC8.

Note: When driving TSSYNC with RSYNCx, the corresponding DS26518 port should be configured such that RSYNCx is an output (RIOCR.2 = 0).

Register Name: **TCSRn (n = 8 to 1)**
Register Description: **DS26518 TCLK Source Ports 8–1**
Register Offset: **0x0014, 0x0024, 0x0034, 0x0044, 0x0054, 0x0064, 0x0074, 0x0084**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TDS3	TDS2	TDS1	TDS0
Default	—	—	—	—	*See note*	*See note*	*See note*	*See note*

Bits 3 to 0: DS26518 Port 1 TCLK Source (TDS[3:0]). The source for TCLKx is shown in Table 6-8.

Table 6-8. TCLKx Source Definition

TDS[3:0]	TCLKx SOURCE DEFINITION
0000	Tri-state TCLKx.
0001	Drive TCLKx with RCLK1.
0010	Drive TCLKx with RCLK2.
0011	Drive TCLKx with RCLK3.
0100	Drive TCLKx with RCLK4.
0101	Drive TCLKx with RCLK5.
0110	Drive TCLKx with RCLK6.
0111	Drive TCLKx with RCLK7.
1000	Drive TCLKx with RCLK8.
1001	Drive TCLKx with the 1.544MHz clock.
1010	Drive TCLKx with the 2.048MHz clock.

Note: Initial values are such that TCLK1←RCLK1, TCLK2←RCLK2, TCLK3←RCLK3, TCLK4←RCLK4, TCLK5←RCLK5, TCLK6←RCLK6, TCLK7←RCLK7, TCLK8←RCLK8, which corresponds to address 0x14 = 0b0001, address 0x24 = 0b0010, address 0x34 = 0b0011, address 0x44 = 0b0100, address 0x54 = 0b0101, address 0x64 = 0b0110, address 0x74 = 0b0111 and address 0x84 = 0b1000.

Register Name: **TSYNCSn (n = 8 to 1)**
Register Description: **DS26518 TSYNC Source Ports 8 to 1**
Register Offset: **0x0015, 0x0025, 0x0035, 0x0045, 0x0055, 0x0065, 0x0075, 0x0085**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TSRC3	TSRC2	TSRC1	TSRC0
Default	—	—	—	—	0	0	0	0

Bits 3 to 0: DS26518 Port 1 TSYNC Source (TSRC[3:0]). The source for TSYNCx is shown in Table 6-9.

Table 6-9. TSYNCx Source Definition

TSRC[3:0]	TSYNCx SOURCE DEFINITION
0000	Tri-state TSYNCx.
0001	Drive TSYNCx with RSYNC1.
0010	Drive TSYNCx with RSYNC2.
0011	Drive TSYNCx with RSYNC3.
0100	Drive TSYNCx with RSYNC4.
0101	Drive TSYNCx with RSYNC5.
0110	Drive TSYNCx with RSYNC6.
0111	Drive TSYNCx with RSYNC7.
1000	Drive TSYNCx with RSYNC8.

Note: When driving TSYNCx with RSYNCx, the corresponding DS26518 port should be configured such that TSYNCx is an input (TIOCR.2 = 0) and RSYNCx is an output (RIOCR.2 = 0).

Register Name: **RSYNC3Rn (n = 8 to 1)**
Register Description: **DS26518 RSYNC Source Select, Ports 8 to 1**
Register Offset: **0x0016, 0x0026, 0x0036, 0x0046, 0x0056, 0x0066, 0x0076, 0x0086**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	RIO3	RIO2	RIO1	RIO0
Default	—	—	—	—	0	0	0	0

Bits 3 to 0: DS26518 Port 1 RSYNC Source (RIO[3:0]). The source for RSYNCx is shown in Table 6-10.

Table 6-10. RSYNCx Source Definition

RIO[3:0]	RSYNCx SOURCE DEFINITION
0000	Tri-state RSYNCx.
0001	Drive RSYNCx with RSYNC1.
0010	Drive RSYNCx with RSYNC2.
0011	Drive RSYNCx with RSYNC3.
0100	Drive RSYNCx with RSYNC4.
0101	Drive RSYNCx with RSYNC5.
0110	Drive RSYNCx with RSYNC6.
0111	Drive RSYNCx with RSYNC7.
1000	Drive RSYNCx with RSYNC8.

Note: When driving RSYNCy with RSYNCx, the corresponding DS26518 port should be configured such that RSYNCx is an output (RIOCR.2 = 0) and RSYNCy is an input (RIOCR.2 = 1).

Register Name: **TSERSR[n] (n = 8 to 1)**
Register Description: **DS26518 TSER Source, Ports 8 to 1**
Register Offset: **0x0017, 0x0027, 0x0037, 0x0047, 0x0057, 0x0067,0x0077, 0x0087**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TS3	TS2	TS1	TS0
Default	—	—	—	—	*See note*	*See note*	*See note*	*See note*

Bits 3 to 0: DS26518 Port 1 TSER Source (TS[3:0]). The source for TSERx is shown in Table 6-11.

Table 6-11. TSERx Source Definition

TS[3:0]	TSERx SOURCE DEFINITION
0000	Tri-state TSERx.
0001	Drive TSERx with RSER1.
0010	Drive TSERx with RSER2.
0011	Drive TSERx with RSER3.
0100	Drive TSERx with RSER4.
0101	Drive TSERx with RSER5.
0110	Drive TSERx with RSER6.
0111	Drive TSERx with RSER7.
1000	Drive TSERx with RSER8.
1001	Drive TSERx low.

Note: Initial values are such that TSER1←RSER1, TSER2←RSER2, TSER3←RSER3, TSER4←RSER4, TSER5←RSER5, TSER6←RSER6, TSER7←RSER7, TSER8←RSER8, which corresponds to address 0x17 = 0b0001, address 0x27 = 0b0010, address 0x37 = 0b0011, address 0x47 = 0b0100, address 0x57 = 0b0101, address 0x67 = 0b0110, address 0x77 = 0b0111 and address 0x87 = 0b1000.

6.5 FPGA Control Examples

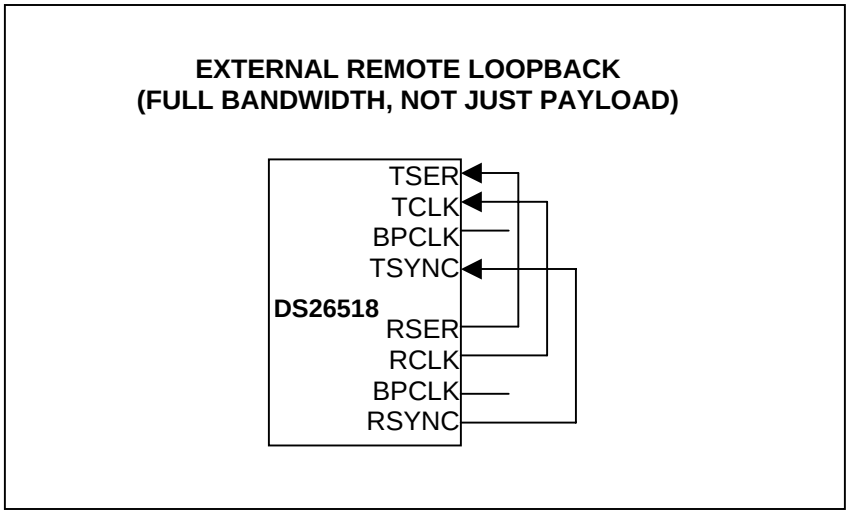


Table 6-12. FPGA Configuration (Port 1, T1 Mode)

REGISTER NAME	SETTING	COMMENT
CSR	0X01	Drive DS26518 MCLK with 2.048MHz.
TCSR1	0X01	Drive TCLK1 with RCLK1.
SYSCLK_TR	0X00	Drive TSYSCLK with 1.544MHz.
TSYNCS1	0X01	Drive TSYNC1 with RSYNC1.
SYNCTSS	0X01	Drive TSSYNC with RSYNC1.
RSYNCSRN	0X00	Tri-state FPGA driver pin for DS26518 RSYNC.
TSERSR1	0X01	Drive DS26518 TSER1 with data from RSER1.

Table 6-13. DS26518 Partial Configuration (Port 1, T1 Mode)

REGISTER NAME	SETTING	COMMENT
RIOCR	RSIO = 0	RSYNC is an output.
TIOCR	TSIO = 0	TSYNC is an input.
TESCR	TESE = 0	Bypass Rx and Tx elastic stores.
RESCR	RESE = 0	
TCR3	TCSS1 = 0	TCLK is driven by TCLK pin.
	TCSS2 = 0	

7. ADDITIONAL INFORMATION/RESOURCES

7.1 DS26518 Information

For more information about the DS26518, refer to the DS26518 data sheet at www.maxim-ic.com/DS26518.

7.2 DS26518DK Information

For more information about the DS26518DK including software downloads, refer to the DS26518DK Quick View page at www.maxim-ic.com/DS26518DK.

7.3 Technical Support

For additional technical support, go to www.maxim-ic.com/support.

8. COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C2, C9, C10, CB1, CB3, CB5, CB6, CB7, CB10–CB14, CB16, CB18, CB20–CB23, CB25, CB26, CB29–CB32, CB34, CB49, CB52, CB53, CB54, CB56–CB63, CB70, CB74, CB75, CB76, CB79, CB80, CB88, CB89, CB100, CB101	49	1µF ±10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C3, C5, C7, C8, CB19, CB35, CB36, CB37, CB47, CB50, CB51, CB55, CB64, CB65, CB66, CB68, CB71, CB102, CB103	19	10µF ±20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
C4	1	0.01µF ±10%, 50V X7R ceramic capacitor (0603)	AVX	06035C103KAT
C6, CB24, CB27, CB38-CB45, CB48, CB67, CB72, CB73, CB77, CB78, CB81-CB87	24	0.1µF ±20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
CB15, CB17	2	22pF ±5%, 25V NPO ceramic capacitors (0603)	AVX	06033A220JAT
CB2, CB28, CB46, CB69	4	68µF ±20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
CB4, CB33	2	68µF ±20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
CB8, CB9	2	10pF ±5%, 50V ceramic tall-case capacitors (1206)	Phycomp	1206CG100J9B200
CB90–CB97	8	0.1µF ±10%, 25V ceramic capacitors (1206)	Panasonic	ECJ-3VB1E104K
CB98, CB99, CB104–CB109	8	560pF ±5%, 50V ceramic capacitors (1206)	AVXZ	12065A561JAT2A
DB1	1	1A, 40V Schottky diode	International Rectifier	10BQ040
DS1, DS3	2	Green SMD LEDs	Panasonic	LN1351C
DS2, DS4–DS19	17	Red SMD LEDs	Panasonic	LN1251C
GND_TP1–GND_TP4, GND_TPB1	5	Standard ground clips	Keystone	4954
H1–H4	4	4-40 hardware, 0.50 Nylon standoff and Nylon hex-nut	NA	4-40KIT4
J1	1	100-mil, 2-7 position jumper	NA	NA
J2	1	2.1mm/5.5mm powerjack right-angle PCB, closed frame, high current 24V DC at 5A	Digi-Key	CP-002AH-ND
J3	1	Black Type B, single, right angle jumper	Molex	NA
J4	1	DB9 right-angle connector (long case)	AMP	747459-1
J5, J16–J23	9	100-mil, 2-position jumpers	NA	NA
J6	1	12-pin, dual-row, vertical connector	NA	NA
J7	1	Terminal strip (10-pin, dual-row, vertical)	Samtec	TSW-105-07-T-D
J8–J15	8	22-pin, dual-row, vertical headers	Samtec	HDR-TSW-111-14-T-D
J24–J39	16	2-pin headers, 0.100 centers, vertical	Samtec	TSW-102-07-T-S
JB1, JB2	2	Right-angle RJ45 8-pin, 4-port jacks	Molex	43223-8140
JP1–JP11	11	100-mil 3-position jumpers	NA	NA

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R1	1	470Ω ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ471V
R2–R33	32	0Ω ±5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
RB1, RB3–RB6, RB10, RB12, RB13, RB16, RB18, RB19, RB21–RB24, RB26, RB27, RB30, RB41	19	10kΩ ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
RB2	1	30Ω ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ300V
RB7	1	1.0MΩ ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ105V
RB8, RB9	2	27Ω ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ270V
RB11	1	0Ω ±5%, 1/8W resistor (1206)	Panasonic	ERJ-8GEYJ0R00V
RB14, RB17, RB32	3	1.0kΩ ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ102V
RB15	1	1.5kΩ ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ152V
RB20, RB29, RB31, RB33, RB36, RB39, RB42, RB43	9	1.0kΩ ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ102V
RB25	1	10.0kΩ ±1%, 1/16W resistor (0603)	Panasonic	ERJ-3EKF1002V
RB28, RB35, RB44–RB59	18	330Ω ±5%, 1/10W resistors (0805)	Panasonic	ERJ-6GEYJ331V
RB34	1	330Ω ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ331V
RB37	1	330Ω ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ331V
RB38, RB40	2	0.0Ω ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEY0R00V
RB60–RB75	16	61.9Ω ±1%, 1/8W (resistors (1206)	Panasonic	ERJ-8ENF61R9V
SW1	1	4-pin single-pole switch	Panasonic	EVQPAE04M
T1, T2	2	SMT 32-pin transformers Transmit/receive 1:2 and 1:1	Pulse	TX1475
U1, UB2	2	Cypress SRAM, Lab Stock	NA	NA
U2	1	MMC2107 Processor	Motorola	MMC2107
U3	1	8-Pin μMAX/SO 2.5V or Adj	Maxim	MAX1792EUA25
U4	1	1Mb flash-based configuration mem	Xilinx	XCF01SV020C
U5	1	Xilinx Spartan 2.5V FPGA, 256-pin BGA	Xilinx	XC2S50-5FG256C
U6	1	8-port T1/E1/J1 transceiver, -40°C to +85°C, 256-pin TE-CSBGA	Dallas Semiconductor	DS26518
UB1	1	MAX3233E UART	Maxim	MAX3233E
UB3, UB5	2	Linear regulator 1.5W, 3.3V or Adj, 1A, 16-pin TSSOP-EP	Maxim	MAX1793EUE-33
UB4	1	USB UART (USB: 8-bit FIFO), 32-pin LQFP	FTD	FT245BM
UB6	1	Linear regulator 1.5W, 1.8V or Adj, 1A, 16-pin TSSOP-EP	Maxim	MAX1793EUE-18
XB1	1	Low-profile 8.0MHz crystal	ECL	EC1-8.000M
Y1	1	Low-profile 6.00MHz crystal	Pletronics	LP49-26-6.00M
Y2	1	Oscillator, crystal clock (3.3V socket)	SaRonix	NA
YB1	1	Oscillator, crystal clock (3.3V, 1.544MHz)	SaRonix	NTH039A3-1.5440
YB2	1	Oscillator (4-pin half-size; 16.348MHz, 50ppm)	SaRonix	NCH069B3-16.348

9. SCHEMATICS

The schematics are featured in the following pages.

DS26518

OCTAL T1/E1/J1 TRANSCEIVER

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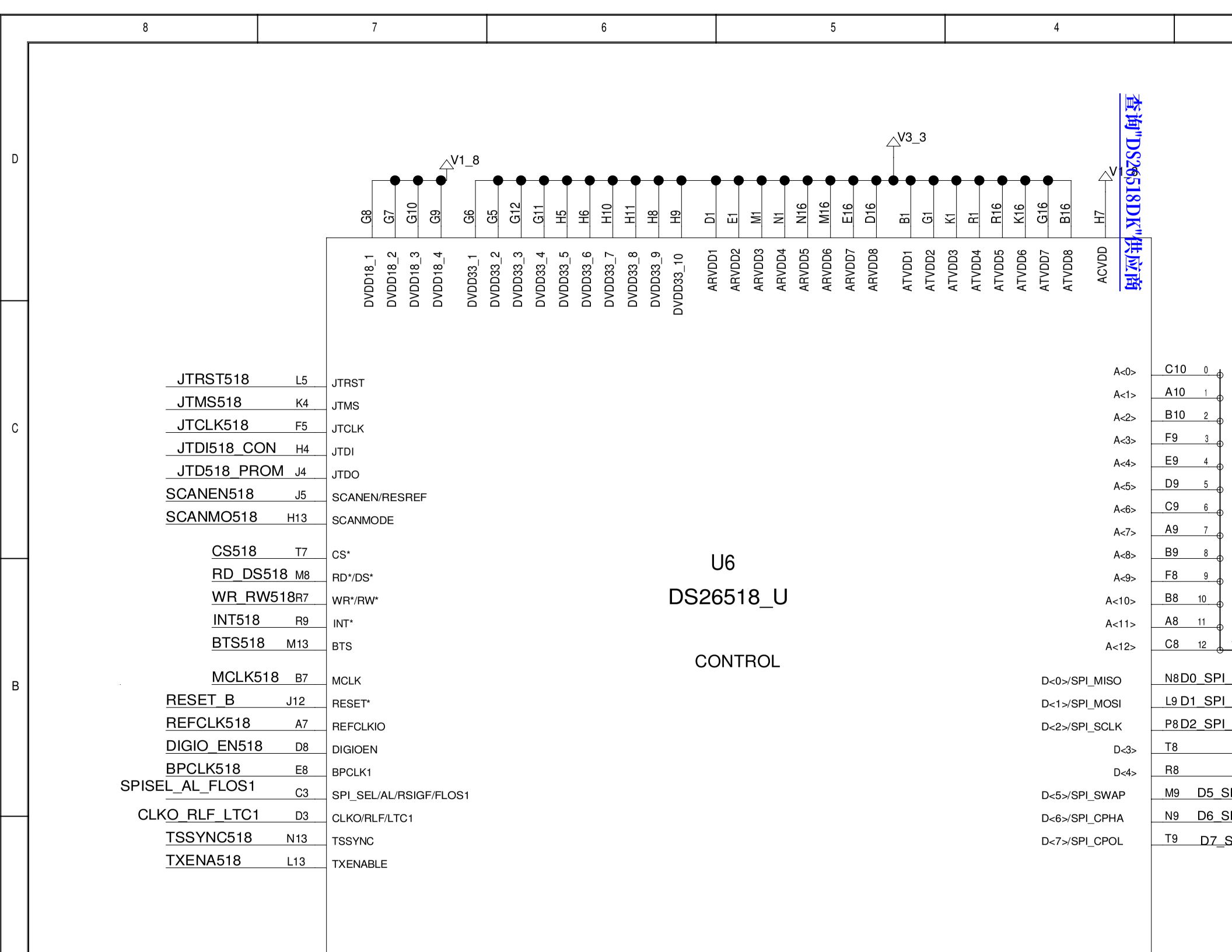
8. DS26518 BNC / XFRM 7-8
9. FPGA (SIGNAL MUX)
10. DS26518 TEST POINTS
11. DS26518 TEST POINTS
12. FGPA ADDRESS DATA BUS
13. FGPA CONFIGURATION / JTAG PORT
14. MICROPROCESSOR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JTMS518 K4 JTMS
JTCLK518 F5 JTCLK
JTDI518_CON H4 JTDI
JTD518_PROM J4 JTDO
SCANEN518 J5 SCANEN/RESREF
SCANMO518 H13 SCANMODE
CS518 T7 CS*
RD_DS518 M8 RD*/DS*
WR_RW518 R7 WR*/RW*
INT518 R9 INT*
BTS518 M13 BTS
MCLK518 B7 MCLK
RESET_B J12 RESET*
REFCLK518 A7 REFCLKIO
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BPCLK518 E8 BPCLK1
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CLKO_RLF_LTC1 D3 CLKO/RLF/LTC1
TSSYNC518 N13 TSSYNC
TXENA518 L13 TXENABLE
U6
DS26518_U
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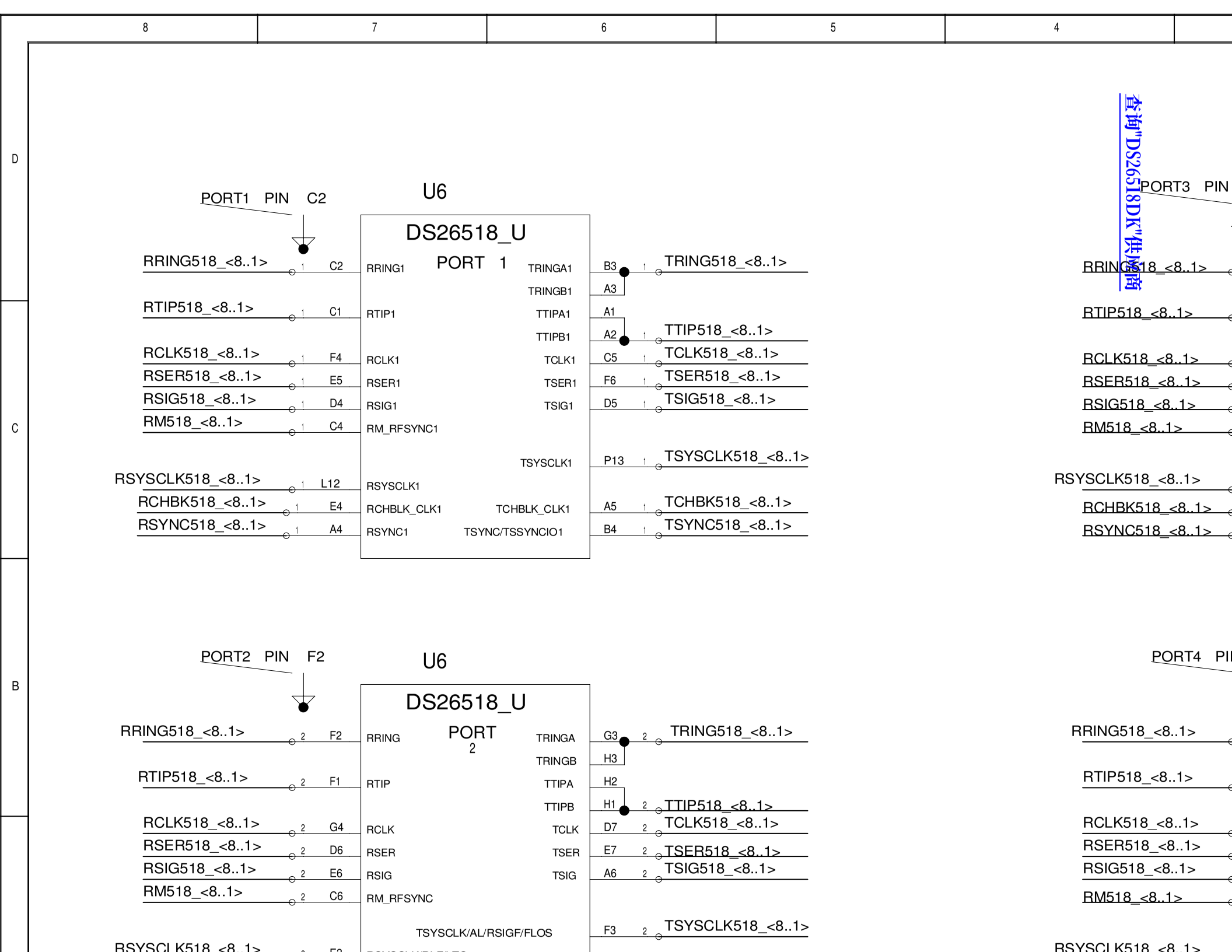
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E6
C6
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RSIG
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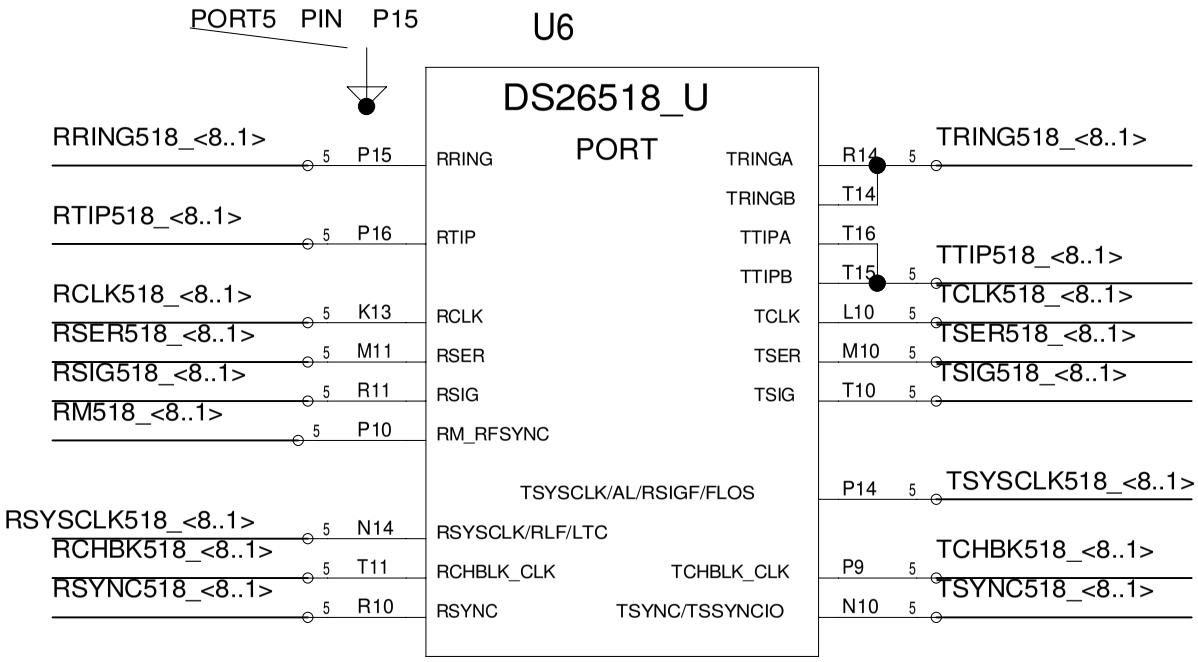
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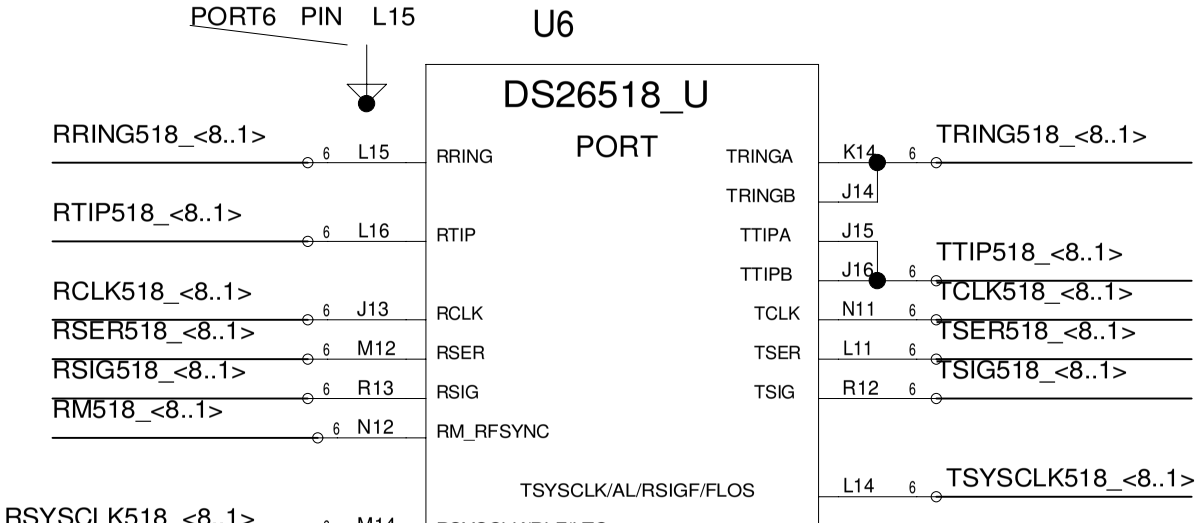
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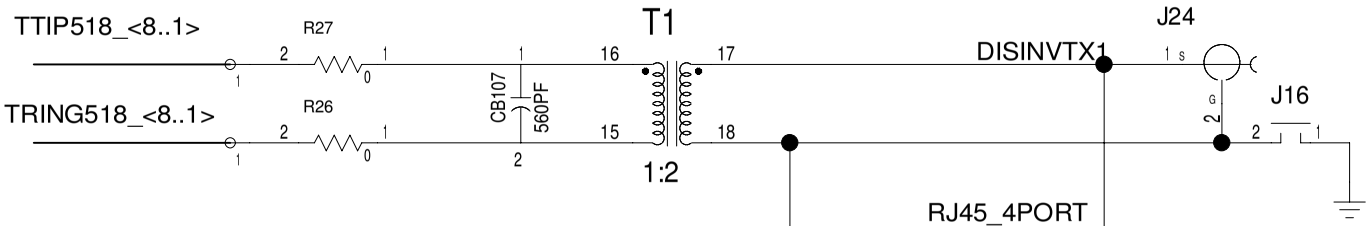

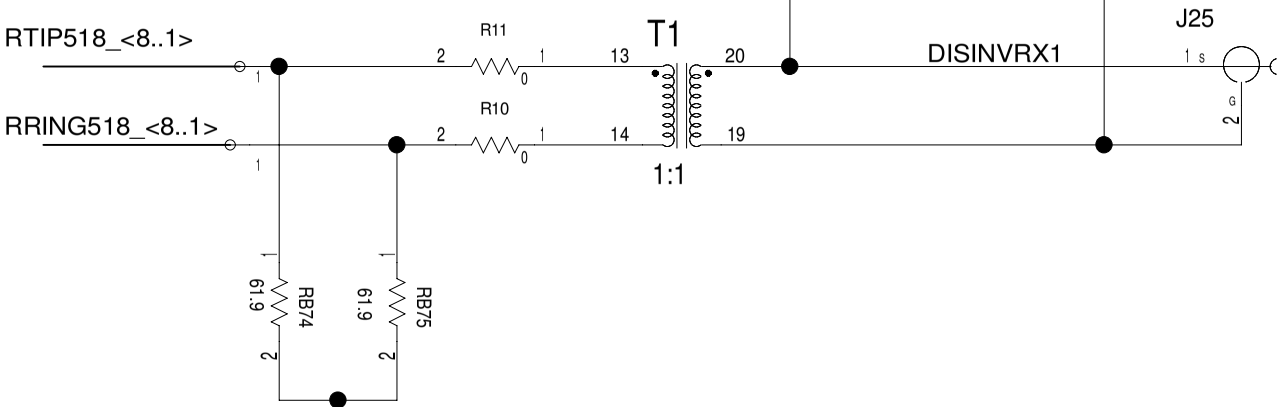

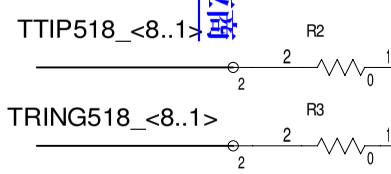

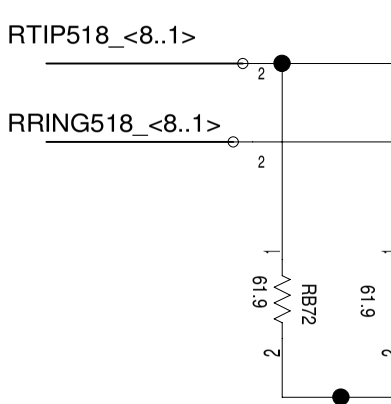

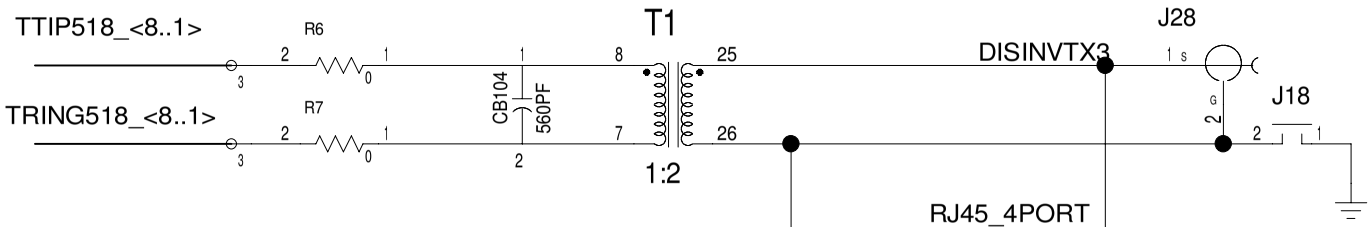

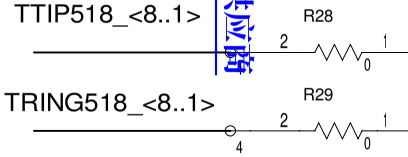

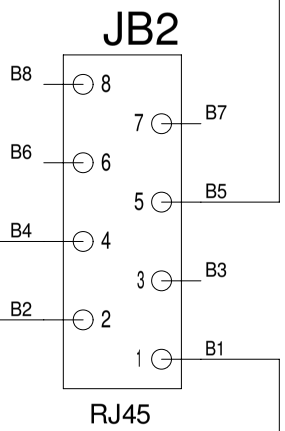

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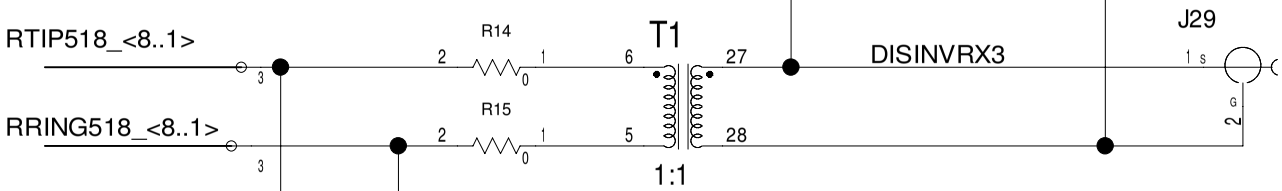

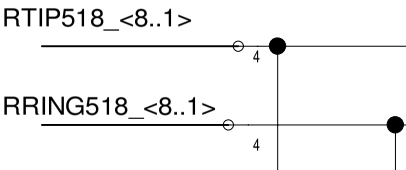

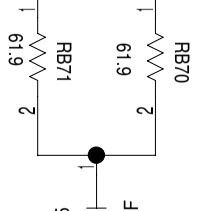

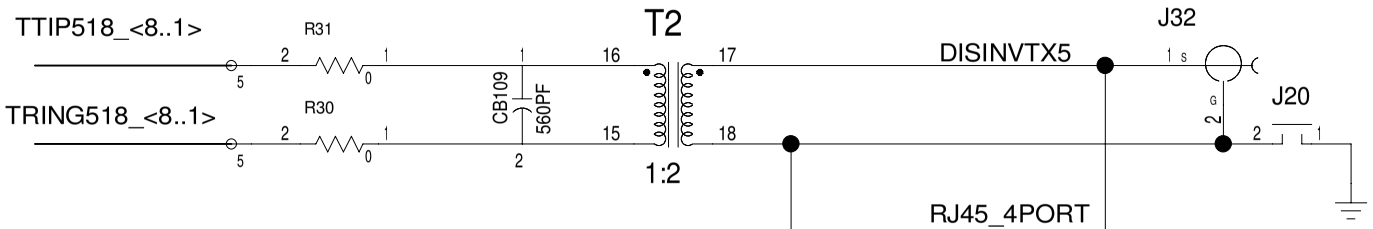

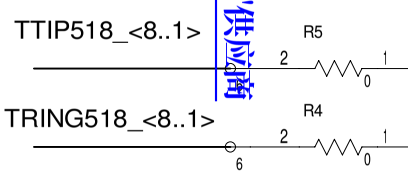

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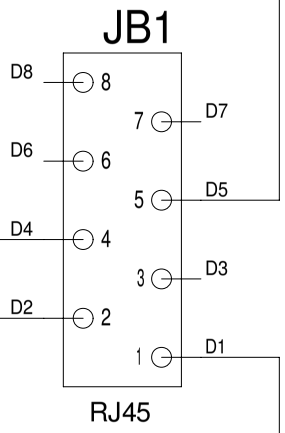
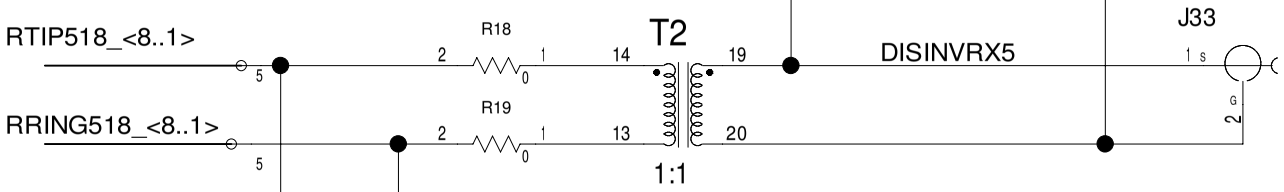
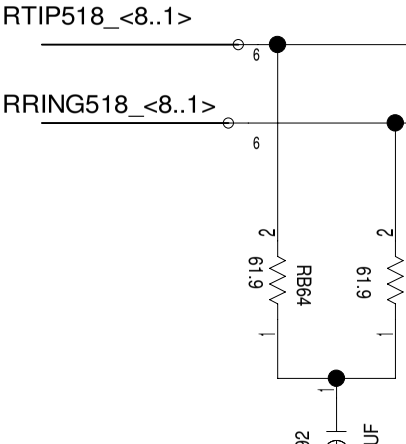
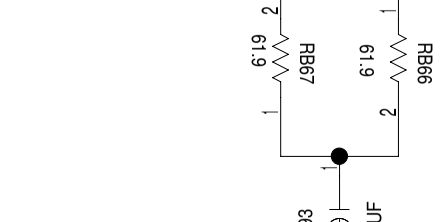
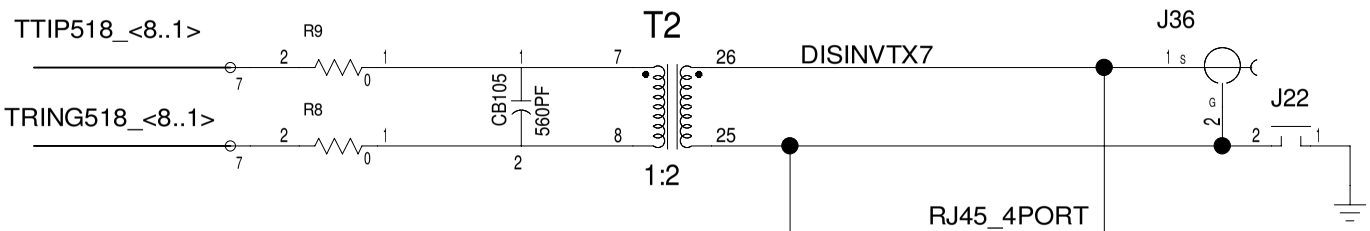
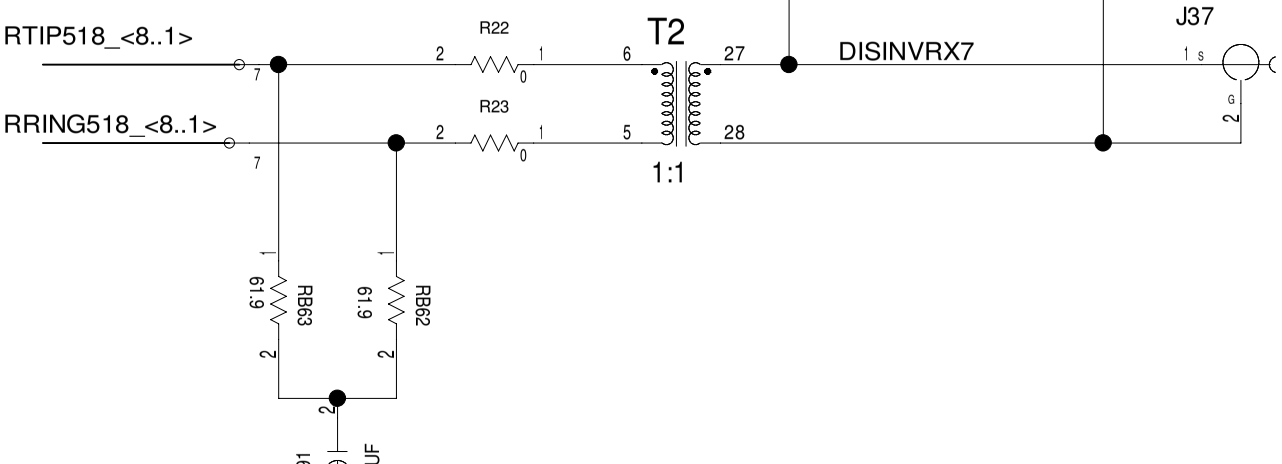


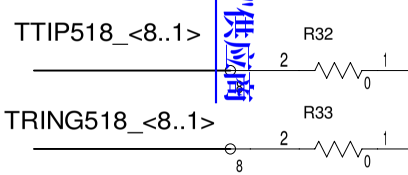


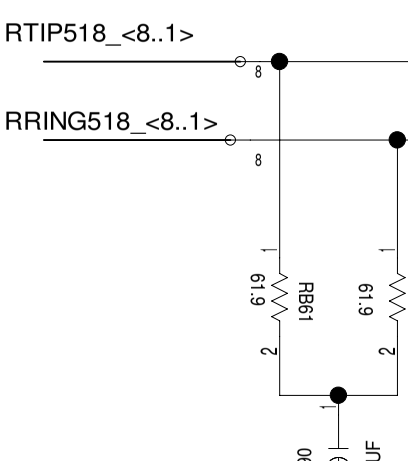


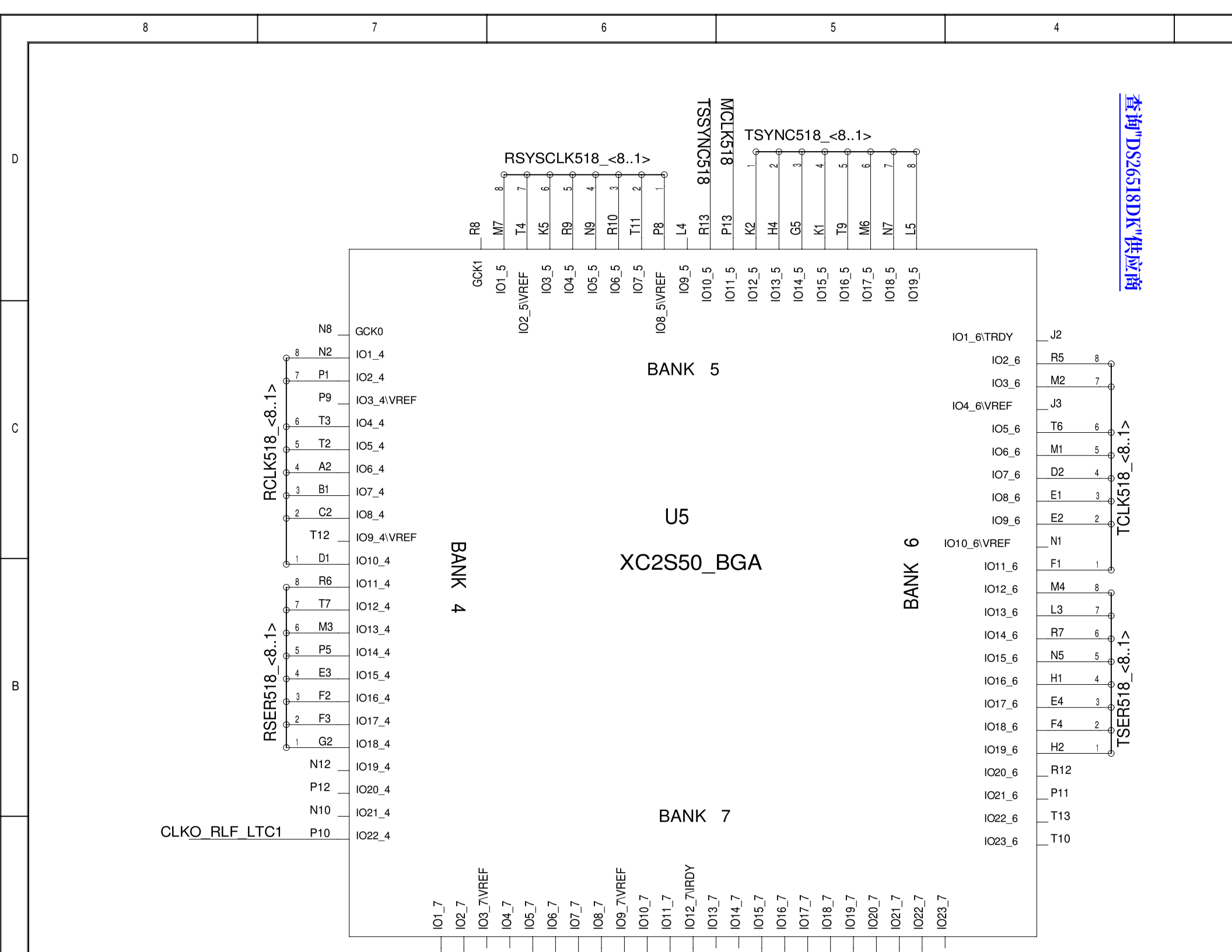


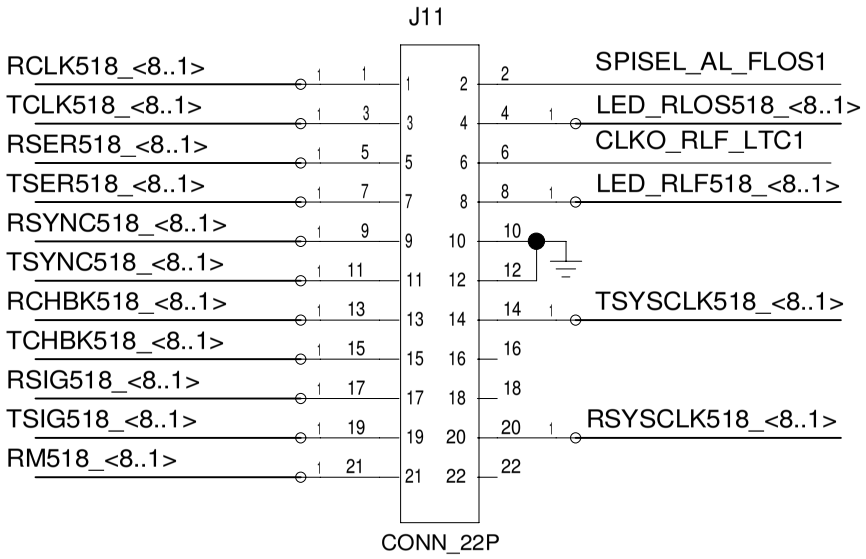


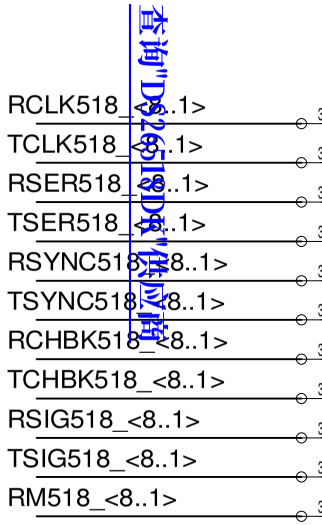


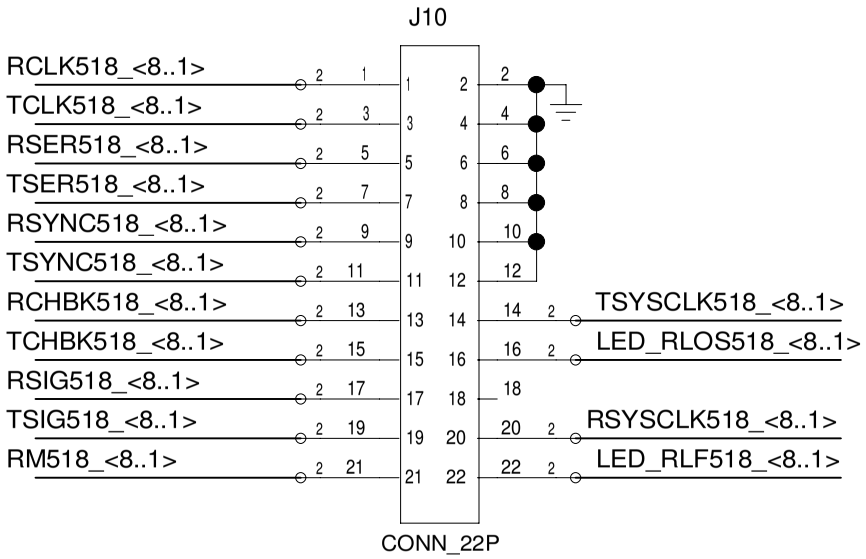


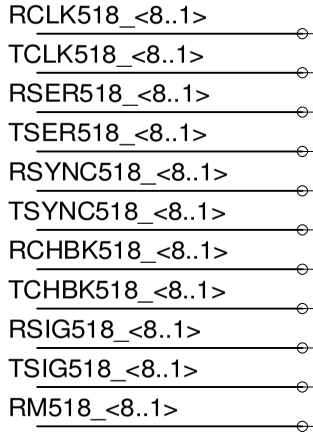


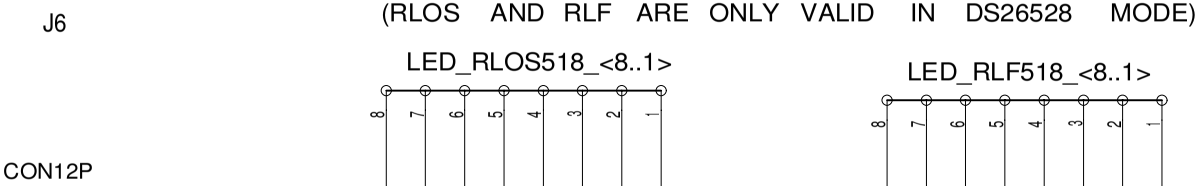


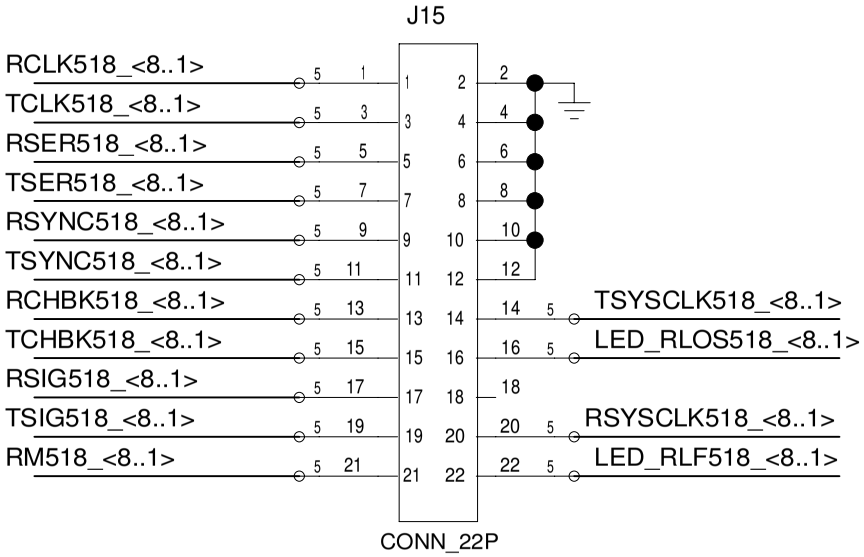

J11
RCLK518_<8..1>
TCLK518_<8..1>
RSER518_<8..1>
TSER518_<8..1>
RSYNC518_<8..1>
TSYNC518_<8..1>
RCHBK518_<8..1>
TCHBK518_<8..1>
RSIG518_<8..1>
TSIG518_<8..1>
RM518_<8..1>
SPISEL_AL_FLOS1
LED_RLOS518_<8..1>
CLKO_RLF_LTC1
LED_RLF518_<8..1>
TSYSCLK518_<8..1>
RSYSCLK518_<8..1>
CONN_22P

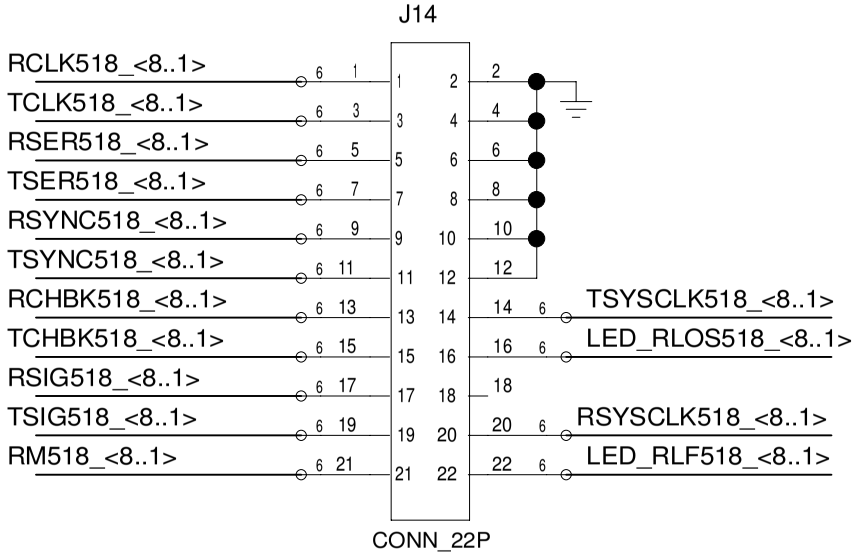

RCLK518_<8..1>
TCLK518_<8..1>
RSER518_<8..1>
TSER518_<8..1>
RSYNC518_<8..1>
TSYNC518_<8..1>
RCHBK518_<8..1>
TCHBK518_<8..1>
RSIG518_<8..1>
TSIG518_<8..1>
RM518_<8..1>

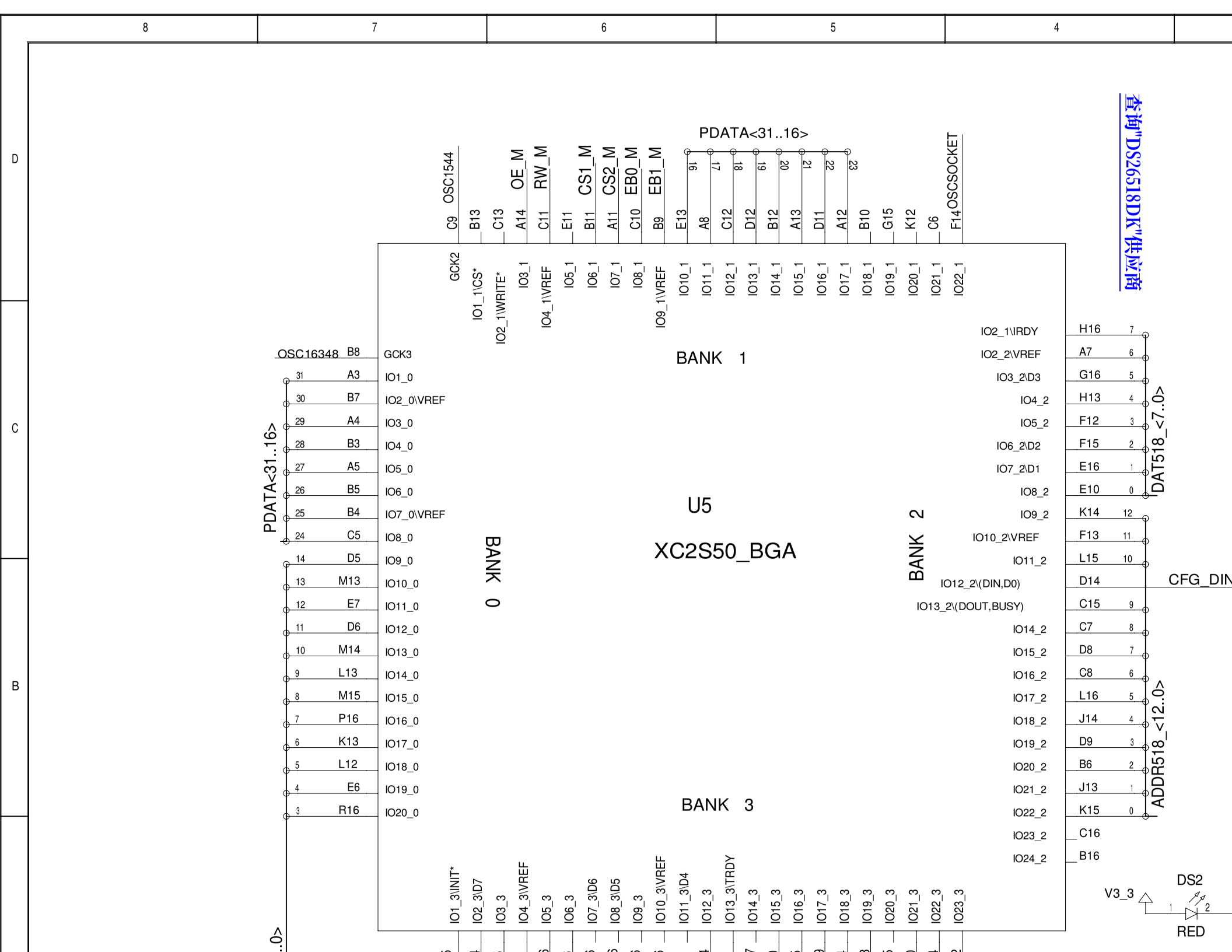

J10
RCLK518_<8..1>
TCLK518_<8..1>
RSER518_<8..1>
TSER518_<8..1>
RSYNC518_<8..1>
TSYNC518_<8..1>
RCHBK518_<8..1>
TCHBK518_<8..1>
RSIG518_<8..1>
TSIG518_<8..1>
RM518_<8..1>
TSYSCLK518_<8..1>
LED_RLOS518_<8..1>
RSYSCLK518_<8..1>
LED_RLF518_<8..1>
CONN_22P

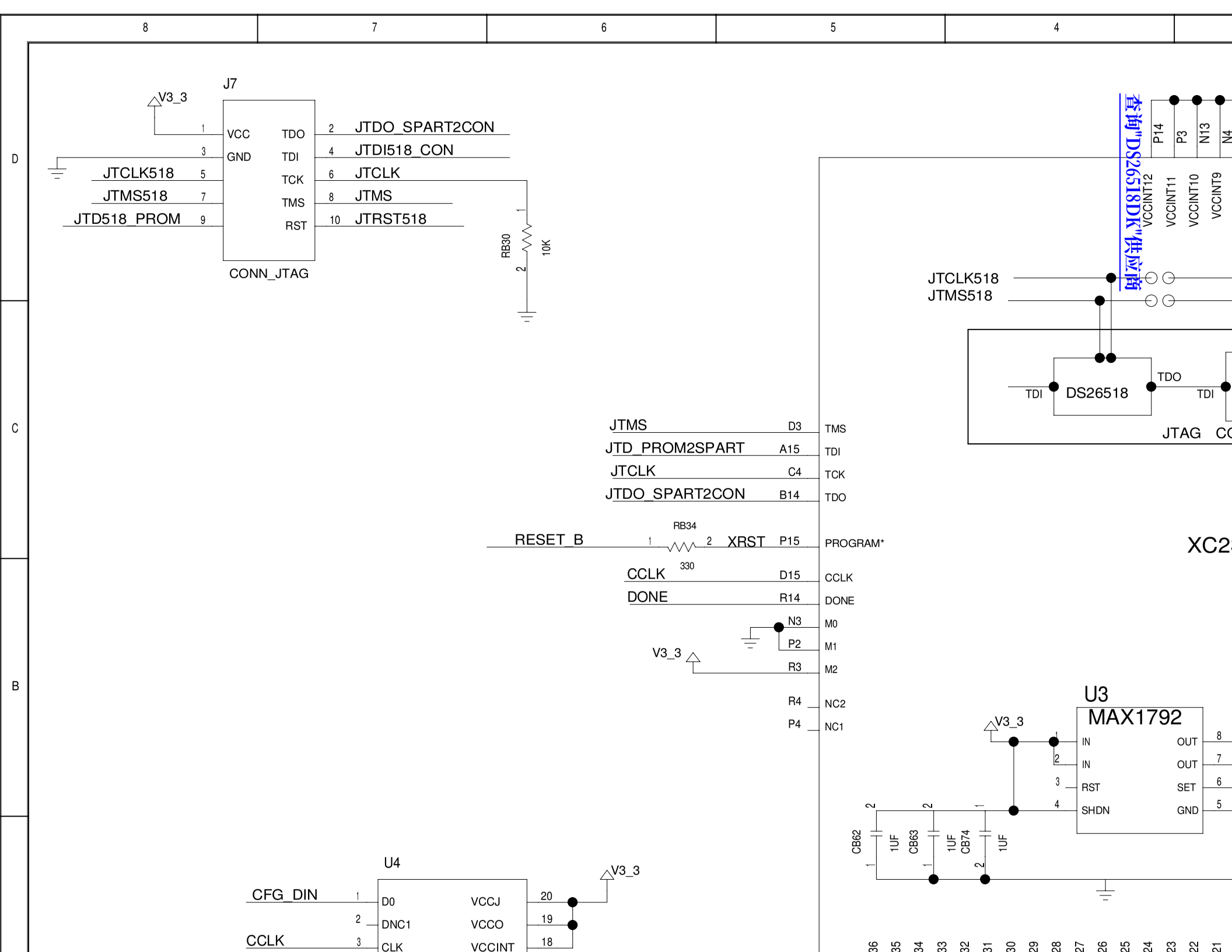

RCLK518_<8..1>
TCLK518_<8..1>
RSER518_<8..1>
TSER518_<8..1>
RSYNC518_<8..1>
TSYNC518_<8..1>
RCHBK518_<8..1>
TCHBK518_<8..1>
RSIG518_<8..1>
TSIG518_<8..1>
RM518_<8..1>

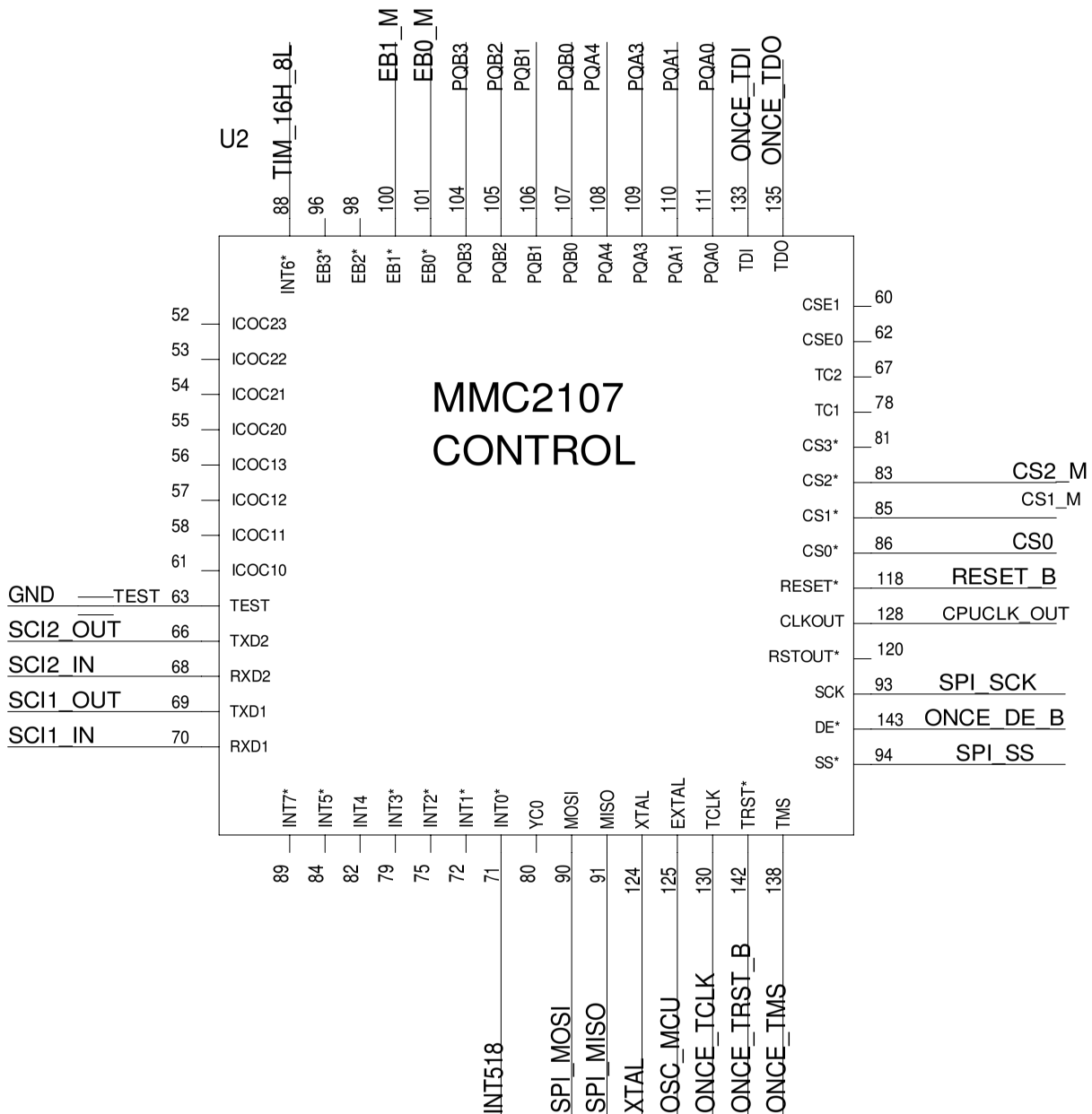

J6
(RLOS AND RLF ARE ONLY VALID IN DS26528 MODE)
LED_RLOS518_<8..1>
LED_RLF518_<8..1>
CON12P

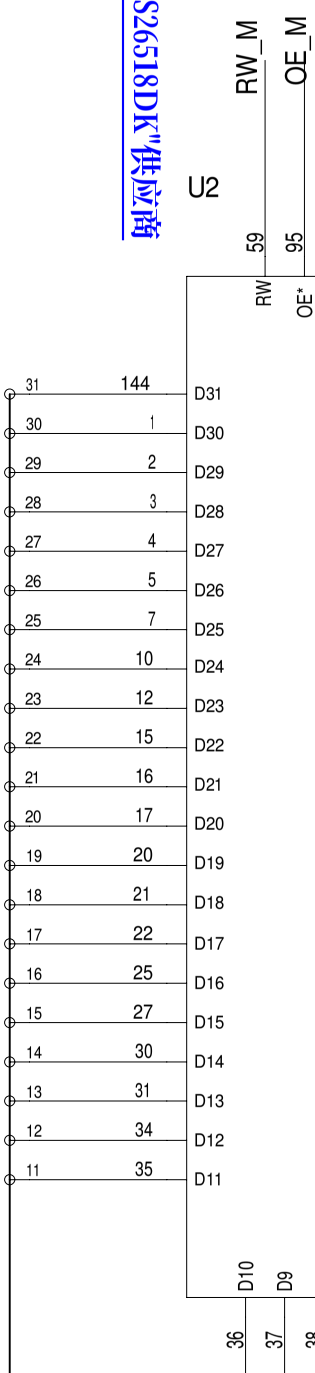




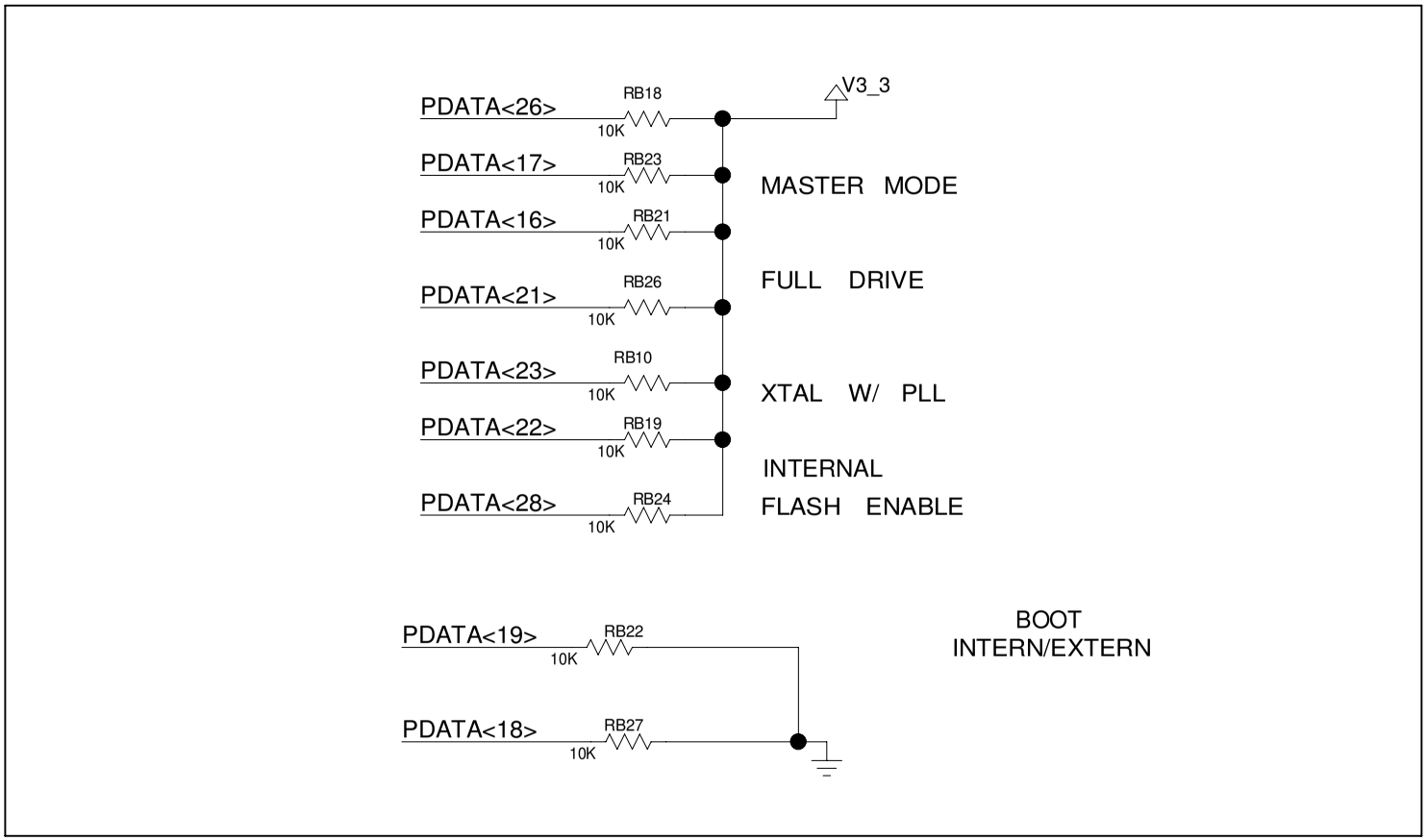


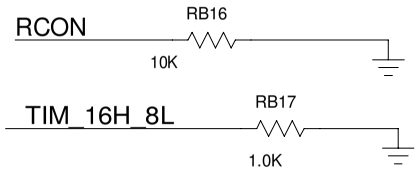

J7
V3_3
VCC
GND
TDO
TDI
TCK
TMS
RST
JTDO_SPART2CON
JTDI518_CON
JTCLK
JTMS
JTRST518
JTCLK518
JTMS518
JTD518_PROM
CONN_JTAG
RB30
10K
P14
P3
N13
N4
VCCINT12
VCCINT11
VCCINT10
VCCINT9
JTCLK518
JTMS518
TDI
DS26518
TDO
TDI
JTAG
JTMS
JTD_PROM2SPART
JTCLK
JTDO_SPART2CON
D3
A15
C4
B14
TMS
TDI
TCK
TDO
RB34
RESET_B
XRST
P15
PROGRAM*
330
CCLK
D15
CCLK
DONE
R14
DONE
N3
P2
R3
M0
M1
M2
V3_3
R4
P4
NC2
NC1
U3
MAX1792
V3_3
IN
IN
RST
SHDN
OUT
OUT
SET
GND
CB62
1UF
CB63
1UF
CB74
1UF
U4
V3_3
CFG_DIN
CCLK
D0
DNC1
CLK
VCCJ
VCCO
VCCINT

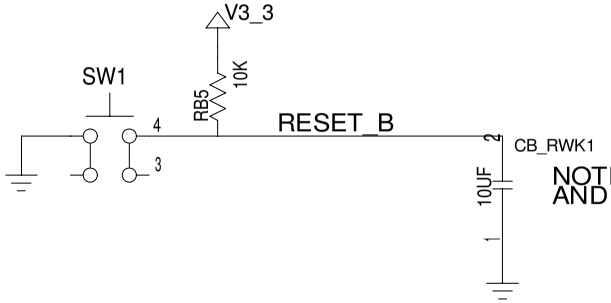




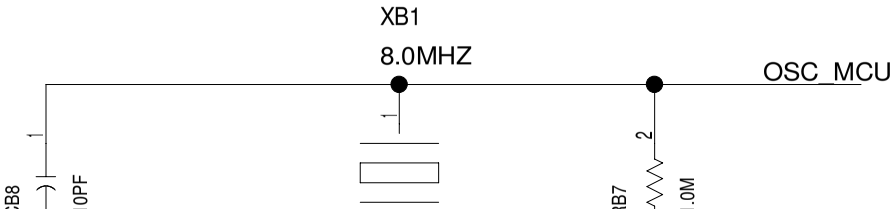
RESET CONFIGURATION

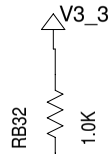


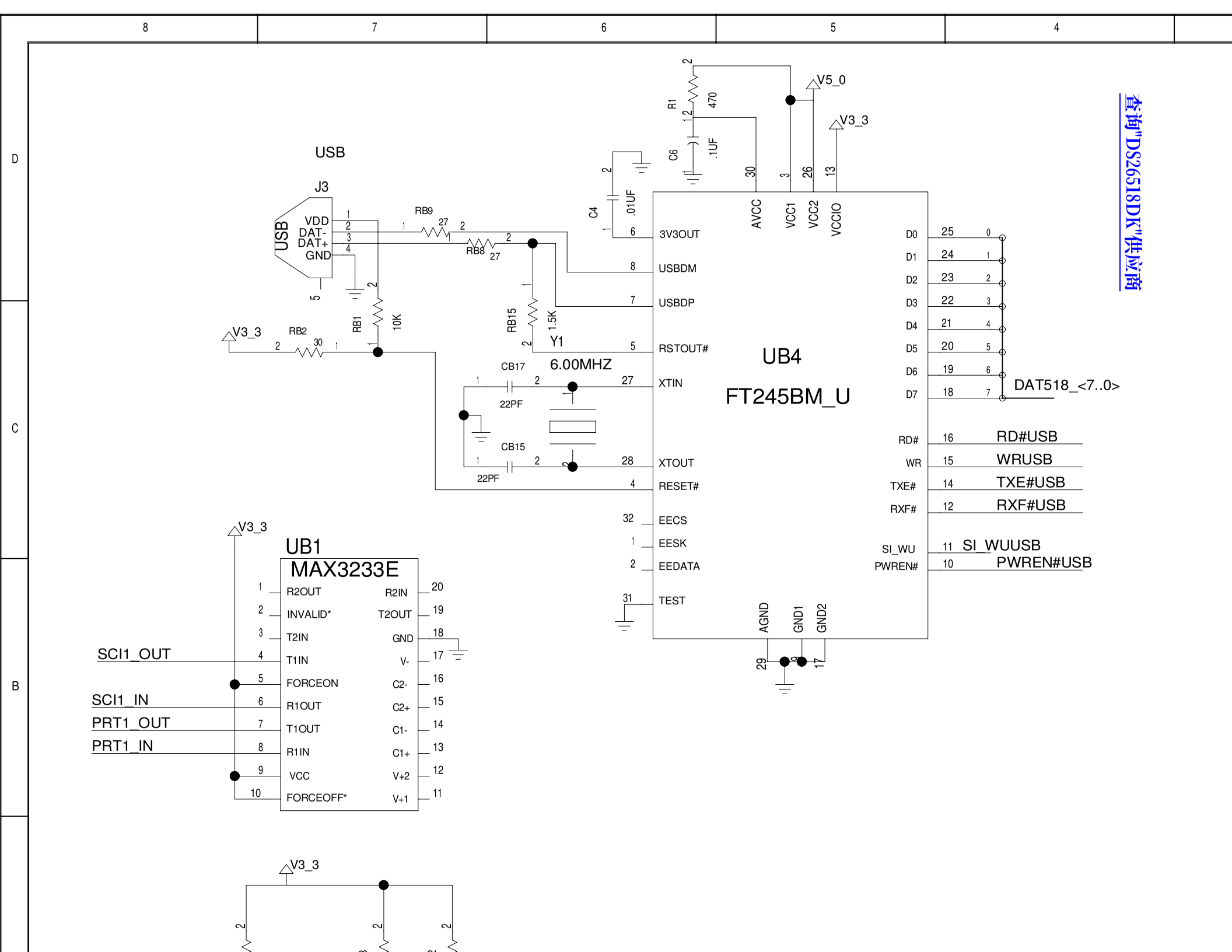




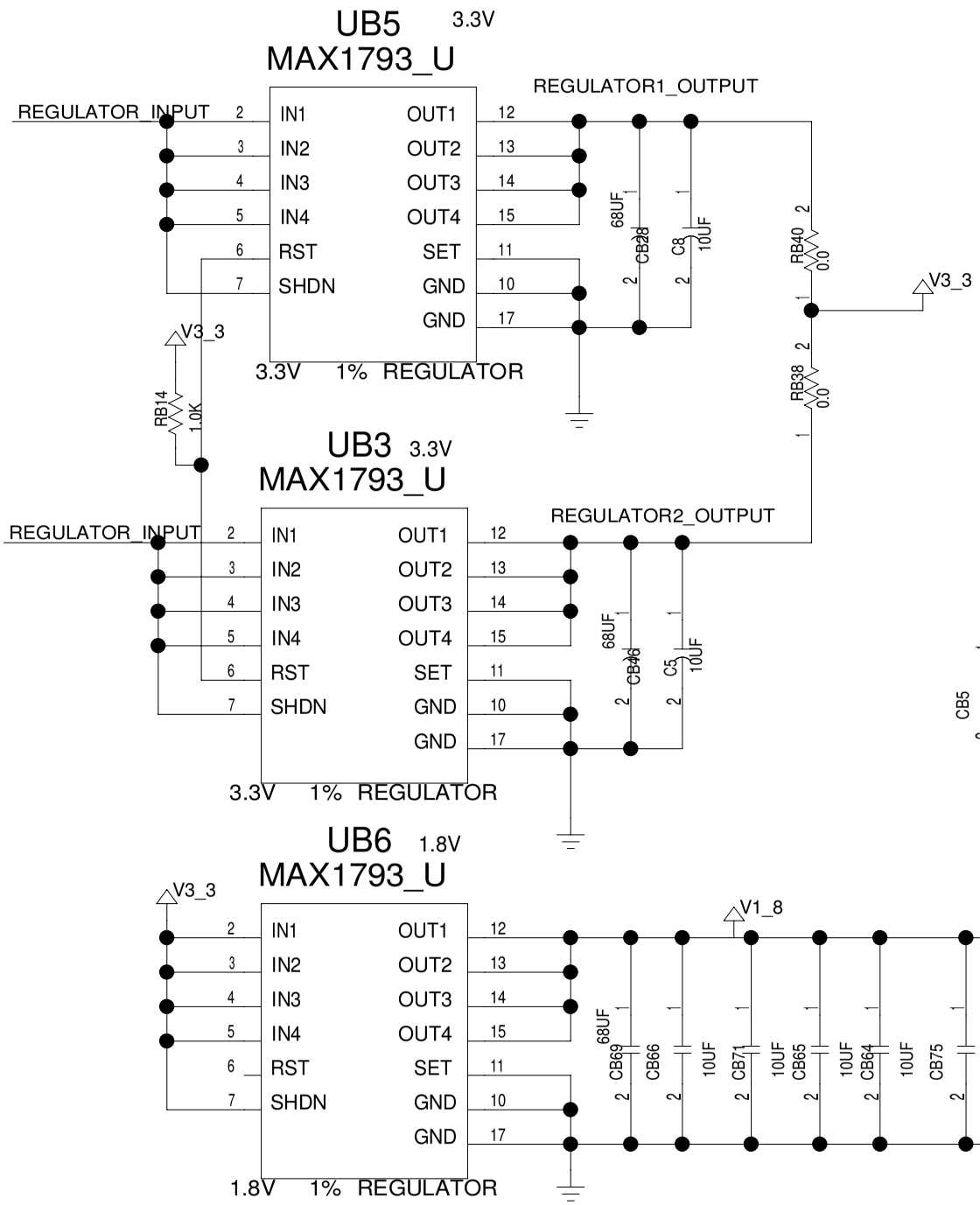
NOTE: CB_RWK1 IS A REWORK COMPONENT AND IS HAND SOLDERED TO SW1.2+SW1.3

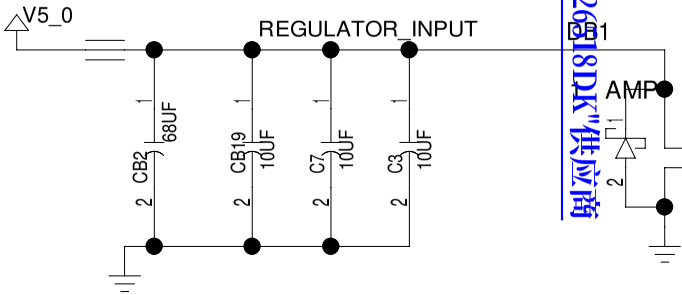


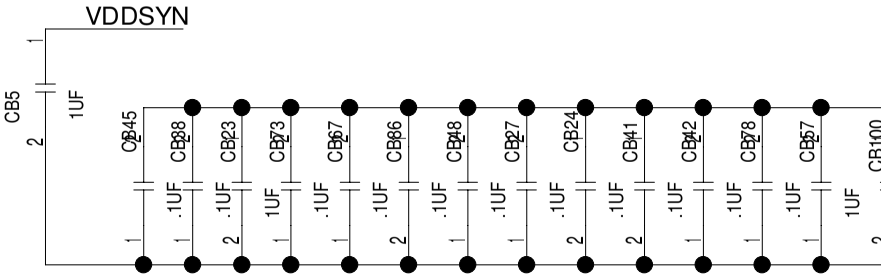




TRACES BETWEEN REGULATOR OUTPUT AND V3.3 SHOULD
BE LONG ENOUGH TO BUILD 0.06 OHM OF RESISTANCE
TO ENSURE LOAD SHARING BETWEEN THE 3.3V 1% REGULATORS
TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER







Title: Basenet Report
Design: dn_ds26528_dn
Date: Apr 17 11:00:30 2006

Base nets and synonyms for
dn_ds26528_dn_lib.DN_DS26528_DN(@dn_ds26528_dn_lib.dn_ds26528_dn(sch_1))

Base Signal	Synonyms	Location([Zone][dir])
ADDR518_<12..0>	ADDR518_<12..0> - @dn_ds26528_dn_lib.DN_DS26528_DN	12B3 2B3
BPCLK518	BPCLK518 - @dn_ds26528_dn_lib.DN_DS26528_DN	2B8 9A7 10A7
BTS518	BTS518 - @dn_ds26528_dn_lib.DN_DS26528_DN	2B8 9B3
CCLK	CCLK - @dn_ds26528_dn_lib.DN_DS26528_DN	13A8 13B6
CFG_DIN	CFG_DIN - @dn_ds26528_dn_lib.DN_DS26528_DN	12B4 13A8
CLKO_RLF_LTC1	CLKO_RLF_LTC1 - @dn_ds26528_dn_lib.DN_DS26528_DN	9A8 10D6 2B8
CPUCLK_OUT	CPUCLK_OUT - @dn_ds26528_dn_lib.DN_DS26528_DN	12A6 14B5
CS0	CS0 - @dn_ds26528_dn_lib.DN_DS26528_DN	14B5 15B2 15D2
CS1_M	CS1_M - @dn_ds26528_dn_lib.DN_DS26528_DN	12D6 14B5
CS2_M	CS2_M - @dn_ds26528_dn_lib.DN_DS26528_DN	12D6 14C5
CS518	CS518 - @dn_ds26528_dn_lib.DN_DS26528_DN	2B2 2B8
CS_X1	CS_X1 - @dn_ds26528_dn_lib.DN_DS26528_DN	2C1 12A5
D0_SPI_MISO	D0_SPI_MISO - @dn_ds26528_dn_lib.DN_DS26528_DN	2B2 2B3
D1_SPI_MOSI	D1_SPI_MOSI - @dn_ds26528_dn_lib.DN_DS26528_DN	2B2 2B3
D2_SPI_CLK	D2_SPI_CLK - @dn_ds26528_dn_lib.DN_DS26528_DN	2A2 2B3
D5_SPI_SWAP	D5_SPI_SWAP - @dn_ds26528_dn_lib.DN_DS26528_DN	2B3 9D2
	DAT518_<7..0> - @dn_ds26528_dn_lib.DN_DS26528_DN	16C4 2A1 12C3
D6_SPI_CPHA	D6_SPI_CPHA - @dn_ds26528_dn_lib.DN_DS26528_DN	2B3 9C2
	DAT518_<7..0> - @dn_ds26528_dn_lib.DN_DS26528_DN	16C4 2A1 12C3
D7_SPI_CPOL	D7_SPI_CPOL -	2A3 9C2

	@dn_ds26528_dn_lib.
DISINVRX2	DISINVRX2 -
	@dn_ds26528_dn_lib.
DISINVRX3	DISINVRX3 -
	@dn_ds26528_dn_lib.
DISINVRX4	DISINVRX4 -
	@dn_ds26528_dn_lib.
DISINVRX5	DISINVRX5 -
	@dn_ds26528_dn_lib.
DISINVRX6	DISINVRX6 -
	@dn_ds26528_dn_lib.
DISINVRX7	DISINVRX7 -
	@dn_ds26528_dn_lib.
DISINVRX8	DISINVRX8 -
	@dn_ds26528_dn_lib.
DISINVTX1	DISINVTX1 -
	@dn_ds26528_dn_lib.
DISINVTX2	DISINVTX2 -
	@dn_ds26528_dn_lib.
DISINVTX3	DISINVTX3 -
	@dn_ds26528_dn_lib.
DISINVTX4	DISINVTX4 -
	@dn_ds26528_dn_lib.
DISINVTX5	DISINVTX5 -
	@dn_ds26528_dn_lib.
DISINVTX6	DISINVTX6 -
	@dn_ds26528_dn_lib.
DISINVTX7	DISINVTX7 -
	@dn_ds26528_dn_lib.
DISINVTX8	DISINVTX8 -
	@dn_ds26528_dn_lib.
DONE	DONE -
	@dn_ds26528_dn_lib.
EB0_M	EB0_M -
	@dn_ds26528_dn_lib.
EB1_M	EB1_M -
	@dn_ds26528_dn_lib.
FLASH_VPP	FLASH_VPP -
	@dn_ds26528_dn_lib.
INT518	INT518 -
	@dn_ds26528_dn_lib.
INT518_LED	INT518_LED -
	@dn_ds26528_dn_lib.
JTCLK	JTCLK -
	@dn_ds26528_dn_lib.
JTCLK518	JTCLK518 -
	@dn_ds26528_dn_lib.

	@dn_ds26528_dn_lib.DN_DS26528_DN	
JTD_PROM2SPART	JTD_PROM2SPART -	13A6 13C6
	@dn_ds26528_dn_lib.DN_DS26528_DN	
JTMS	JTMS -	13A8 13D7 13C6
	@dn_ds26528_dn_lib.DN_DS26528_DN	
JTMS518	JTMS518 -	13D8 2C8
	@dn_ds26528_dn_lib.DN_DS26528_DN	
JTRST518	JTRST518 -	13D7 2C8
	@dn_ds26528_dn_lib.DN_DS26528_DN	
LED_RLF518_<8..1>	LED_RLF518_<8..1> -	10B2 10B6 10C2 10D6 11A1
	@dn_ds26528_dn_lib.DN_DS26528_DN	11A5 11C1 11C5 10A4
LED_RLOS518_<8..1>	LED_RLOS518_<8..1> -	10B2 10B6 10C2 10D6 11B1
	@dn_ds26528_dn_lib.DN_DS26528_DN	11B5 11C1 11C5 10A6
MCLK518	MCLK518 -	9D5 10A7 2B8
	@dn_ds26528_dn_lib.DN_DS26528_DN	
OE_M	OE_M -	12D6 14D3 15B2 15D2
	@dn_ds26528_dn_lib.DN_DS26528_DN	
ONCE_DE_B	ONCE_DE_B -	14B5 16B1
	@dn_ds26528_dn_lib.DN_DS26528_DN	
ONCE_TCLK	ONCE_TCLK -	14A6 16C3
	@dn_ds26528_dn_lib.DN_DS26528_DN	
ONCE_TDI	ONCE_TDI -	14D6 16C3
	@dn_ds26528_dn_lib.DN_DS26528_DN	
ONCE_TDO	ONCE_TDO -	14D6 16C3
	@dn_ds26528_dn_lib.DN_DS26528_DN	
ONCE_TMS	ONCE_TMS -	14A6 16C1
	@dn_ds26528_dn_lib.DN_DS26528_DN	
ONCE_TRST_B	ONCE_TRST_B -	14A6 16B2
	@dn_ds26528_dn_lib.DN_DS26528_DN	
OSC1544	OSC1544 -	12D1 12D7
	@dn_ds26528_dn_lib.DN_DS26528_DN	
OSC16348	OSC16348 -	12C1 12C7
	@dn_ds26528_dn_lib.DN_DS26528_DN	
OSCSOCKET	OSCSOCKET -	12C1 12D4
	@dn_ds26528_dn_lib.DN_DS26528_DN	
OSC_MCU	OSC_MCU -	14A6 15A6
	@dn_ds26528_dn_lib.DN_DS26528_DN	
PADDR<15..0>	PADDR<15..0> -	12A7
	@dn_ds26528_dn_lib.DN_DS26528_DN	
	PADDR<22..0> -	14A1
	@dn_ds26528_dn_lib.DN_DS26528_DN	
	PADDR<17..1> -	15A3 15C3
	@dn_ds26528_dn_lib.DN_DS26528_DN	
PADDR<22..0>	PADDR<22..0> -	14A1
	@dn_ds26528_dn_lib.DN_DS26528_DN	
PADDR<17..1>	PADDR<22..0> -	14A1
	@dn_ds26528_dn_lib.DN_DS26528_DN	

PDATA<16>	PDATA<16> -
	@dn_ds26528_dn_lib.
PDATA<23..16>	PDATA<31..0> -
	@dn_ds26528_dn_lib.
	PDATA<23..16> -
	@dn_ds26528_dn_lib.
	PDATA<31..16> -
	@dn_ds26528_dn_lib.
PDATA<31..16>	PDATA<31..0> -
	@dn_ds26528_dn_lib.
	PDATA<31..16> -
	@dn_ds26528_dn_lib.
	PDATA<31..24> -
	@dn_ds26528_dn_lib.
PDATA<17>	PDATA<17> -
	@dn_ds26528_dn_lib.
PDATA<18>	PDATA<18> -
	@dn_ds26528_dn_lib.
PDATA<19>	PDATA<19> -
	@dn_ds26528_dn_lib.
PDATA<21>	PDATA<21> -
	@dn_ds26528_dn_lib.
PDATA<22>	PDATA<22> -
	@dn_ds26528_dn_lib.
PDATA<23>	PDATA<23> -
	@dn_ds26528_dn_lib.
PDATA<31..24>	PDATA<31..0> -
	@dn_ds26528_dn_lib.
	PDATA<31..16> -
	@dn_ds26528_dn_lib.
	PDATA<31..24> -
	@dn_ds26528_dn_lib.
PDATA<26>	PDATA<26> -
	@dn_ds26528_dn_lib.
PDATA<28>	PDATA<28> -
	@dn_ds26528_dn_lib.
PQA0	PQA0 -
	@dn_ds26528_dn_lib.
PQA1	PQA1 -
	@dn_ds26528_dn_lib.
PQA3	PQA3 -
	@dn_ds26528_dn_lib.
PQA4	PQA4 -
	@dn_ds26528_dn_lib.
PQB0	PQB0 -
	@dn_ds26528_dn_lib.
PQB1	PQB1 -

PRT1_IN	PRT1_IN - @dn_ds26528_dn_lib.DN_DS26528_DN	16A8 16B8
PRT1_OUT	PRT1_OUT - @dn_ds26528_dn_lib.DN_DS26528_DN	16A8 16B8
PWREN#USB	PWREN#USB - @dn_ds26528_dn_lib.DN_DS26528_DN	12A5 16B4
RCHBK518_<8..1>	RCHBK518_<8..1> - @dn_ds26528_dn_lib.DN_DS26528_DN	3A4 3A8 3C4 3C8 4A4 4A8 4C4 4C8 10B4 10B8 10C4 10C8 11B4 11B8 11C4 11C8
RCLK518_<8..1>	RCLK518_<8..1> - @dn_ds26528_dn_lib.DN_DS26528_DN	3A4 3A8 3C4 3C8 4A4 4A8 4C4 4C8 9C7 10C4 10C8 10D4 10D8 11B4 11B8 11D4 11D8
RCON	RCON - @dn_ds26528_dn_lib.DN_DS26528_DN	14D3 15B8
RD#USB	RD#USB - @dn_ds26528_dn_lib.DN_DS26528_DN	12A5 16C4
RD_DS518	RD_DS518 - @dn_ds26528_dn_lib.DN_DS26528_DN	12A4 2B8
REFCLK518	REFCLK518 - @dn_ds26528_dn_lib.DN_DS26528_DN	2B8 9A7 10A7
REGULATOR1_OUTPUT	REGULATOR1_OUTPUT - @dn_ds26528_dn_lib.DN_DS26528_DN	17D7
REGULATOR2_OUTPUT	REGULATOR2_OUTPUT - @dn_ds26528_dn_lib.DN_DS26528_DN	17C7
RESET_B	RESET_B - @dn_ds26528_dn_lib.DN_DS26528_DN	14B5 15B5 16C3 2B8 13C7
RM518_<8..1>	RM518_<8..1> - @dn_ds26528_dn_lib.DN_DS26528_DN	3A4 3A8 3C4 3C8 4A4 4A8 4C4 4C8 10B4 10B8 10C4 10C8 11A4 11A8 11C4 11C8
RRING518_<8..1>	RRING518_<8..1> - @dn_ds26528_dn_lib.DN_DS26528_DN	3B4 3B8 3D4 3D8 4B4 4B8 4D4 4D8 5B4 5B8 6B4 6B8 7B4 7B8 8B4 8B8
RSER518_<8..1>	RSER518_<8..1> - @dn_ds26528_dn_lib.DN_DS26528_DN	3A4 3A8 3C4 3C8 4A4 4A8 4C4 4C8 9B7 10B8 10C4 10D4 10D8 11B4 11B8 11D4 11D8
RSIG518_<8..1>	RSIG518_<8..1> - @dn_ds26528_dn_lib.DN_DS26528_DN	3A4 3A8 3C4 3C8 4A4 4A8 4C4 4C8 10B4 10B8 10C4 10C8 11B4 11B8 11C4 11C8
RSYNC518_<8..1>	RSYNC518_<8..1> - @dn_ds26528_dn_lib.DN_DS26528_DN	3A4 3A8 3C4 3C8 4A4 4A8 4C4 4C8 9A5 10B4 10B8 10D4 10D8 11B4 11B8 11C4 11C8
RSYSCLK518_<8..1>	RSYSCLK518_<8..1> - @dn_ds26528_dn_lib.DN_DS26528_DN	10B2 10B6 10C2 10C6 11B1 11B5 11C1 11C5 3A4 3A8

SCANEN518	SCANEN518 - @dn_ds26528_dn_lib.
SCANMO518	SCANMO518 - @dn_ds26528_dn_lib.
SCI1_IN	SCI1_IN - @dn_ds26528_dn_lib.
SCI1_OUT	SCI1_OUT - @dn_ds26528_dn_lib.
SCI2_IN	SCI2_IN - @dn_ds26528_dn_lib.
SCI2_OUT	SCI2_OUT - @dn_ds26528_dn_lib.
SI_WUUSB	SI_WUUSB - @dn_ds26528_dn_lib.
SPISEL_AL_FLOS1	SPISEL_AL_FLOS1 @dn_ds26528_dn_lib.
SPI_MISO	SPI_MISO - @dn_ds26528_dn_lib.
SPI_MOSI	SPI_MOSI - @dn_ds26528_dn_lib.
SPI_SCK	SPI_SCK - @dn_ds26528_dn_lib.
SPI_SS	SPI_SS - @dn_ds26528_dn_lib.
TCHBK518_<8..1>	TCHBK518_<8..1> @dn_ds26528_dn_lib
TCLK518_<8..1>	TCLK518_<8..1> @dn_ds26528_dn_lib
TIM_16H_8L	TIM_16H_8L - @dn_ds26528_dn_lib.
TRING518_<8..1>	TRING518_<8..1> @dn_ds26528_dn_lib
TSER518_<8..1>	TSER518_<8..1> @dn_ds26528_dn_lib
TSIG518_<8..1>	TSIG518_<8..1> @dn_ds26528_dn_lib
TSSYNC518	TSSYNC518 - @dn_ds26528_dn_lib.
TSYNC518_<8..1>	TSYNC518_<8..1>

		9A6
TTIP518_<8..1>	TTIP518_<8..1> - @dn_ds26528_dn_lib.DN_DS26528_DN	3A5 3B1 3C1 3C5 4B1 4B5 4C1 4C5 5D4 5D8 6D4 6D8 7D4 7D8 8D4 8D8
TXE#USB	TXE#USB - @dn_ds26528_dn_lib.DN_DS26528_DN	12A5 16C4
TXENA518	TXENA518 - @dn_ds26528_dn_lib.DN_DS26528_DN	2A8 9A2
VDDSYN	VDDSYN - @dn_ds26528_dn_lib.DN_DS26528_DN	14D2 17C5
WRUSB	WRUSB - @dn_ds26528_dn_lib.DN_DS26528_DN	12A5 16C4
WR_RW518	WR_RW518 - @dn_ds26528_dn_lib.DN_DS26528_DN	12A5 2B8
XRST	XRST - @dn_ds26528_dn_lib.DN_DS26528_DN	13A8 13C5
XTAL	XTAL - @dn_ds26528_dn_lib.DN_DS26528_DN	14A6 15A6
X_INIT	X_INIT - @dn_ds26528_dn_lib.DN_DS26528_DN	12A7 13A8