ZARLINK SEMICONDUCTOR

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MGCM01

TDMA/AMPS Baseband Interface

DS2497 ISSUE 3.3 December 2002

Features

- IS136 TDMA/AMPS Compatible
- Channel Filtering (30kHz)
- FM Demodulator
- RSSI Output
- Dual IF Synthesisers
- Flexible Power Control
- Fully Programmable via Serial Bus
- 3 Volt operation
- 48-pin TQFP package

Applications

- Dual Mode TDMA/AMPS Mobile Telephones
- Dual Band (PCS1900/900) TDMA/AMPS Mobile Telephones
- PCS 1900 TDMA Mobile Telephones

Description

The MGCM01 provides channel filtering for IS136 TDMA/AMPS mobile telephones.

Ordering Information

MGCM01/KG/TP1N

The inputs for the receive path are I and Q signals at an IF of 60kHz. The I and Q signals are filtered by a 60kHz switched capacitor bandpass filter and are then demodulated to give baseband I and Q signals. The MGCM01 also provides voltage gain so that the baseband outputs can be input directly to an A to D converter.

The internal FM discriminator can be used for demodulating AMPS signals; the receive path also provides RSSI.

Transmit I and Q baseband signals from D to A converters can be input directly to the MGCM01, which provides reconstruction filters and a variable gain buffer.

The two PLL synthesisers are used for generation of the receive and transmit IF LO signals.

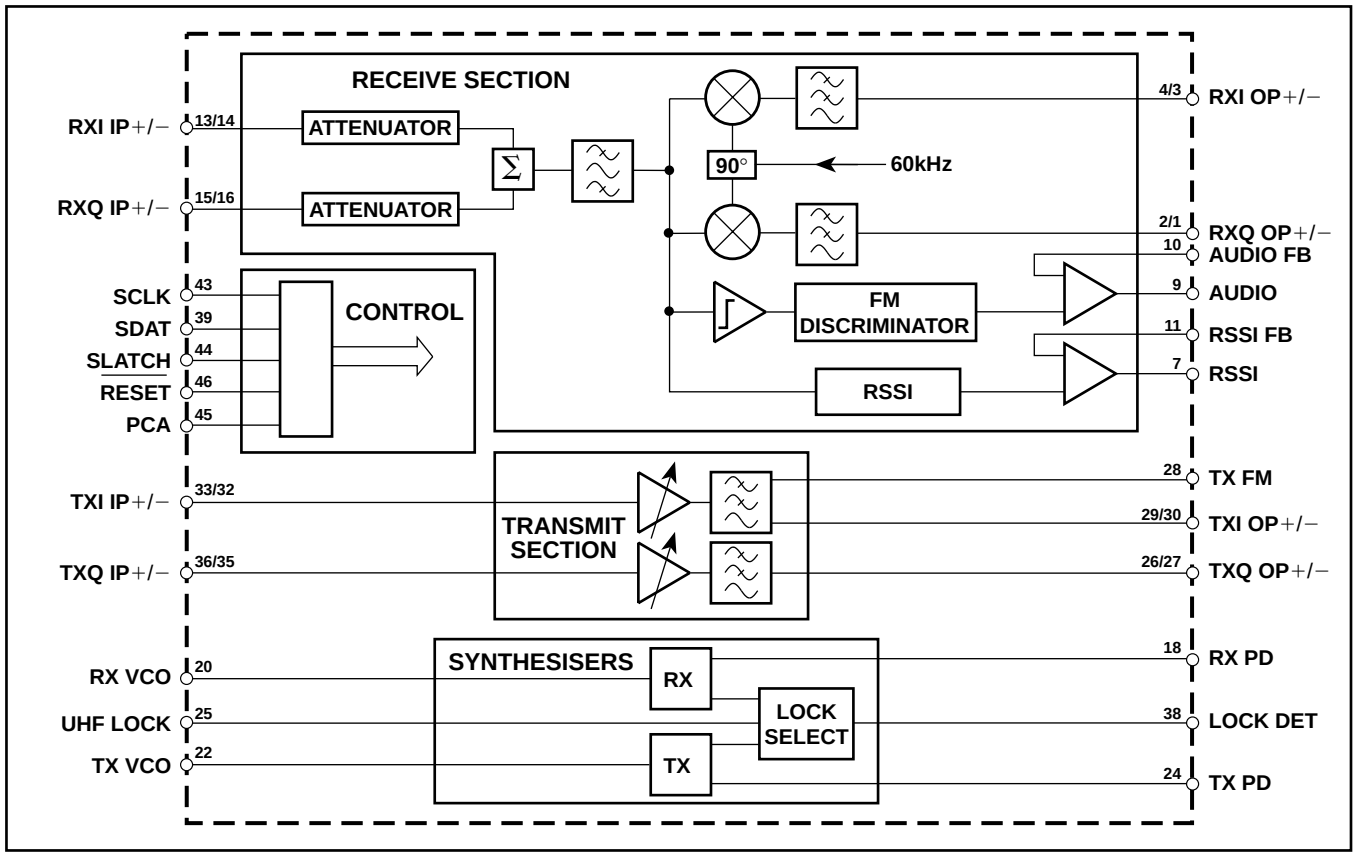

Figure 1 - MGCM01 block diagram

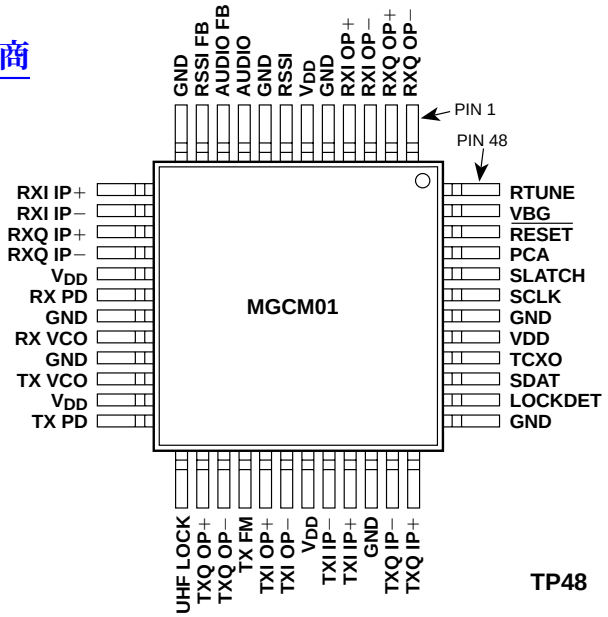

Figure 2 - Pin connections - top view

Pin	Name	Type	Description	Pin	Name	Type	Description
1	RXQ OP-	O	Baseband receive Q output-	25	UHF LOCK	I	UHF synthesiser lock input
2	RXQ OP+	O	Baseband receive Q output+	26	TXQ OP+	O	Transmit Q output+
3	RXI OP-	O	Baseband receive I output-	27	TXQ OP-	O	Transmit Q output-
4	RXI OP+	O	Baseband receive I output+	28	TX FM	O	Transmit FM output
5	GND	GND	Ground (substrate connection)	29	TXI OP+	O	Transmit I output+
6	V_{DD}	PWR	Power - RSSI/demodulator	30	TXI OP-	O	Transmit I output-
7	RSSI	O	RSSI output	31	V_{DD}	PWR	Power - transmit section
8	GND	GND	Ground - RSSI/demodulator	32	TXI IP-	I	Transmit I input-
9	AUDIO	O	Demodulator audio/data output	33	TXI IP+	I	Transmit I input+
10	AUDIO FB	I	Demodulator feedback	34	GND	GND	Ground TX channel
11	RSSI FB	I	RSSI feedback	35	TXQ IP-	I	Transmit Q input-
12	GND	GND	Ground - receive section	36	TXQ IP+	I	Transmit Q input+
13	RXI IP+	I	Receive I Input+	37	GND	GND	Ground (substrate connection)
14	RXI IP-	I	Receive I Input-	38	LOCK DET	O	Synthesiser lock detect output
15	RXQ IP+	I	Receive Q Input+	39	SDAT	I	Serial interface, serial data in
16	RXQ IP-	I	Receive Q Input-	40	TCXO	I	19·44MHz reference from TCXO
17	V_{DD}	PWR	Power - receive section	41	V_{DD}	PWR	Power supply - digital
18	RX PD	O	Rx PLL charge pump output	42	GND	GND	Ground - digital
19	GND	GND	Ground (substrate connection)	43	SCLK	I	Serial interface clock
20	RX VCO	I	Receive IF PLL input	44	SLATCH	I	Serial interface latch
21	GND	GND	Ground - synthesiser	45	$\overline{PCA}$	I	Power control assert
22	TX VCO	I	Transmit IF PLL input	46	$\overline{RESET}$	I	Chip master reset (active low)
23	V_{DD}	PWR	Power - synthesiser	47	V_{BG}	O	Bandgap reference decoupling
24	TX PD	O	Tx PLL charge pump output	48	RTUNE	I	Bias Ref. - connect 100kΩ to GND

Table 1 Pin descriptions

Absolute Maximum Ratings

Supply voltage (V_{DD})	-0·3V to +3·9V	Storage temperature	-55°C to +150°C
Voltage applied to any pin	-0·3V to V_{DD} +0·3V	Max. junction temperature	+150°C
Operating temperature	-30°C to +100°C	ESD (Human Body Model)	2kV

Electrical Characteristics

T_{AMB} = -30°C to +85°C, V_{DD} = 3V ±10%, V_{EE} = 0V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply Current					
Sleep		20	100	µA	
Power down		550		µA	Reference circuits active
Receive section (I/Q)		10	12·5	mA	At 25°C and V_{DD} = 3·0V
Receive section (FM)		9	12	mA	At 25°C and V_{DD} = 3·0V
Receive section (I/Q)			14	mA	
Receive section (FM)			14	mA	
Transmit section (I/Q)		5·2	8	mA	
Transmit section (FM)		2·8	5·5	mA	
Logic Inputs					
Input voltage high, V_{IH}	0·8V_{DD}			V	
Input voltage low, V_{IL}			0·2V_{DD}	V	
Input current			10	nA	V_{IN} = 0V to V_{DD}
Input capacitance			10	pF	
Logic Outputs					
Output voltage low, V_{OL}			0·4	V	
Output voltage high, V_{OH}	0·6V_{DD}			V	
Output current			± 1	mA	
Serial Control Timing					See Figure 3
SDATA set up time, t_1	20			ns	
SDATA hold time, t_2	20			ns	
SCLK pulse width t_3	50			ns	
SLATCH set up time, t_4	20			ns	
SLATCH pulse width, t_5	50			ns	
SCLK period, t_6	100			ns	
Switch on/off times					
TX turn on/turn off time			0·5	ms	
RX turn on/turn off time			1·0	ms	
TCXO Input					
Input resistance	10			kΩ	
Input capacitance	10			pF	
Input sensitivity	0·5		2	Vp-p	AC coupled
Frequency		19·44		MHz	

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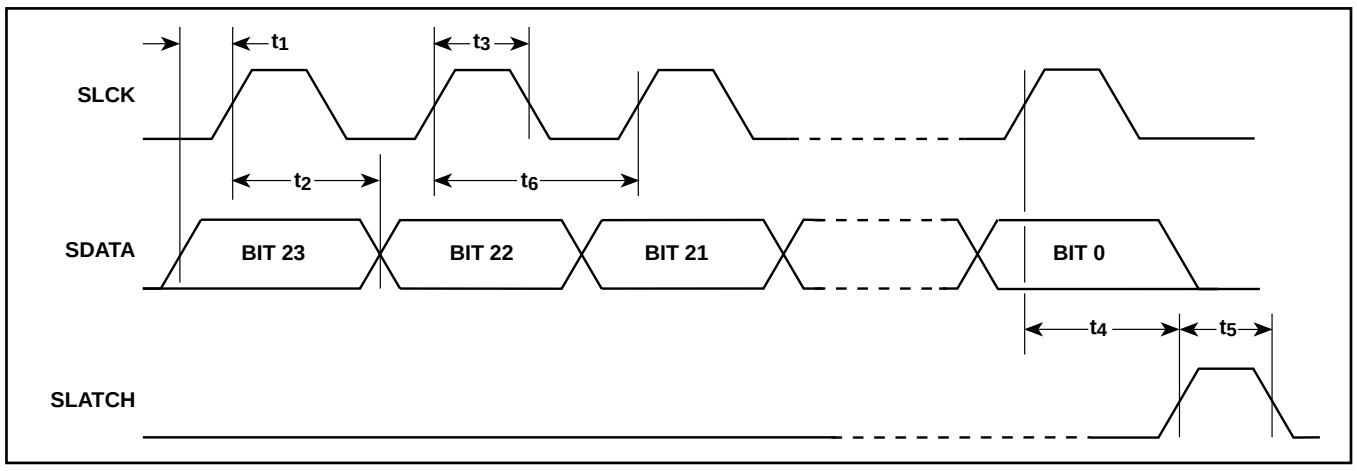


Figure 3 - Serial bus timing diagram

Electrical Characteristics (continued)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Receive - General					
Input impedance		10		kΩ	Differential
Output impedance		2		kΩ	Differential
Input voltage RXI, RXQ		$V_{DD}/2$		V	Input normally AC coupled
Output voltage RXI, RXQ	V_{DD}-1·6	V_{DD}-1·4	V_{DD}-1·2	V	
Out of band 60kHz 1dB compression	125			mV	Note 2
Out of Band 120 kHz 1dB compression	13			mV	Note 2
Input IP3	0·65	1·0		V	Note 3
Receive (I/Q Mode)					
Input signal		0·53		mV	Differential (gain = 56dB)
Gain	54	56	58·5	dB	See Table 6
I/Q gain matching	-0·5		0·5	dB	
I/Q quadrature accuracy		TBD	TBD	deg	
I/Q bandwidth Matching		0·5	2	%	
Group delay ripple		14	16	µs p-p	0 to 12·5kHz
Gain ripple		1·5	2·2	dB p-p	0 to 12·5kHz
Noise			17	µV	10Hz to 100kHz referred to input
Output 1dB compression	3			V p-p	Differential
LO breakthrough		10	22	mV	60kHz
Other spurious signals			-40	dB	
Receive (FM Mode)					
Input signal	30			µV	Output SINAD = 12dB
Audio output			500	mV	Defined by external components
Receive Filter (Bandpass)					Note 4
Centre frequency		60		kHz	Figure 5
3dB bandwidth	±16		±18	kHz	
Stop band attenuation					Relative to signal at 60kHz
0 to 3kHz	67	69		dB	
3 kHz to 10kHz	61	63		dB	
10 kHz to 22kHz	48	51		dB	
38kHz	18	20		dB	Note 5
82kHz	18	20		dB	Note 5
98kHz to 110kHz	48	50		dB	
110kHz to 117kHz	61	63		dB	
117kHz to 123kHz	68	70		dB	
123kHz to 1·36MHz	71	73		dB	
1·36MHz to 1·52MHz	36	48		dB	
1·52MHz to 10MHz	71	73		dB	
Image attenuation					Figure 6
0 to -10kHz	61			dB	
-10kHz to -42kHz	40			dB	
-42kHz to -78kHz	25	28		dB	
-78kHz to -105kHz	40			dB	
-105kHz to -1·36MHz	61			dB	
-1·36MHz to -1·52MHz	36	48		dB	
-1·52M Hz to -10MHz	61			dB	
Gain Ripple		1·0	1·5	dB	

cont…

Electrical Characteristics (continued)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
RSSI					
Dynamic range	70	73		dB	
Accuracy	- 3		+ 3	dB	
RSSI slope	17	20	23	mV/dB	
Input signal	0·024		110	mV	Internal attenuator enabled
Input signal	0·024		20	mV	Internal attenuator disabled
RSSI output level	V_{DD}/2-1·2		V_{DD}/2+1·2	V	
Attenuator gain	-31·5	-32·5	-33·5	dB	
Attenuator switch-in level		4·5		mV	Input referred
Attenuator switch-out level		2·25		mV	Input referred
RSSI output impedance		1		kΩ	
Transmit (I/Q and FM)					
Gain	11	12	13	dB	See Table 9
	8·5	9	9·5	dB	See Table 9
	5·5	6	6·5	dB	See Table 9
	2·5	3	3·5	dB	See Table 9
	-0·5	0	0·5	dB	See Table 9
Input DC voltage		0·8		V	
Output DC voltage	1·0	1·2	1·4	V	
Input signal range			2	Vp-p	Note 6
Output signal range			2	Vp-p	Note 6
Output amplitude balance	-0·3		+0·3	dB	
Output phase balance			0·7	deg	
Output DC offset		20	30	mVp-p	
3dB filter bandwidth	22	25	29	kHz	
Gain ripple			1	dB	0 to 12·5kHz
Group delay variation			10	µs	0 to 12·5kHz
Stop band attenuation	30			dB	100kHz to 2 MHz
	40			dB	>2MHz
Noise, in band			-50	dBc	Note 7
Noise 20 to 45kHz			-60	dBc	BW = 300Hz
Noise 45 to 60 kHz			-75	dBc	BW = 300Hz
Noise >= 60 kHz			-85	dBc	BW = 300Hz
Synthesisers					
Input frequency	1		115	MHz	
Input sensitivity	100			mV	
Charge pump current, I_O	400	496	600	µA	Default mode, see Table 12
	140	176	210	µA	See Table 12
	75	96	115	µA	See Table 12
	13	16	19	µA	See Table 12
Charge pump output compliance	0·5		V_{DD}-0·5	V	I_O ±15%

NOTES
1. All signal voltages are RMS unless stated otherwise.
2. Level of out of band blocking signal to cause 1dB compression of in band wanted signal.
3. Measured with unmodulated blocking signals at 60 and 120kHz.
4. These filter characteristics are for the 60kHz bandpass filter. This provides all the filtering in FM mode. There is additional filtering in I/Q mode provided by the baseband low pass filters. Details are shown in Figure 4.
5. Extrapolate linearly between 22kHz-38kHz, 82kHz-98kHz.
6. The input and output signal ranges are the maximum available. For example if the input signal is 2V pk-pk then the programmed gain must only be 0dB.
7. Noise relative to full scale signal.

OPERATING DESCRIPTION

Receive

TDMA IS136 mode

The receive path filtering is shown in more detail in Figure 4. The inputs to the MGCM01 are I and Q signals at an IF of 60 kHz. These can be generated by a quadrature demodulator circuit such as the Zarlink Semiconductor MGCR01 (Saturn) AGC amplifier and demodulator. This device is normally used for mixing direct to baseband but can also mix down to low IF quadrature signals. The I and Q signals are passed through anti-alias filters to prevent spurious responses in the subsequent switched capacitor filter. The anti-alias filter is a third order Butterworth with a 230kHz cutoff. The I and Q signals are then combined and passed through a switched capacitor bandpass filter. This filter is a tenth order Chebychev. The advantage of using a switched capacitor filter is that it gives very stable performance and no calibration is required. The circuit also provides rejection of the image frequency following the down conversion to 60kHz.

Following the bandpass filter the signal is mixed down to baseband I and Q and is output from differential outputs. There is additional baseband filtering to remove spurious signals from the down converters and clock breakthrough from the switched capacitor filters. Further detail of the filtering in the the MGCM01 receive path is shown in Figure 4. The baseband outputs can be fed directly into A to D converters in a baseband circuit.

AMPS FM Mode

Demodulation can be performed using the I and Q baseband signals. However, the MGCM01 also includes a limiting amplifier and an FM discriminator. The FM discriminator consists of a shift register acting as a delay line. The output of the discriminator is a digital signal which must be filtered to recover the audio signal. The discriminator output is routed through the cascaded baseband I and Q low pass smoothing filters and finally through an output buffer stage. External components can be used to optimise the gain and frequency response of the output amplifier.

Further information on using MGCM01 in FM mode is provided in application note "MGCM01 in AMPS environment".

RSSI

The MGCM01 also contains RSSI circuitry. This would normally be used when using the FM discriminator to provide the received signal strength to the phone's microcontroller. The RSSI circuit has over 70dB dynamic range. In the presence of strong signals the RSSI circuit switches in a 32dB attenuator in the IF I and Q input stages to optimise dynamic range. The RSSI circuit will not normally be used in I/Q mode except if required to monitor base station signal strength.

A block diagram of the RSSI circuit is shown in Figure 7. The switched capacitor filter has a limited dynamic range of approximately 50dB due to aliased noise from the sampling process used. In order to enable the RSSI to operate over a larger dynamic range the RSSI output is input to a comparator. The output of the comparator then switches a 32·5dB attenuator in the 60kHz I and Q input stages and enables a larger dynamic range for the RSSI. Hysteresis is built in to prevent oscillation when close to the threshold level. Figure 8 shows the RSSI characteristic. At low signal levels the RSSI output increases with signal level; however, at high signal level when the attenuator is switched in the input path, the RSSI output is mirrored around $V_{DD}/2$ and decreases with increasing signal level. The slope is the same at high level as at low level but is, of course, negative. The actual slope (or gain) and settling time for the RSSI are set by external components as shown in Figure 7.

The RSSI output from the MGCM01 will normally be input into an A to D converter. This, together with the baseband controller can convert the RSSI signal to a monotonic digital output as required by the IS136 specifications.

Calibration will be required to determine the slope and offset at low and high signal levels, and the threshold level of the RSSI characteristic. For example if the RSSI output is less than $V_{DD}/2$ then the RSSI slope is positive; if greater than $V_{DD}/2$ then the RSSI slope is negative.

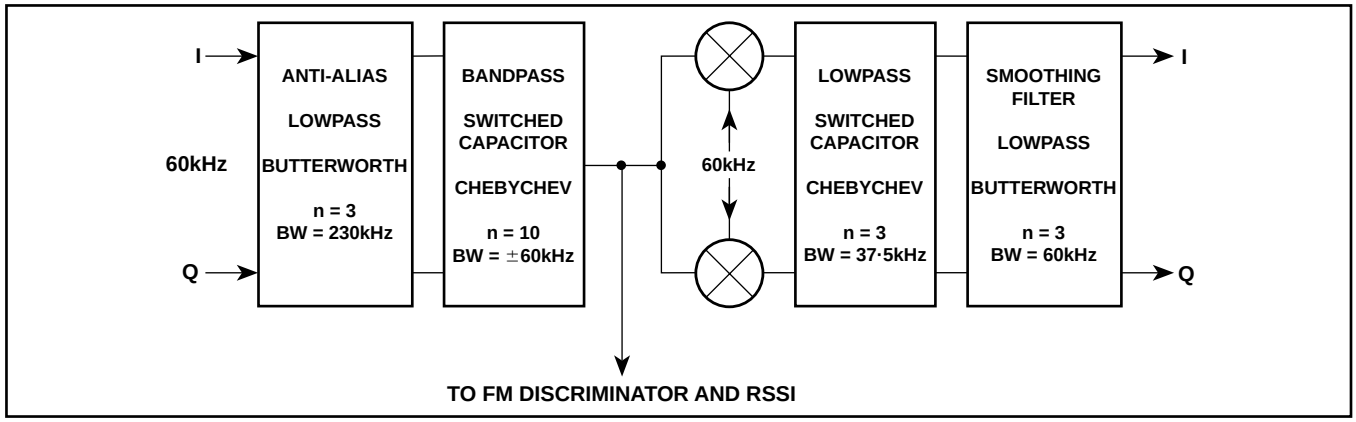


Figure 4 - Receive path filters

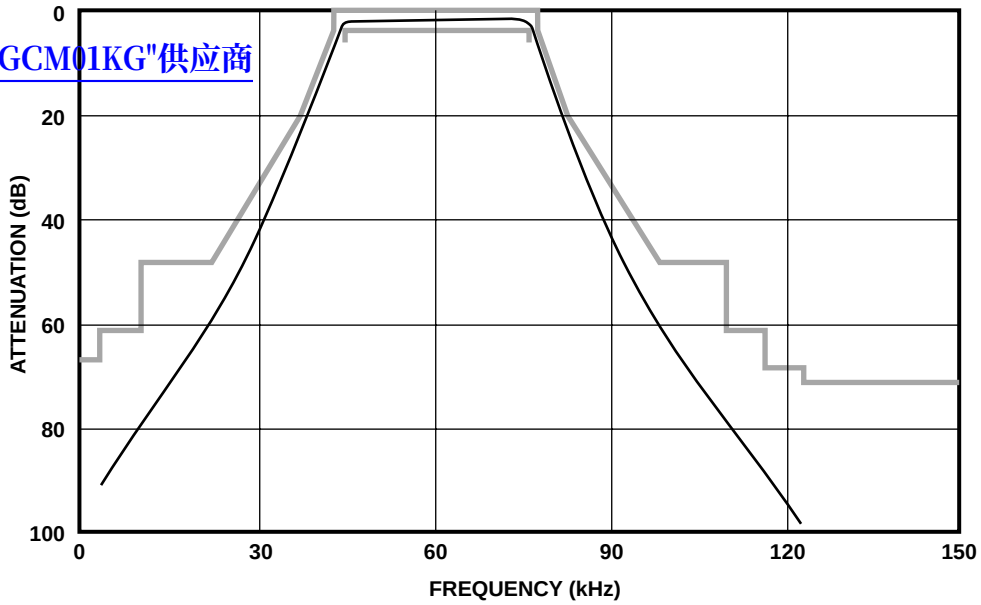


Figure 5a - Filter response

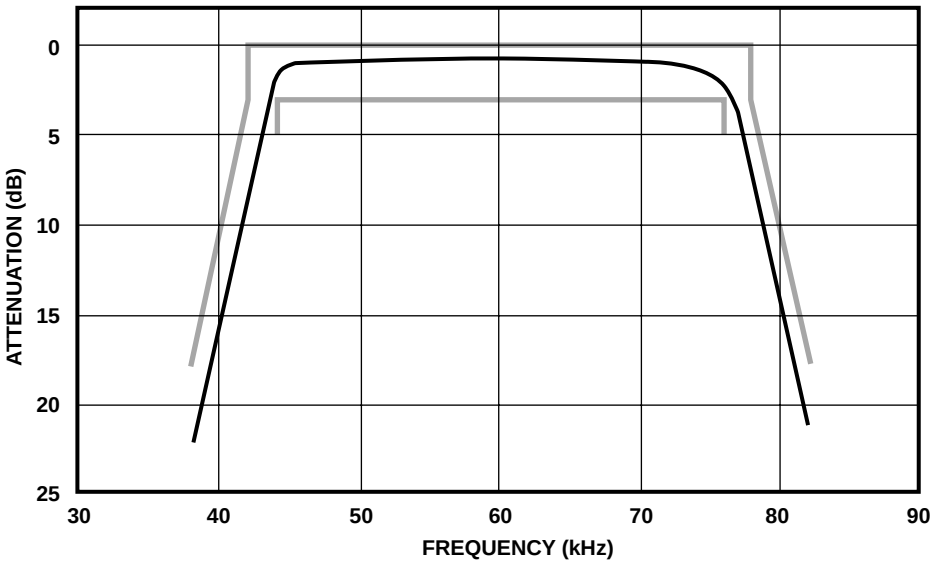


Figure 5b Passband detail

Figure 5 - Bandpass filter response

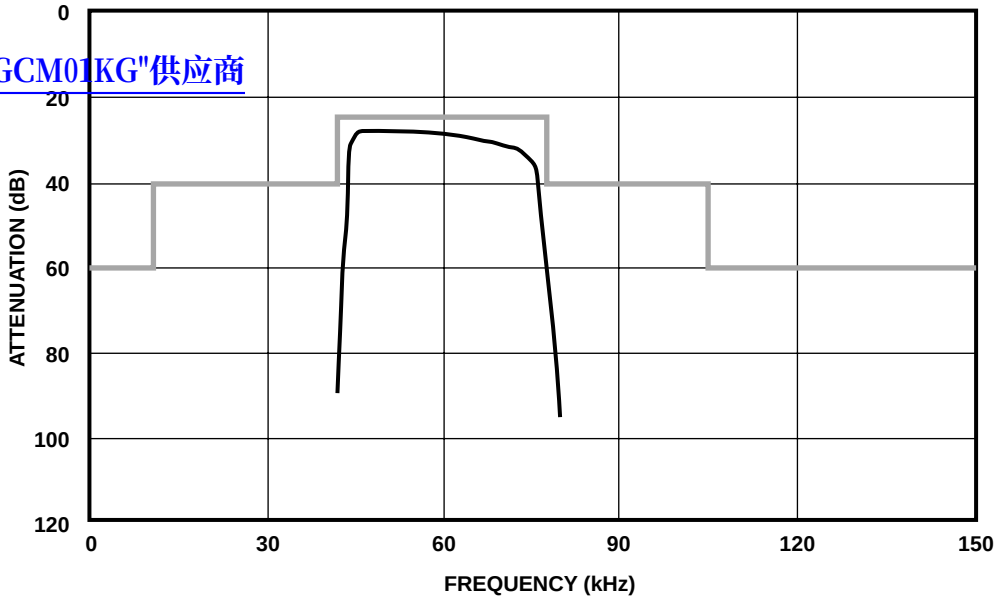


Figure 6 - Bandpass filter image response

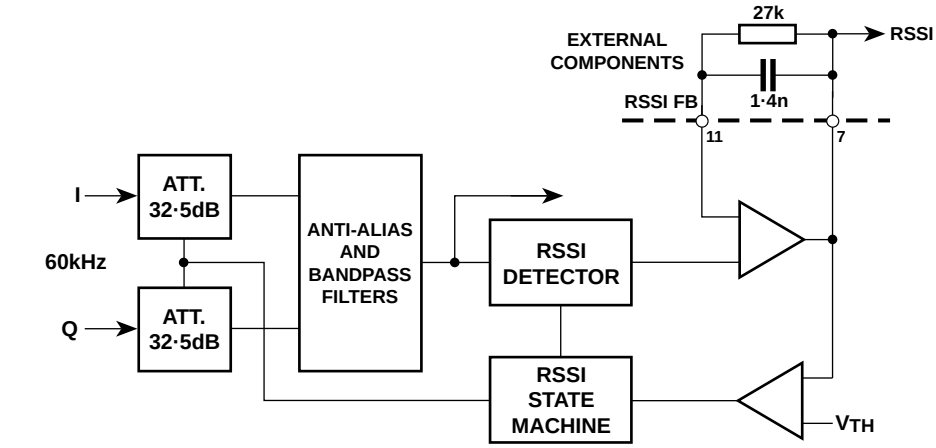


Figure 7 - RSSI block diagram

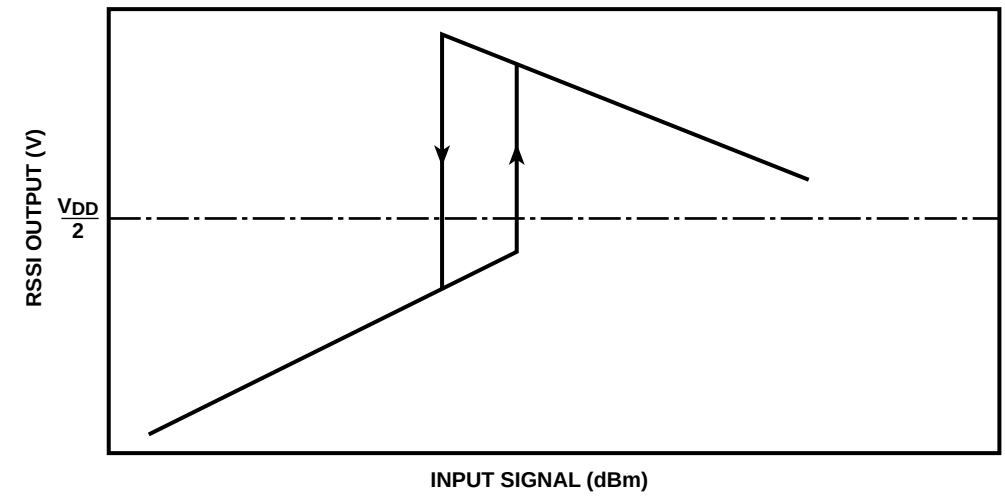


Figure 8 - RSSI characteristic

TRANSMIT

TDMA IS136 Mode I/Q Modulation

The inputs to the MGCM01 are derived from baseband D to A converters. These signals are passed through variable gain buffers. The gain of the buffers can be programmed from 0 to 12 dB in 3 dB increments, as shown in Table 9, allowing compatibility with a number of baseband and transmit modulator devices.

The buffers are followed by reconstruction filters to remove spurious responses from preceding D to A converters. These filters are third order Butterworth with 25kHz cut off frequency. The filters contain automatic calibration to set the cut off frequency. This can be controlled via the serial programming bus.

All inputs and outputs are differential

AMPS FM Mode

In this mode the input can be either a single ended or differential signal from a baseband D to A converter. The output is a single ended signal and is used to directly modulate the transmit IF. The signal path is the same as for I/Q mode but with only the I channel active and the Q channel powered down. The I+, Q+ outputs are switched high and the I-, Q- outputs are switched low to set the modulator in the Zarlink Semiconductor MGCT02 (Moon) chip to FM mode.

SYNTHESISERS

Two VHF PLL synthesisers are included for the generation of receive and transmit IF LO signals. The synthesisers are compatible with the VCO and prescaler circuits on the Zarlink Semiconductor MGCT02 and MGCR01 devices. The two synthesisers are identical.

The synthesisers include 2-modulus prescalers with programmable division ratio from 8/9 to 128/129, as detailed in Table 11, followed by an 11-bit programmable counter and 7-bit swallow counter to control the 2-modulus prescaler. The reference divider is a fully programmable 15-bit counter. The reference frequency is a 19·44MHz TCXO.

The synthesiser charge pumps can be programmed to four current levels, as shown in Table 12, to drive the appropriate loop filters.

The synthesisers also provide lock detect outputs. There is also a UHF LOCK input, pin 25, which can be connected to the system UHF synthesiser and is then gated with MGCM01 lock detect to give a combined output to the baseband controller via LOCK DETECT output, pin 38. This logic can use either the receive or transmit lock detect as selected via the serial bus.

PROGRAMMING

The MGCM01 features very flexible programming via the 3-wire serial bus. Data is clocked in 24-bit words with a latch pulse following the final data bit. The latch input must be held low at all other times.

The serial bus not only programs the modes of operation but also enables unused sections of the chip to be powered on and off as required. This is particularly important in a TDMA system when the phone does not receive or transmit all of the time. An added feature is the PCA (Power Control Assert), pin 45, which allows the MGCM01 to alternate between receive and transmit modes without reloading cammands via the serial bus and give more accurate timing.

Details of the serial bus are shown in Table 4. A total of 8 words can be programmed but some of these are for test purposes only and are not required in normal applications.

The programming is described in more detail in the following sections. Serial bus timing is shown in the Electrical Characteritics and Figure 3.

Word	Bit																						
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	X	X	X	RXDIV<17:0>																		0	0	0
2	X	X	X	TXDIV<17:0>																		0	0	1
3	X	X	X	0	TLI	RLI	REFRX<14:0>															0	1	0
4	X	X	X	0	0	TPP	REFTX<14:0>															0	1	1
5	X	X	X	RPP	0	0	TPR<2:0>			RPR<2:0>			TTC	RTC	TCP<1:0>		RCP<1:0>		LDC	0	0	1	0	0
6	X	X	X	X	X	X	X	X	X	0	TXG<2:0>			TXC	TX<1:0>		X	TC<3:0>				1	0	1
7	X	X	X	0	0	0	PCS<2:0>			X	X	RSS	RX	X	CONT<3:0>				X	X	X	1	1	0
8	CALCO<7:0>									TEST								0	X	X	X	1	1	1

Table 4 Serial bus details

X	Not used
RXDIV<17:0>	Receive synthesiser (LO2) division ratio
TXDIV<17:0>	Transmit synthesiser division ratio
REFRX<14:0>	Receive synthesiser reference division ratio
REFTX<14:0>	Transmit synthesiser reference division ratio
RCP, TCP<1:0>	Receive/Transmit synthesiser charge pump current control
RTC, TTC	Receive/Transmit synthesiser charge pump tristate control
RPR, TPR<2:0>	Receive/Transmit synthesiser prescaler ratio
RPP, TPP	Receive/Transmit synthesiser phase detector polarity
TLI, RLI	Receive/Transmit lock detect invert
LDC	Lock detect select
TX<1:0>	Transmit control
PCS<2:0>	Power Control system
RX	Receive mode
TXG<2:0>	Transmit gain
RSS	RSSI control
CONT<3:0>	Receive control
TXC	Transmit calibrate
TC<3:0>	Transmit calibrate control - set to 1000
CALCO<7:0>	Sets transmit cut off frequency - set to 00001100 for standard 25kHz cutoff

Receive Programming

The MGCM01 has two basic receive modes:

1. **I/Q mode.** The 60 kHz IF signal is mixed down to baseband I and Q signals. This mode is used for IS136 TDMA and may also be used for AMPS.

2. **FM mode.** The baseband I/Q path is powered down and the MGCM01 discriminator is used for demodulation. This mode can be used for AMPS.

These modes are selected by the RX mode bit, Word 7, Bit 11 as shown in Table 5.

RX	Mode
0	I/Q
1	FM

Table 5

Additional control is provided by the receive control bits, Word 7 Bits 9:6 (CONT<3:0>). CONT<2> sets the bandwidth of the 60 kHz bandpass filter. The low bandwidth mode (CONT<2> = 1) should be used for FM mode. However, the higher bandwidth mode (±20 kHz) may be used in TDMA operation.

The input attenuator control CONT<3> is active with RSS set to 1 and inactive if RSS is set to 0, as described in the next section.

CONT<3:0>				Mode
X	X	0	0	56dB gain (default)
X	0	X	X	±20kHz bandwidth
X	1	X	X	±16kHz bandwidth
0	X	X	X	Attenuator enabled
1	X	X	X	Attenuator disabled

Table 6

RSS Word 7 Bit 12 allows manual control of the input attenuator in conjunction with CONT<3>.

RSS	Operation
0	Normal attenuator mode
1	Manual attenuator

Table 7

Transmit Programming

MGCM01 has two basic transmit modes.

1. **I/Q mode.** I and Q signals from baseband digital to analog converter are filtered and buffered. This mode is used for IS136 TDMA.

2. **FM mode.** This is used for direct FM modulation of transmit IF oscillator.

These modes are controlled by TX <1:0>, Word 6 Bits 9 to 8, as shown in Table 8.

TX<1:0>		Mode
0	0	TDMA
1	0	FM

Table 8

A calibration of the transmit filters can be initialised by setting TXC, Word 6 Bit 10 to 1. After calibration the internal register for this bit is reset to 0.

The transmit gain can be programmed by TXG<2:0>, Word 6 Bits 13 to 11, as shown in Table 9.

TXG<2:0>			Gain (dB)
X	X	1	0
0	0	0	3
0	1	0	6
1	0	0	9
1	1	0	12

Table 9

Transmit Calibration

This is initiated by setting TXC, Word 6 Bit 10 high. Calibration takes approximately 0.6ms. In order for the calibration to give the required cutoff, CALCO<7:0> Word 8 Bits 23 to 16, must be set to 00001100. The calibration code is then stored in TC<3:0>, Word 6 Bits 6 to 3 and TXC is reset low. If TC<3:0> is overwritten then a further calibration is required.

Synthesiser Programming

The receive and transmit synthesisers are of a similar design and use identical programming. Each synthesiser includes a dual modulus (N, N+1) prescaler followed by A and M counters giving a total division ratio of MN+A, where
M is an 11-bit number
A is a 7-bit number
N is the prescaler modulus; this can also be programmed.

The value of A must be less than N.

The A and M values are combined to give the RXDIV, TXDIV values in Words 1 and 2.

Receive Synthesiser

The M value is programmed in Word 1 Bits 20 to10; the A value is programmed in Word 1 Bits 9 to 3

The reference divider REFRX, a 15-bit number, is programmed in Word 3 bits 17 to 3. The dual modulus prescaler is programmed by RPR<2:0>, Word 5 Bits 14:12, as shown in Table 10

RPR<2:0>			Prescaler ratio
0	X	X	8/9
1	0	0	16/17
1	0	1	32/33
1	1	0	64/65
1	1	1	128/129

Table 10

Transmit Synthesiser

The M value is programmed in Word 2 Bits 20 to 10; the A value is programmed in Word 2 Bits 9 to 3.

The reference divider REFTX, a 15-bit number, is programmed in Word 4 Bits 17 to 3.

The dual modulus prescaler is programmed by TPR<2:0>, Word 5 Bits 17 to 15, as shown in Table 11.

TPR<2:0>			Prescaler ratio
0	X	X	8/9
1	0	0	16/17
1	0	1	32/33
1	1	0	64/65
1	1	1	128/129

Table 11

Synthesiser Control

The transmit and receive synthesiser control programming is independent but has the same format.

Charge Pump Current

Four charge pump currents for each synthesiser can be programmed using RCP<1:0> and TCP<1:0>, Word 5 Bits 7 to 6 and Bits 9 to 8 respectively, as shown in Table 12. This allows additional flexibility when optimising loop filters and overall synthesiser performance.

RCP/TCP<1:0>		Current (μA)
0	0	496
0	1	176
1	0	96
1	1	16

Table 12

Charge Pump Output control

The charge pump can be inverted using RPP, Word 5 Bit 20 for the receive synthesiser and TPP, Word 4 Bit 18 for the transmit synthesiser as shown in Table 13.

RPP/TPP	Mode
0	Normal
1	Inverted

Table 13

The charge pump outputs can also be put into a high impedance inactive state using RTC and TTC, word 5 Bits 11 and 10 respectively as shown in Table 14.

RTC/TTC	Mode
0	Normal
1	High impedance

Table 14

Lock Detect Output Polarity

The Lock detect output polarity can be inverted using RLI/ TLI, Word 3 Bits 18 and 19, respectively as shown in Table 15. In normal operation lock detect outputs are high when locked.

RLI/TLI	Mode
0	Normal
1	Invert

Table 15

Lock Detect Output Control

The receive or transmit lock detect output can be selected for gating with the UHF LOCK input using the LDC bit, Word 5 Bit 5, as shown in Table 16.

LDC	Mode
0	Rx lock
1	Tx lock

Table 16

The gating for the total lock detect function is shown in Table 17. The RLI and TLI bits should be set to 0. The combined lock detect output is available on Pin 38.

UHF lock	RX/TX lock	LOCK DET	Mode
0	X	0	UHF unlocked
1	0	0	UHF locked, TX or RX unlocked
1	1	1	All PLLs locked

Table 17

Power Control

The MGCM01 features flexible power control using the PCS<2:0> Word 7, Bits 17 to 15 (see Table 18), using the serial bus in conjunction with the PCA pin.

PCS<2:0>			Mode
0	0	0	Deep Sleep
1	0	0	Sleep
0	1	0	TX
1	1	0	RX
0	0	1	Duplex
1	0	1	Alt RX/TX
0	1	1	RSSI on
1	1	1	RSSI off

Table 18

Description of Power Control Modes

Deep Sleep In this mode all circuitry is powered down except the power control circuits.

Sleep As deep sleep but voltage reference circuits active.

RX Receive Channel powered on. Operates in conjunction with RX mode control.

TX Transmit Channel powered on. Operates in conjunction with TX mode control.

Duplex Receive and Transmit channels active.

Alt RX/TX Receive and transmit under control of PCA. Receive on when PCA = 0, Transmit on when PCA = 1

RSSI On RSSI circuitry is activated when receive mode subsequently selected. This mode must be selected if RSSI or FM mode is required before setting RX or Duplex mode.

RSSI Off RSSI circuitry off when receive mode selected.

These power control modes are activated by the PCA pin. The PCA pin must normally be held high whilst a power control instruction is loaded via the serial bus. The exception is the Alt RX/TX mode which is loaded while PCA is low. The receive and transmit modes can then be toggled with the PCA pin.

Application

The MGCM01 requires a minimal number of external components in a typical application. The TCXO input should be AC coupled using a 10nF capacitor. Internal currents in the device are set by a reference resistor connected from pin 48 to ground. The recommended value for this resistor is 100kΩ. External components on the discriminator and RSSI pins control the output characteristics of these functions. The recommended components are shown in Figures 9 and 10.

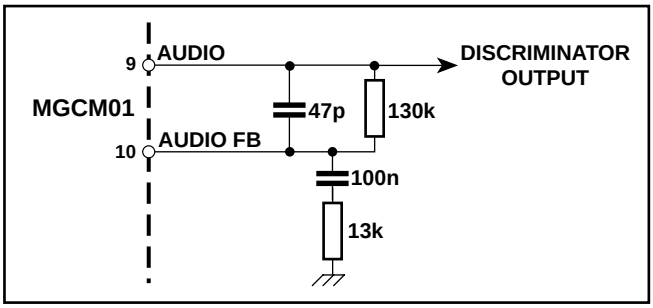


Figure 9 - Discriminator output components

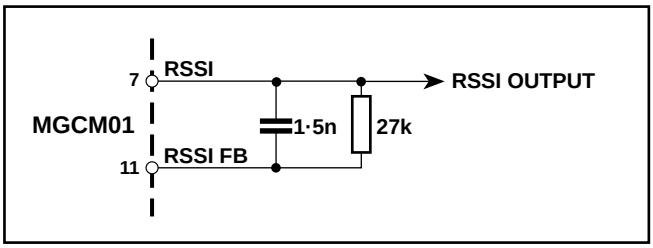


Figure 10 - RSSI output components

Figure 11 shows The MGCM01 operating in a typical IS136 mobile telephone application. This application uses the MGCR01 IF amplifier with AGC and the MGCT02 quadrature modulator and transmit up converter. These devices are part of Zarlink Semiconductor's Planet chipset.

The output from the IF filter is amplified in the MGCR01 IF amplifier which also down-converts to 60kHz differential I and Q signals which are then capacitively coupled to the MGCM01. Gain control for MGCR01 is provided from the baseband controller. MGCR01 includes an oscillator to provide the local oscillator for the quadrature down conversion.

This oscillator normally operates at twice the required LO frequency: an on-chip prescaler divides the oscillator frequency by 4; the prescaler output is used with the MGCM01 PLL.

In TDMA mode the AGC should maintain the MGCM01 input signals at typically 0·5mV. The MGCM01 then provides filtering, amplification and finally quadrature modulation down to baseband I and Q signals, which are directly coupled to baseband analog to digital converters. This mode can also be used for FM if I/Q demodulation is being used.

The on-chip limiting amplifier and discriminator can be used for AMPS FM demodulation. In this mode MGCR01 AGC is fixed to give an input to MGCM01 of typically 0·1 mV. The 60 kHz I and Q signals are filtered and then combined and passed through the limiting amplifier and discriminator. The components shown in Figure 9 provide feedback around the audio output amplifier and are effectively a bandpass filter. An RSSI output is also generated: the external components shown in Figure 10 set the slope and response time for the RSSI characteristic. These component values are recommended as they provide optimum response time and hysteresis.

In the transmit path modulated I and Q signals from baseband digital to analog converters are buffered and filtered. For TDMA mode these are output as I and Q signals to the quadrature modulator inputs of the MGCT02. This modulates an intermediate frequency which is then up-converted to the required RF transmit frequency. For FM mode a single ended output is provided which can be used to directly modulate the MGCT02 oscillator tank circuit.

The transmit IF is generated by an oscillator on Moon with an external tank circuit. For IS136 applications this oscillator normally runs at twice the IF frequency and is divided by 2 to generate the IF. A divide by eight prescaler divides the oscillator frequency and provides an output which together with the transmit synthesiser on the MGCM01 controls the IF.

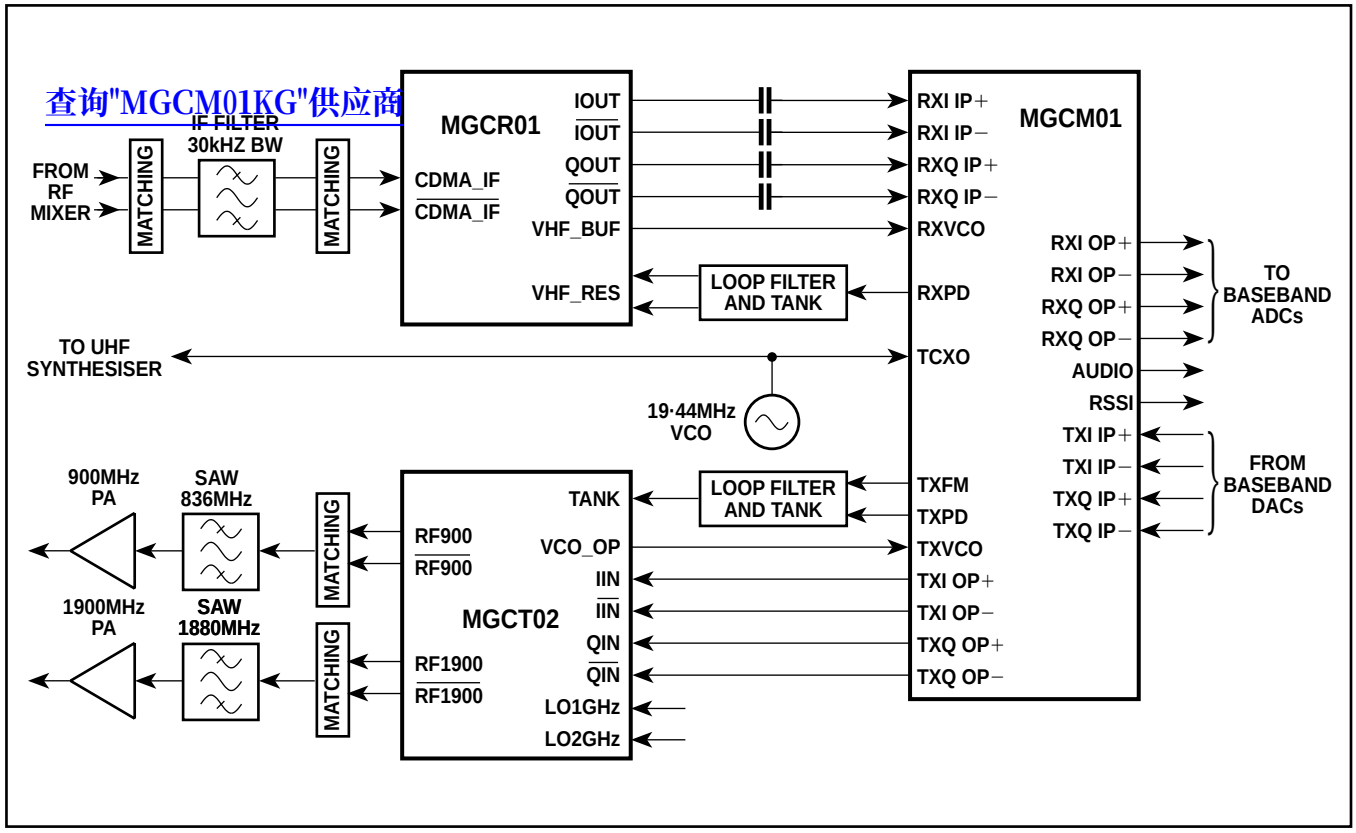
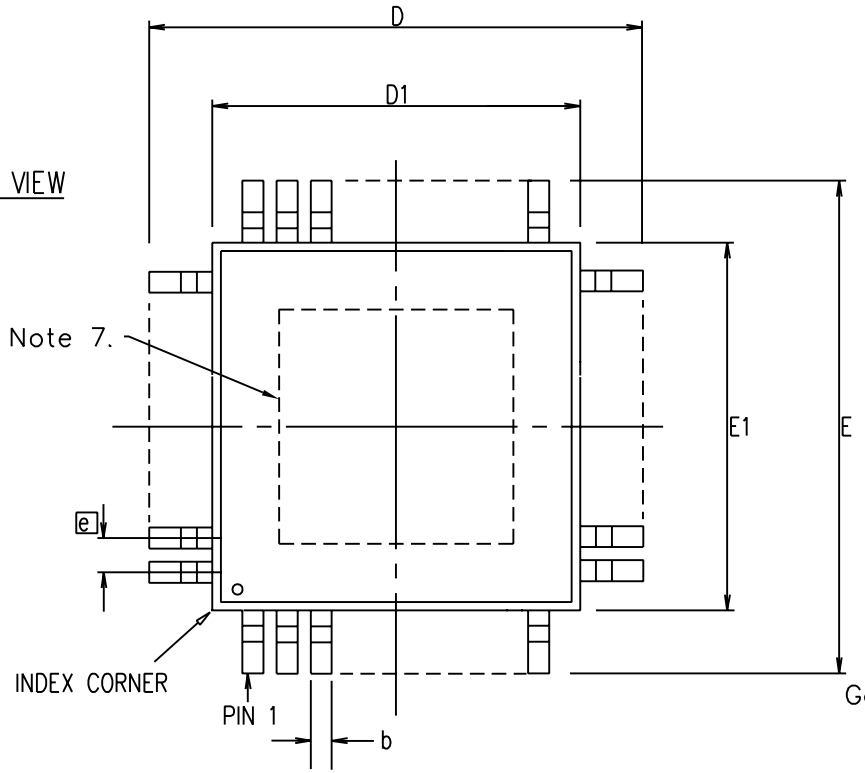
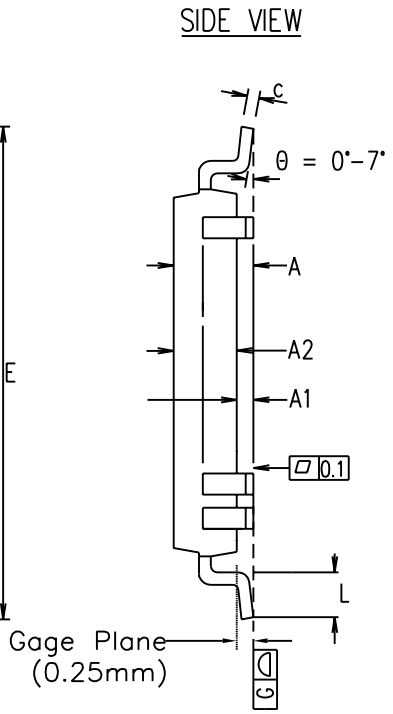


Figure 11 - Typical IS136 application

For more information about all Zarlink products visit our Web Site at

www.zarlink.com





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.20		---	0.047
A1	0.05	0.15		0.002	0.006
A2	0.95	1.05		0.037	0.041
D	9.00 BSC			0.354 BSC	
D1	7.00 BSC			0.276 BSC	
E	9.00 BSC			0.354 BSC	
E1	7.00 BSC			0.276 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	48				
ND	12				
NE	12				
NOTE	SQUARE				

Conforms to JEDEC MS-026 ABC Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity measured at seating plane G, to be 0.08 mm max.
7. Dashed area represents exposed paddle for e-PAD Packages only.
   - See leadframe drawing for e-Pad dimension.
   - Metal area of exposed die pad shall be within 0.30mm of nominal pad size.

This drawing supersedes 418/ED/51612/002 (Swindon)

1	2	3	4
201365	207083	208007	212441
28Oct96	6Jul99	14Dec99	25Mar02

ZARLINK SEMICONDUCTOR

Previous package codes
TP / TH / F

Package Code QD

Package Outline for 48 lead TQFP / E-Pad TQFP (7x7x1.0mm) 2.0mm Footprint

GPD00249

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