

16-bit edge triggered D-type flip-flop (3-State)

[查询 74AC16374DGG 供应商](#)

74AC16374

74ACT16374

FEATURES

- 74ACT16374 has TTL-compatible inputs
- 74AC16374 has CMOS-compatible inputs
- 3-State outputs source/sink 24mA
- 3-State outputs drive bus lines or buffer memory address registers
- Distributed power and ground pins for minimum noise and ground bounce

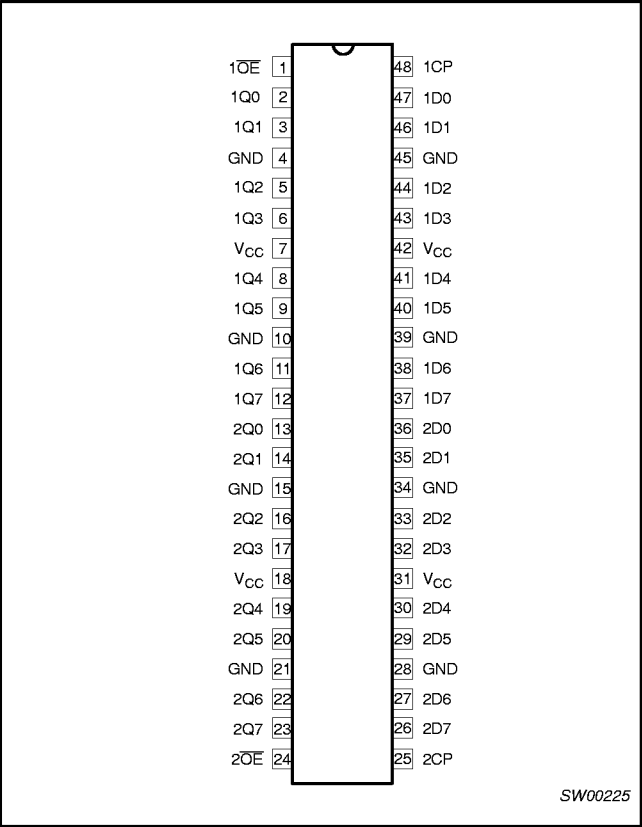
DESCRIPTION

The 74AC16374/74ACT16374 is a 16-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. The '16374' consists of 2 sections of eight edge-triggered flip-flops. A clock (CP) input and an output enable ($\overline{OE}$) are provided for each octal.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; t_r = t_f ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL			UNIT
			AC V _{CC} = 3.3V	AC V _{CC} = 5.0V	ACT V _{CC} = 5.0V	
t _{PHL} /t _{PLH}	Propagation delay CP to Q _n	C _L = 50pF	4.2	2.9	4.6	ns
f _{max}	Maximum clock frequency	C _L = 50pF	160	200	180	MHz
C _I	Input capacitance		4.5			pF
C _{PD}	Power dissipation capacitance	V _I = GND to V _{CC} ¹				pF
		Outputs enabled ²	27			pF
		Outputs enabled ³	220			pF
		Outputs disabled ²	15			pF
		Outputs disabled ³	60			pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW): P_D = C_{PD} × V_{CC}² × f_i + ∑ (C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz; C_L = output load capacity in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V;
∑ (C_L × V_{CC}² × f_o) = sum of outputs.
2. Switch the clock and one data input such that one flip-flop toggles.
3. Switch the clocks and all data inputs such that all 16 flip-flops toggle.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	−40°C to +85°C	74AC16374 DL	7AC16374 DL	SOT370-1
		74ACT16374 DL	7AT16374 DL	
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74AC16374 DGG	7AC16374 DGG	SOT362-1
		74ACT16374 DGG	7AT16374 DGG	

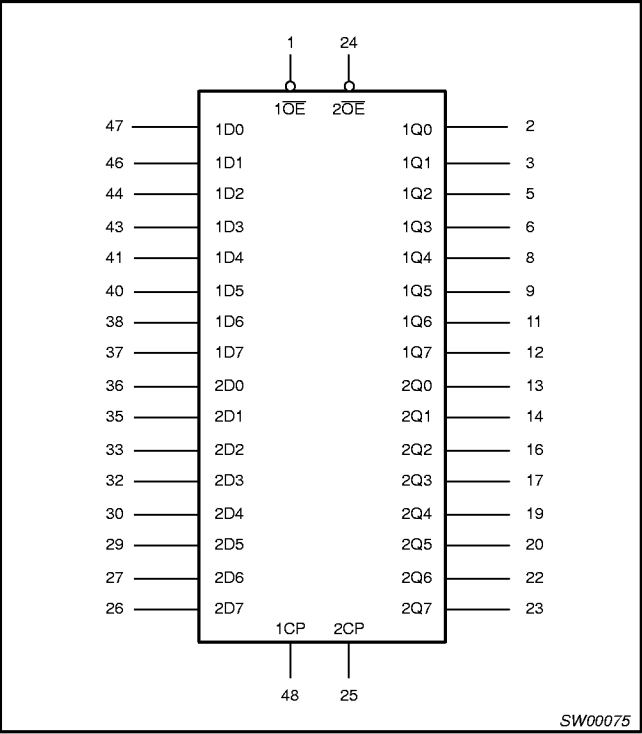
16-bit edge triggered D-type flip-flop (3-State)
[查询 74AC16374DGC 供应商](#)

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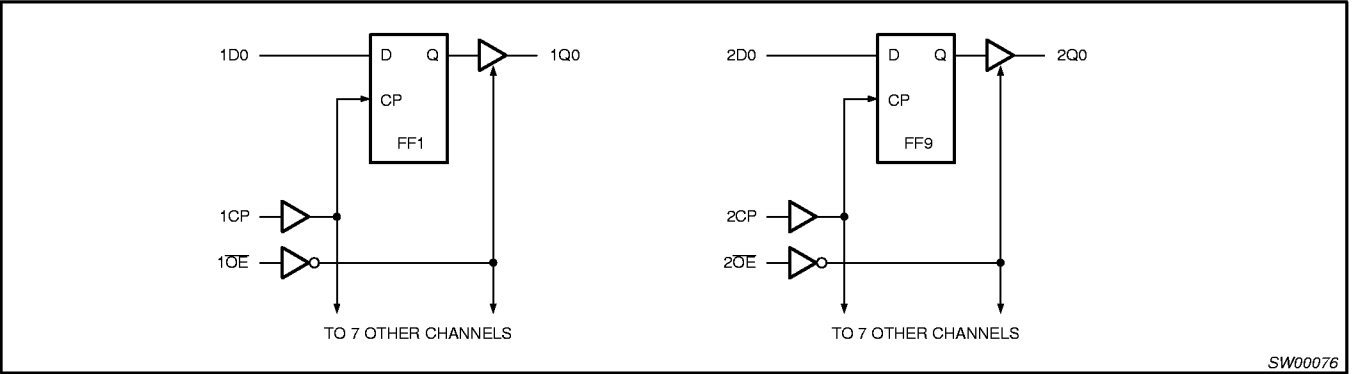
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1 $\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q1 to 1Q7	3-State flip-flop outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q1 to 2Q7	3-State flip-flop outputs
24	2 $\overline{OE}$	Output enable input (active LOW)
25	2CP	Clock input
36, 35, 33, 32, 30, 29, 27, 26	2D1 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D1 to 1D7	Data inputs
48	1CP	Clock input

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

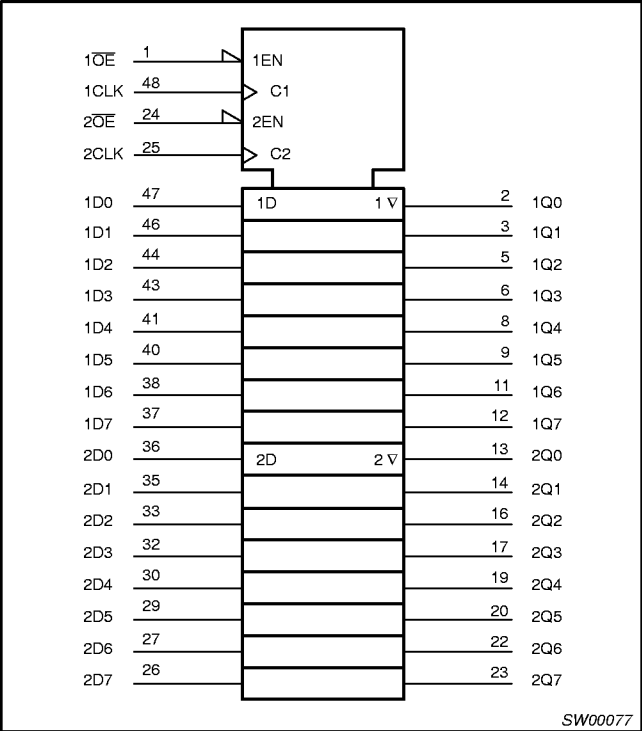
OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0 to Q7
Load and read register	L L	$\uparrow$ $\uparrow$	L h	L H	L H
Load register and disable outputs	H H	$\uparrow$ $\uparrow$	L h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
 $\uparrow$ = LOW-to-HIGH CP transition

16-bit edge triggered D-type flip-flop (3-State)
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74AC16374
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LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage for 'AC	2.0	6.0	V
V_{CC}	DC supply voltage for 'ACT	4.5	5.5	V
V_{IN}	DC input voltage range	0	V_{CC}	V
V_O	DC output voltage range	0	V_{CC}	V
T_{amb}	Operating free-air temperature range	-40	+85	°C
$\Delta V/\Delta t$	Minimum input edge rate — AC devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125		

16-bit edge triggered D-type flip-flop (3-State)
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ABSOLUTE MAXIMUM RATINGS¹
in accordance with the Absolute Maximum Rating System (IEC134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _{IN} = −0.5V	−20	mA
		V _{IN} = V _{CC} + 0.5V	+20	
V _{IN}	DC input voltage		−0.5 to V _{CC} +0.5	V
I _{OK}	DC output diode current	V _O = −0.5V	−20	mA
		V _O = V _{CC} + 0.5V	+20	
V _O	DC output voltage		−0.5 to V _{CC} +0.5	V
I _O	DC output source or sink current		± 50	mA
I _{CC} , I _{GND}	DC V _{CC} or GND current per output		± 50	mA
I _{CC} , I _{GND}	DC V _{CC} or GND current		± 200	mA
T _{stg}	Storage temperature range		−65 to 150	°C
P _{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

- NOTES:**
- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

16-bit edge triggered D-type flip-flop (3-State)

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DC ELECTRICAL CHARACTERISTICS (74AC16374)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{OUT} = 0.1V or (V _{CC} – 0.1V)	3.0	2.1	1.5		V
			4.5	3.15	2.25		
			5.5	3.85	2.75		
V _{IL}	LOW level Input voltage	V _{OUT} = 0.1V or (V _{CC} – 0.1V)	3.0		1.5	0.9	V
			4.5		2.25	1.35	
			5.5		2.75	1.65	
V _{OH}	HIGH level output voltage	I _{OUT} = –50 μA	3.0	2.9	2.99		V
			4.5	4.4	4.49		
			5.5	5.4	5.49		
		V _{IN} = V _{IL} or V _{IH} ; I _{OH} = –12mA ¹	3.0	2.46			V
		V _{IN} = V _{IL} or V _{IH} ; I _{OH} = –24mA ¹	4.5	3.76			
		V _{IN} = V _{IL} or V _{IH} ; I _{OH} = –24mA ¹	5.5	4.76			
V _{OL}	LOW level output voltage	I _{OUT} = 50 μA	3.0		0.01	0.1	V
			4.5		0.01	0.1	
			5.5		0.01	0.1	
		V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 12mA ¹	3.0			0.44	V
		V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA ¹	4.5			0.44	
		V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA ¹	5.5			0.44	
I _{IN}	Input leakage current	V _{IN} = V _{CC} , GND	5.5			± 1.0	μA
I _{OZ}	3-State output OFF-state current	V _{IN} = V _{IL} , V _{IH} V _{OUT} = V _{CC} , GND	5.5			± 2.5	μA
I _{OLD}	Dynamic output current ²	V _{OLD} = 1.65V max	5.5	75			mA
I _{OHD}	Dynamic output current ²	V _{OHD} = 3.85V min	5.5			–75	mA
I _{CC}	Quiescent supply current	V _{IN} = V _{CC} or GND	5.5			80	μA

NOTES:

1. All outputs loaded
2. Maximum test duration 2.0 ms; one output loaded at a time

16-bit edge triggered D-type flip-flop (3-State)

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DC ELECTRICAL CHARACTERISTICS (74ACT16374)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{OUT} = 0.1V or (V _{CC} – 0.1V)	4.5	2.0	1.5		V
			5.5	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{OUT} = 0.1V or (V _{CC} – 0.1V)	4.5		1.5	0.8	V
			5.5		1.5	0.8	
V _{OH}	HIGH level output voltage	I _{OUT} = –50 μA	4.5	4.4	4.49		V
			5.5	5.4	5.49		
		V _{IN} = V _{IL} or V _{IH} ; I _{OH} = –24mA ¹	4.5	3.76	3.86		V
		V _{IN} = V _{IL} or V _{IH} ; I _{OH} = –24mA ¹	5.5	4.76	4.86		
V _{OL}	LOW level output voltage	I _{OUT} = 50 μA	4.5		0.01	0.1	V
			5.5		0.01	0.1	
		V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA ¹	4.5			0.44	V
		V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA ¹	5.5			0.44	
I _{IN}	Input leakage current	V _{IN} = V _{CC} , GND	5.5			± 1.0	μA
I _{OZ}	3-State output OFF-state current	V _{IN} = V _{IL} , V _{IH} V _{OUT} = V _{CC} , GND	5.5			± 2.5	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{IN} = V _{CC} – 2.1V Other inputs at V _{CC} or GND; I _{OUT} = 0	5.5			1.0	mA
I _{OLD}	Dynamic output current ²	V _{OLD} = 1.65V max	5.5	75			mA
I _{OHD}	Dynamic output current ²	V _{OHD} = 3.85V min	5.5			–75	mA
I _{CC}	Quiescent supply current	V _{IN} = V _{CC} or GND	5.5			80	μA

NOTES:

- All outputs loaded
 - Maximum test duration 2.0ms, one output loaded at a time
- In accordance with the Absolute Maximum Rating System (IEC 134)

16-bit edge triggered D-type flip-flop (3-State)

[查询 74AC16374DCG 供应商](#)74AC16374
74ACT16374**AC CHARACTERISTICS (74AC16374)**GND = 0V; $t_r = t_f = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; .

SYMBOL	PARAMETER	V _{CC} ¹	LIMITS					UNIT	WAVEFORM
			T _{amb} = +25°C			T _{amb} = −40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t _{PLH}	Propagation delay CP to Q _n	3.3 5.0	2.0 1.5	4.2 2.9	9 7	1.5 1.0	10 8	ns	1, 4
t _{PHL}	Propagation delay CP to Q _n	3.3 5.0	2.0 1.5	4.2 2.9	9 7	1.5 1.0	10 8	ns	1, 4
t _{PZH}	3-State output enable time OE to Q _n	3.3 5.0	2.0 1.5	4.4 3.0	9 7	1.5 1.0	10 8	ns	2, 4
t _{PZL}	3-State output enable time OE to Q _n	3.3 5.0	2.0 1.5	4.3 3.0	9 7	1.5 1.0	10 8	ns	2, 4
t _{PHZ}	3-State output disable time OE to Q _n	3.3 5.0	2.0 1.5	3.3 2.2	8 6	1.5 1.0	9 7	ns	2, 4
t _{PLZ}	3-State output disable time OE to Q _n	3.3 5.0	2.0 1.5	4.1 2.9	8 6	1.5 1.0	9 7	ns	2, 4
t _w	CP pulse width HIGH or LOW	3.3 5.0	4.5 4.0	1.6 1.4		5 4.5		ns	3
t _{su}	Set-up time D _n to CP	3.3 5.0	1.5 1.5	0.2 0.2		2 2		ns	3
t _h	Hold time D _n to CP	3.3 5.0	1.0 1.0	0 0.2		1.5 1.5		ns	3
f _{max}	Maximum clock pulse frequency	3.3 5.0	100 150	160 200		90 140		MHz	

NOTE:

1. Voltage range 3.3V is $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$
Voltage range 5.0V is $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$

AC CHARACTERISTICS (74ACT16374)GND = 0V; $t_r = t_f = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; .

SYMBOL	PARAMETER	V _{CC} ¹	LIMITS					UNIT	WAVEFORM
			T _{amb} = +25°C			T _{amb} = −40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t _{PLH}	Propagation delay CP to Q _n	5.0	2.0	4.6	9	2.0	10	ns	1, 4
t _{PHL}	Propagation delay CP to Q _n	5.0	2.0	4.6	9	1.5	10	ns	1, 4
t _{PZH}	3-State output enable time OE to Q _n	5.0	2.0	4.3	9	1.5	10	ns	2, 4
t _{PZL}	3-State output enable time OE to Q _n	5.0	1.5	4.3	9	1.5	10	ns	2, 4
t _{PHZ}	3-State output disable time OE to Q _n	5.0	1.5	3.9	8	1.0	9	ns	2, 4
t _{PLZ}	3-State output disable time OE to Q _n	5.0	1.5	4.5	8	1.0	9	ns	2, 4
t _w	CP pulse width HIGH or LOW	5.0	4.0	1.6		4.5		ns	3
t _{su}	Set-up time D _n to CP	5.0	1.5	−0.2		2		ns	3
t _h	Hold time D _n to CP	5.0	1.5	0.4		2		ns	3
f _{max}	Maximum clock pulse frequency	5.0	120	180		110		MHz	

NOTE:

1. These values are at $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$

16-bit edge triggered D-type flip-flop (3-State)

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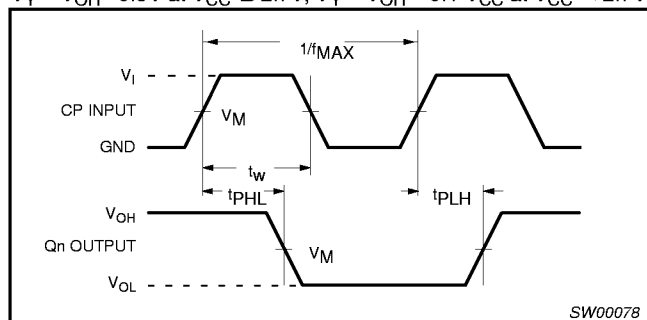
AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.

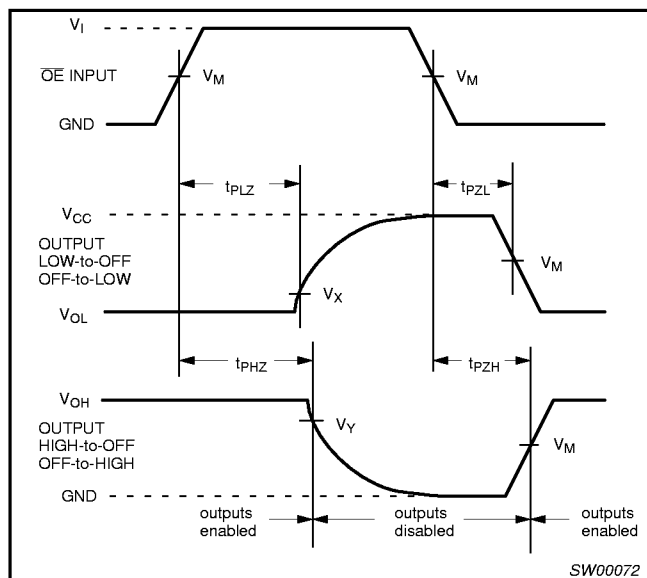
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$

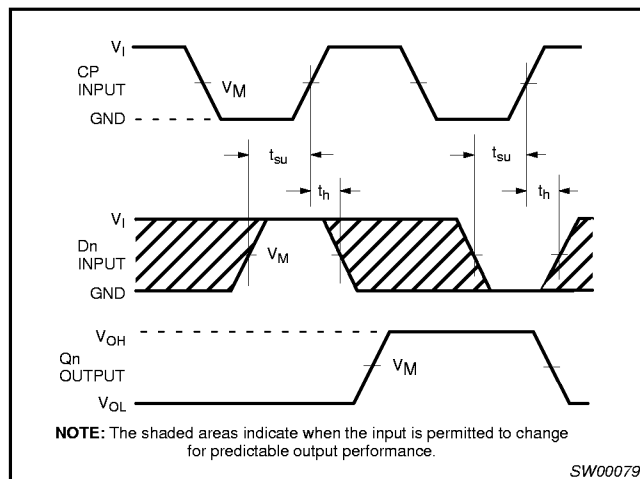
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$



Waveform 1. Clock (CP) to output (Qn) propagation delays, the clock pulse width and the maximum clock pulse frequency



Waveform 2. 3-State enable and disable times



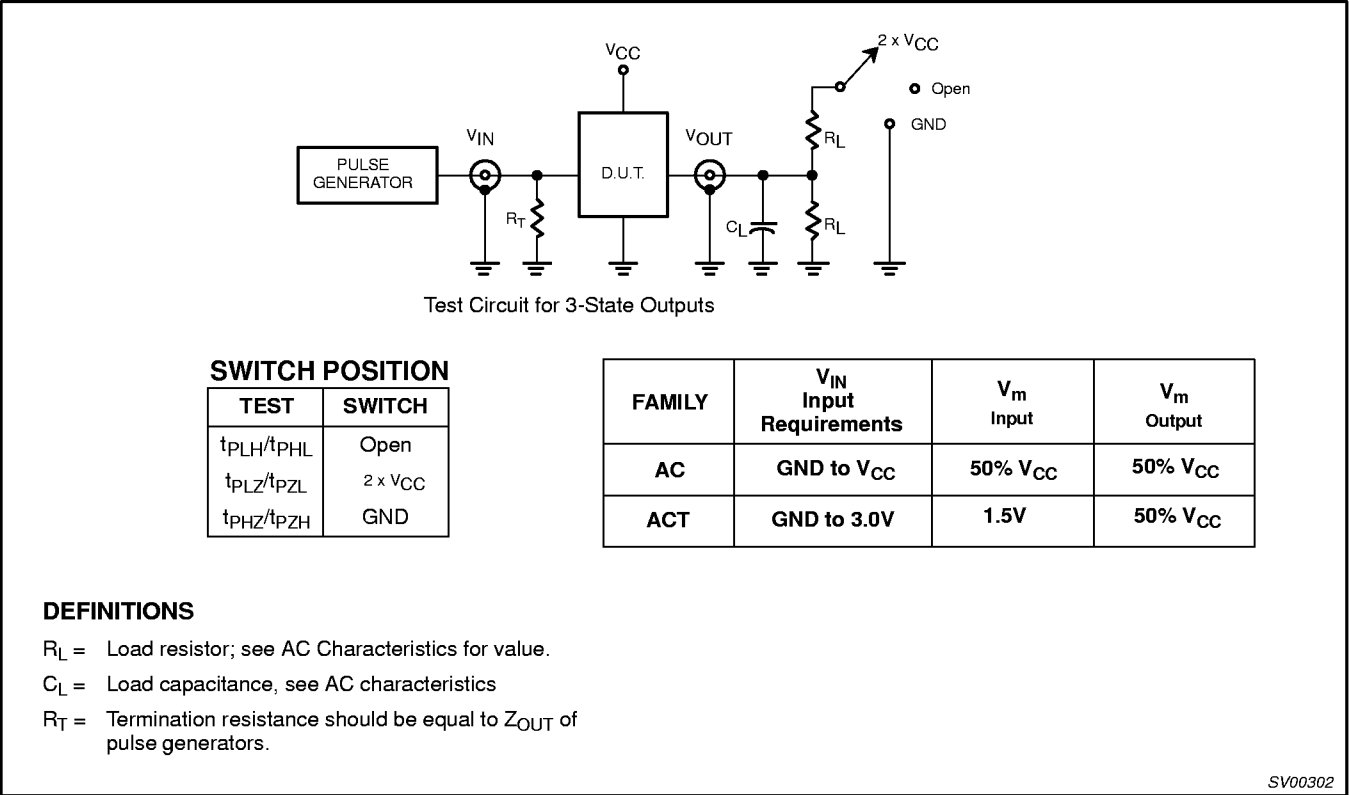
Waveform 3. Data set-up and hold times for the Dn input to the CP input

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[查询“74AC16374DTC”供应商](#)

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TEST CIRCUIT



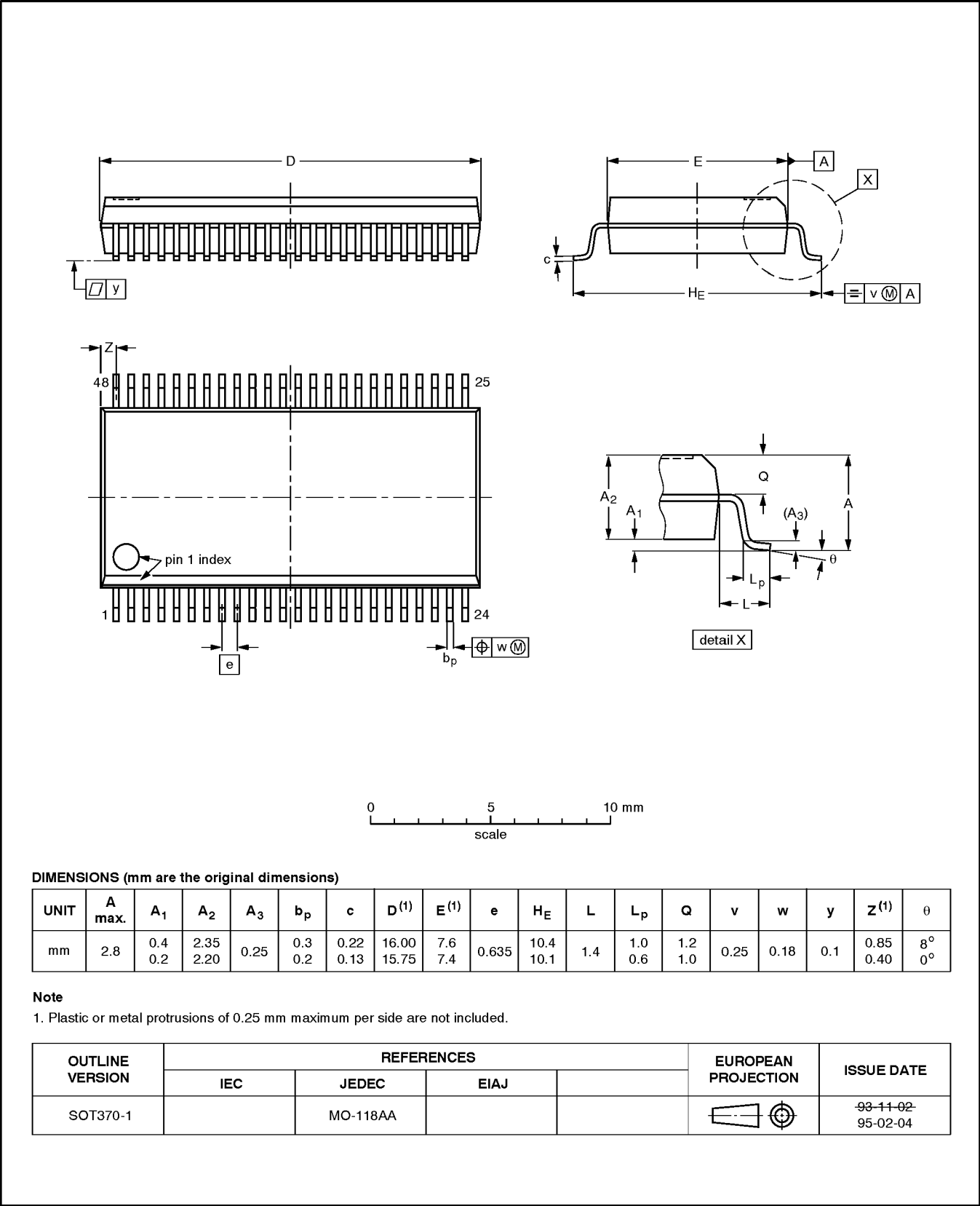
Waveform 4. Load circuitry for switching times

16-bit edge triggered D-type flip-flop (3-State)
[查询 74AC16374 Datasheet 供应商](#)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



16-bit edge triggered D-type flip-flop (3-State)

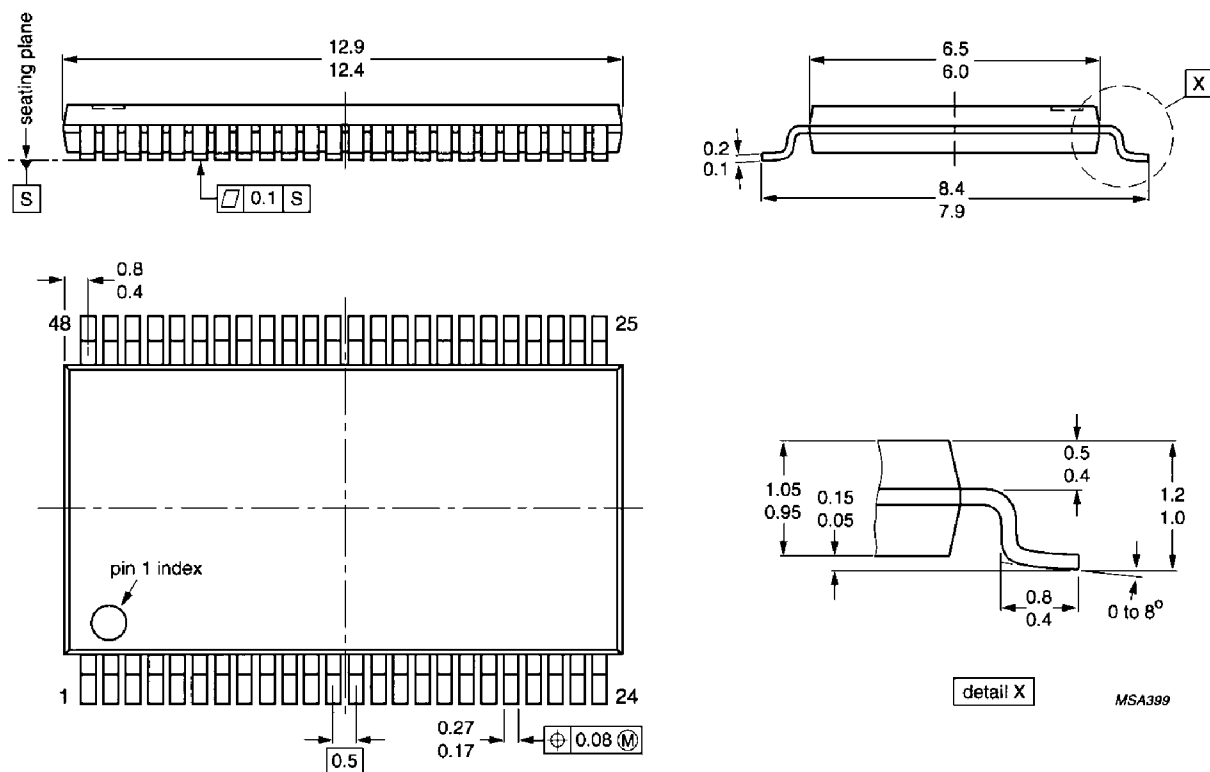
[查询 74AC16374 Datasheet 供应商](#)

74AC16374

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



Dimensions in mm.