



June 1998
Revised February 2001

74LCX112

Low Voltage Dual J-K Negative Edge-Triggered Flip-Flop with 5V Tolerant Inputs

General Description

The LCX112 is a dual J-K flip-flop. Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs with Q, Q outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V or 2.5) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX112 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

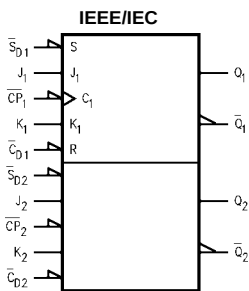
- 5V tolerant inputs
- 2.3V–3.6V V_{CC} specifications provided
- 7.5 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 2000V

Ordering Code:

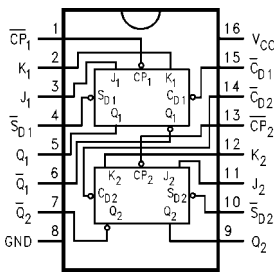
Order Number	Package Number	Package Description
74LCX112M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74LCX112SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX112MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
J ₁ , J ₂ , K ₁ , K ₂	Data Inputs
$\overline{CP_1}$, $\overline{CP_2}$	Clock Pulse Inputs (Active Falling Edge)
$\overline{CD_1}$, $\overline{CD_2}$	Direct Clear Inputs (Active LOW)
$\overline{SD_1}$, $\overline{SD_2}$	Direct Set Inputs (Active LOW)
Q ₁ , Q ₂ , $\overline{Q_1}$, $\overline{Q_2}$	Outputs

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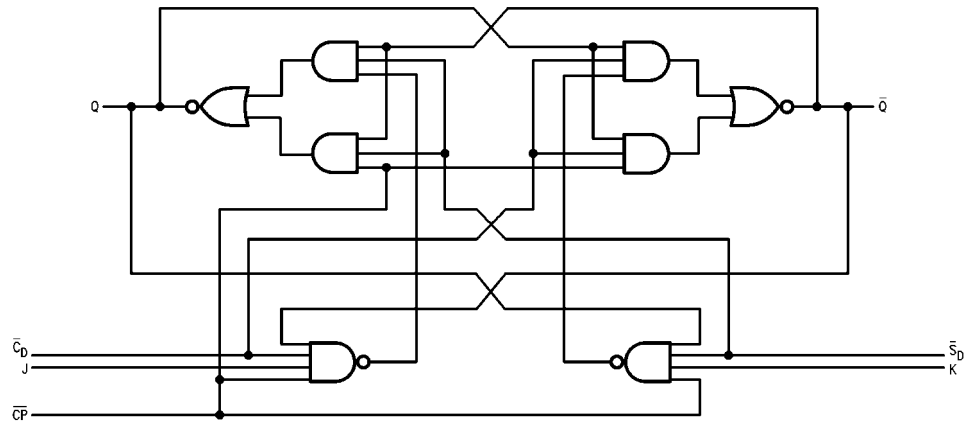
Truth Table

(Each half)

Inputs					Outputs	
$\overline{S_D}$	$\overline{C_D}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\sim$	h	h	$\overline{Q_O}$	Q_O
H	H	$\sim$	l	h	L	H
H	H	$\sim$	h	l	H	L
H	H	$\sim$	l	l	Q_O	$\overline{Q_O}$
H	H	H	X	X	Q_O	$\overline{Q_O}$

H(h) = HIGH Voltage Level
L(l) = LOW Voltage Level
X = Immaterial
 $\sim$ = HIGH-to-LOW Clock Transition
 $Q_O(\overline{Q_O})$ = Before HIGH-to-LOW Transition of Clock
Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram



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AC Electrical Characteristics								
Symbol	Parameters	T _A = 40°C to 85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L =50 pF		C _L = 50 pF		C _L =30 pF		
		Min	Max	Min	Max	Min	Max	
t _{MAX}	Maximum Clock Frequency	150		150		150		MHz
t _{PHL}	Propagation Delay	1.5	7.5	1.5	8.0	1.5	9.0	ns
t _{PLH}	$\overline{CP}_n$ to Q _n or $\overline{Q}_n$	1.5	7.5	1.5	8.0	1.5	9.0	
t _{PHL}	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t _{PLH}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q _n or $\overline{Q}_n$	1.5	7.0	1.7	8.0	1.5	8.4	
t _S	Setup Time	2.5		2.5		4.0		ns
t _H	Hold Time	1.5		1.5		2.0		ns
t _W	Pulse Width $\overline{CP}$	3.3		3.3		4.0		ns
t _W	Pulse Width ($\overline{C}_D$, $\overline{S}_D$)	3.3		3.3		4.0		ns
t _{REC}	Recovery Time	2.0		2.5		4.5		ns
t _{OSHL}	Output to Output Skew		1.0					ns
t _{OSLH}	(Note 4)		1.0					
Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t _{OSHL}), or LOW-to-HIGH (t _{OSLH}).								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		Units		
				Typical				
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	3.3 2.5	0.8 0.6		V		
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	3.3 2.5	−0.8 −0.6				
Capacitance								
Symbol	Parameter	Conditions	Typical		Units			
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7		pF			
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8		pF			
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	25		pF			

AC Loading and Waveforms Generic for LCX Family

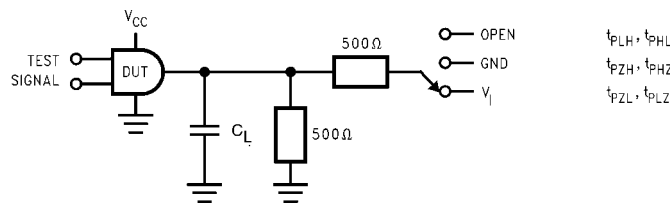
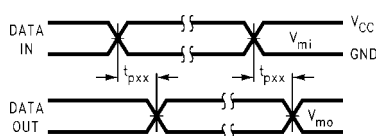
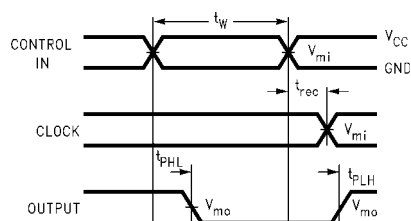


FIGURE 1. AC Test Circuit
(C_L includes probe and jig capacitance)

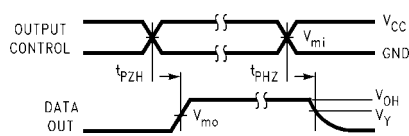
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND



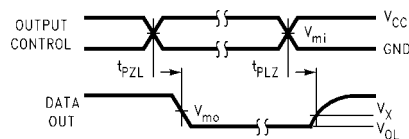
Waveform for Inverting and Non-Inverting Functions



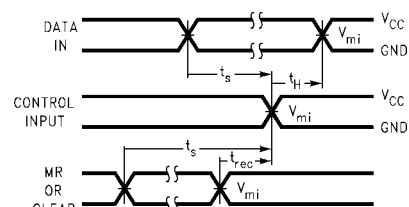
Propagation Delay, Pulse Width and t_{rec} Waveforms



3-STATE Output High Enable and Disable Times for Logic



3-STATE Output Low Enable and Disable Times for Logic



Setup Time, Hold Time and Recovery Time for Logic

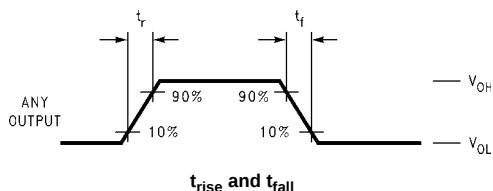
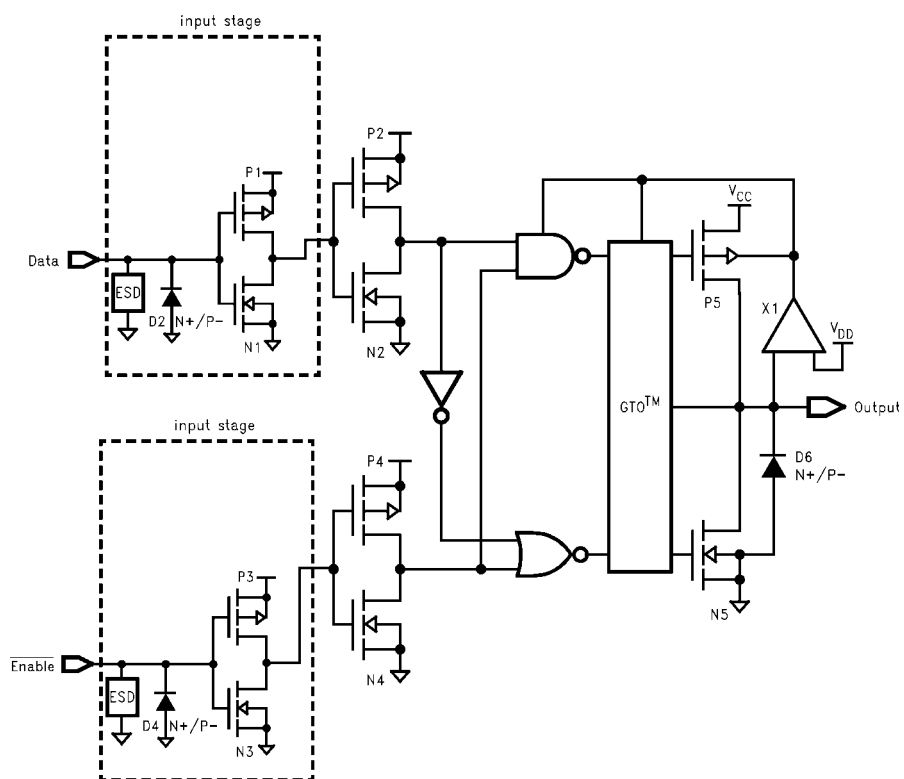


FIGURE 2. Waveforms
(Input Pulse Characteristics; $f=1MHz$, $t_r=t_f=3ns$)

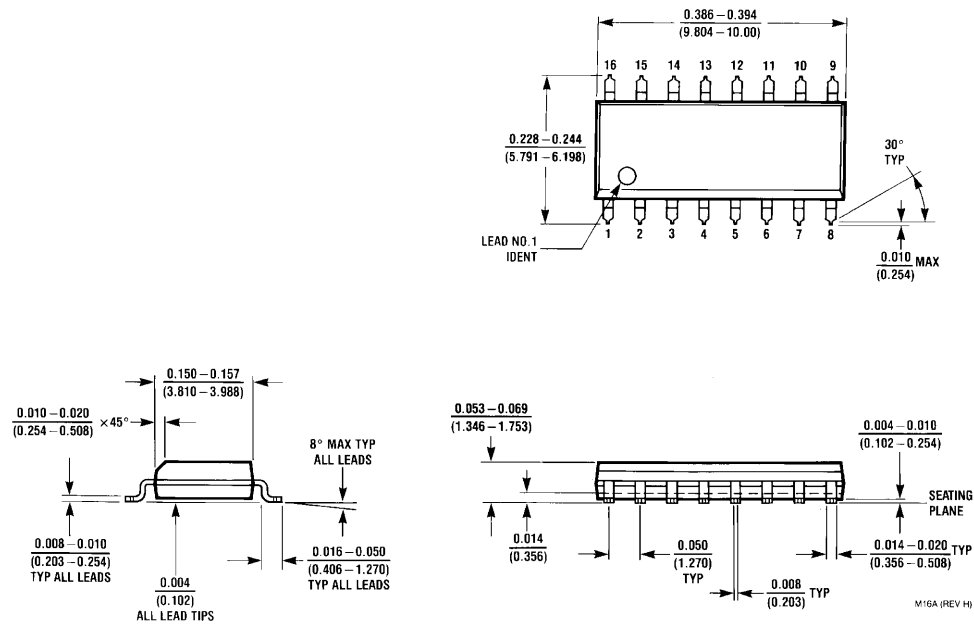
Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mI}	$1.5V$	$1.5V$	$V_{CC}/2$
V_{mO}	$1.5V$	$1.5V$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

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Schematic Diagram Generic for LCX Family



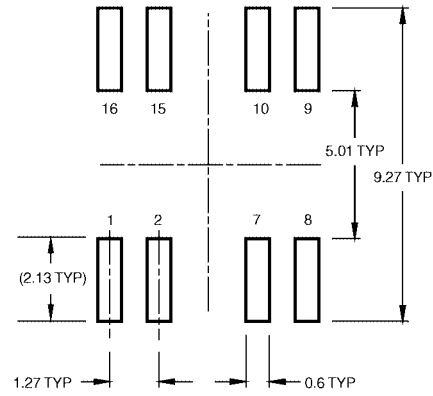
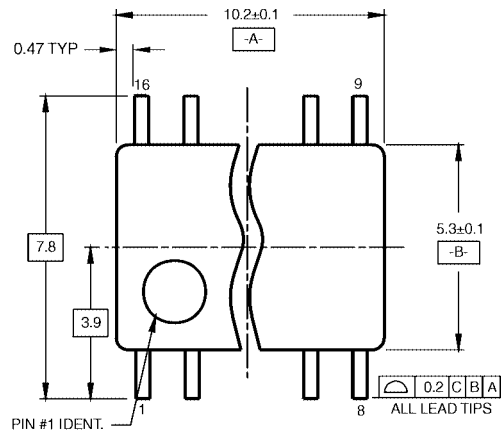
Physical Dimensions inches (millimeters) unless otherwise noted



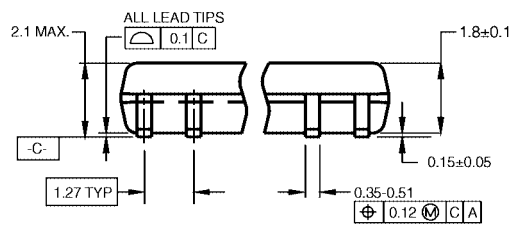
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A

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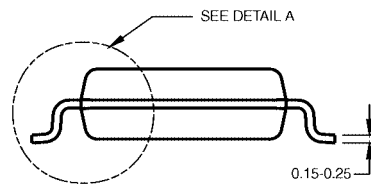
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



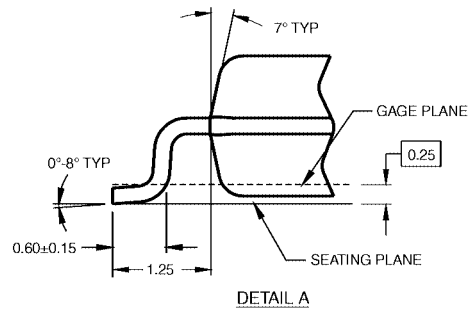
DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

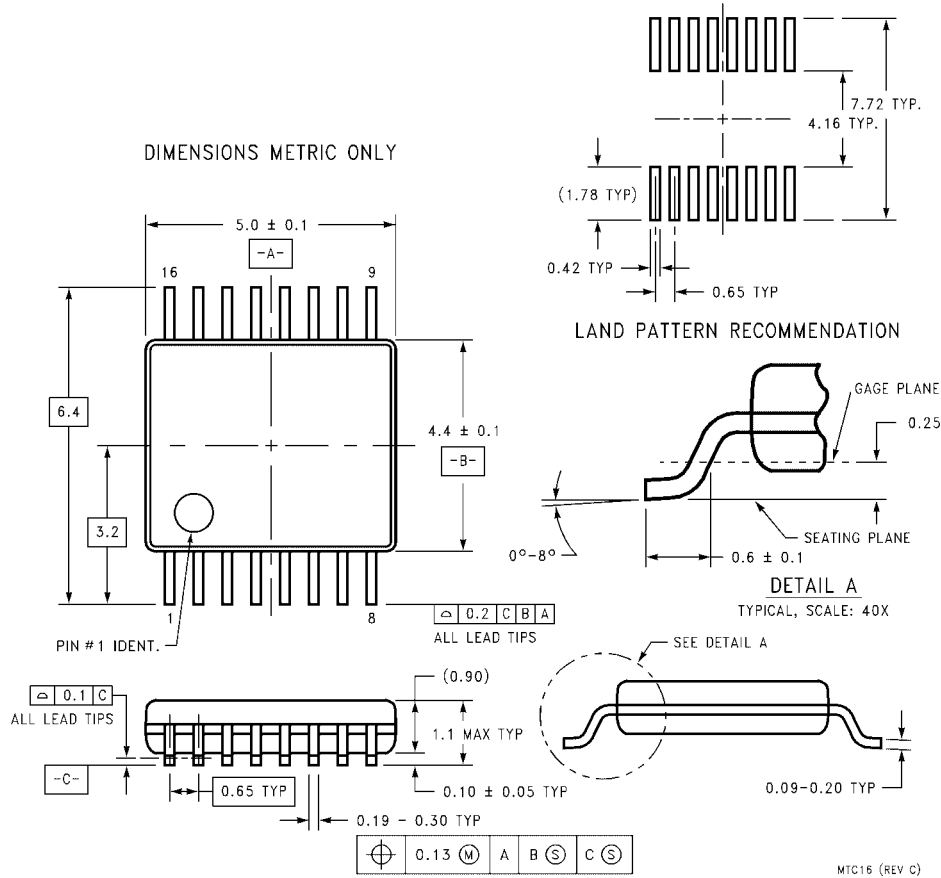
M16DRevB1



DETAIL A

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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