REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Added device type 03. Figure 1; Made corrections to the height dimensions for case outlines Y and Z. Added Figure 2; Terminal connections table. Redrew entire document. -sld.	00-01-31	Raymond Monnin

The original first page of this drawing has been replaced

REV																				
SHEET																				
REV	D	D	D	D	D															
SHEET	15	16	17	18	19															

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Donald R. Osborne	**DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY D. A. Dicenzo	
	APPROVED BY N. A. Hauck	MICROCIRCUIT, HYBRID, LINEAR, DUAL REDUNDANT, REMOTE TERMINAL UNIT (RTU)
	DRAWING APPROVAL DATE 87-08-06	
	REVISION LEVEL D	SIZE: A; CAGE CODE: **67268**; **5962-87535**
		SHEET 1 OF 19

DSCC FORM 2233
APR 97

5962-E280-99

1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits to be processed in accordance with MIL-PRF-38534.

1.2 PIN. The PIN shall be as shown in the following example:

5962-87535	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	BUS-65112	Dual redundant remote terminal (RTU)
02	2452	Dual redundant remote terminal (RTU)
03	CT2512	Dual redundant remote terminal (RTU)

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	78	Hybrid package
Y	See figure 1	82	Flat package
Z	See figure 1	82	Flat package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Logic Supply voltage (V_L)	5.5 V dc
Positive supply voltage (V_{CC})	18.0 V dc
Negative supply voltage (V_{EE})	-18.0 V dc
Storage temperature range	-65°C to +150°C
Thermal rise, case to junction (ΔT_J)	13.9°C
Lead soldering temperature (10 seconds)	+300°C
Power dissipation (T_C = +125°C)	Duty cycle dependent (see table I power supplies)

1.4 Recommended operating conditions.

Logic Supply voltage range (V_L)	+4.5 V dc to +5.5 V dc
Positive supply voltage range (V_{CC})	+14.25 V dc to +15.75 V dc
Negative supply voltage (V_{EE})	-14.25 V dc to -15.75 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Maximum differential input voltage	40 Vp-p

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1553 - Interface Standard for Digital Time Division Command/Response Multiplex Data Bus.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuits Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements shall be in accordance with MIL-PRF-38534.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Pin functions. Pin functions shall be as specified in table III.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤T_C ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver							
Differential input impedance	Z_{IN} diff	DC to 1 MHz	2/	All	4		kΩ
Differential input voltage	V_{IN} diff		2/	All		40	Vp-p
Input threshold	V_{TH}	Direct coupled, (across 35Ω load)	4,5,6	All		1.2	Vp-p
Common mode rejection ratio	CMRR	DC to 2 MHz	2/ 3/	All	40		dB
Common mode voltage	CMV	DC to 2 MHz	2/ 3/	All	-10	+10	V
Transmitter							
Differential output voltage	V_{OUT} diff	Direct coupled, (across 35Ω load)	4,5,6	All	6.0	9.0	Vp-p
Output rise and fall time	t_r, t_f		9,10,11	01	100	180	ns
				02,03	100	300	ns
Output noise	N_{OUT}		2/ 3/	All		14	mVp-p
Logic							
High level input voltage	V_{IH}	V_L = 5.5 V	1,2,3	All	2.4		V
Low level input voltage	V_{IL}	V_L = 5.5 V	1,2,3	All		0.7	V
High level input current 4/	I_{IH}	V_L = 5.5 V, V_{IH} = 2.7 V	1,2,3	All	-0.7	-0.03	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input current 5/	I_{IH}	V_L = 5.5 V, V_{IH} = 2.7 V	1,2,3	01,03	-20	+20	µA
				02	-300	+20	
Low level input current 4/	I_{IL}	V_L = 5.5 V, V_{IL} = 0.4 V	1,2,3	01,03	-1.6	-.09	mA
				02	-1.6	+.02	
Low level input current 5/	I_{IL}	V_{IL} = 0.4 V	1,2,3	01,03	-20	+20	µA
				02	-300	+20	
High level output voltage 6/	V_{OH}	V_L = 4.5 V, I_{OH} = 0.3 mA	1,2,3	All	2.7		V
High level output voltage 7/	V_{OH}	V_L = 4.5 V, I_{OH} = 3 mA	1,2,3	All	2.7		V
Low level output voltage 8/	V_{OL}	V_L = 4.5 V, I_{OL} = -1.6 mA	1,2,3	All		0.4	V
Low level output voltage 9/	V_{OL}	V_L = 4.5 V, I_{OL} = -4mA	1,2,3	All		0.4	V
Low level output voltage 7/	V_{OL}	V_L = 4.5 V, I_{OL} = -6 mA	1,2,3	All		0.4	V
Functional test 10/			7,8	All			pass/ fail
Input capacitance	C_I	f = 1 MHz	see 4.3.1c	All		50	pF
Input/output capacitance 7/	C_{IO}	f = 1 MHz	see 4.3.1c	All		50	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supplies							
+5 V dc current drain	I_L	V_L = +5.5 V dc, Inputs = 0 V dc, except 12 MHz clock input active, All outputs open	1,2,3	All		160	mA
-15 V dc current drain	I_{EE}	V_{EE} = -15.75 V dc	1,2,3	All		60	mA
+15 V dc current drain	I_{CC}	V_{CC} = +15.75 V dc					
- idle			1,2,3	All		80	mA
- 25% transmit			1,2,3	All		130	mA
- 50% transmit			1,2,3	All		180	mA
-100% transmit			1,2,3	All		280	mA

1/ V_{CC} = +15 V, V_{EE} = -15 V, V_L = + 5 V unless otherwise specified.

2/ This parameter is not tested, but is guaranteed by design.

3/ Receiver and transmitter parameters are specified with transformer.

4/ I_{IH} and I_{IL} for input pins BRO ENA, ADDRE, ADDRC, ADDRA, ADDRD, ADDRB, and ADDRP.

5/ I_{IH} and I_{IL} for all input pins other than in note 4.

6/ V_{OH} for all output pins other than in note 7.

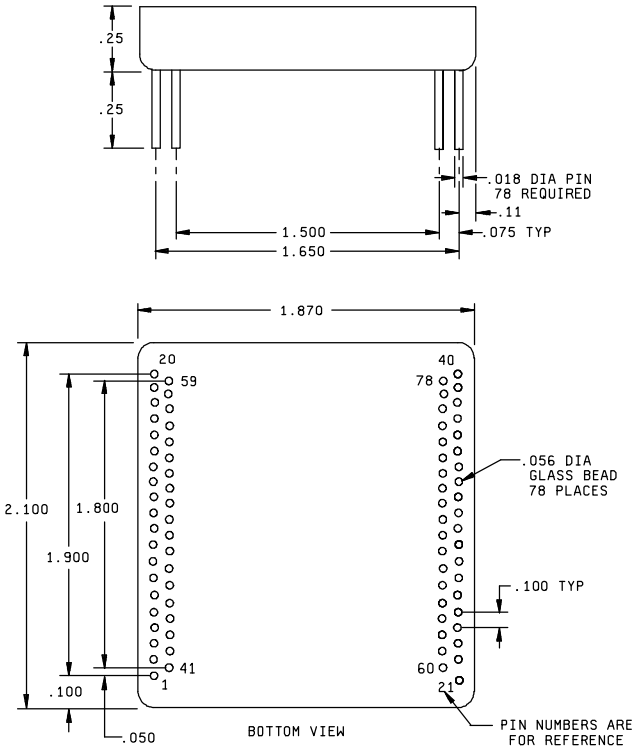
7/ V_{OL}, V_{OH}, and C_{IO} for pins DB0 through DB15.

8/ V_{OL} for output pins A10, A8, A6, $\overline{\text{HSFAIL}}$, A5, $\overline{\text{RTFAIL}}$, A11, $\overline{\text{BITEN}}$, $\overline{\text{NBGT}}$, A9, A7, $\overline{\text{GBR}}$, $\overline{\text{ME}}$, $\overline{\text{STATEN}}$.

9/ V_{OL} for output pins $\overline{\text{RTADERR}}$, A3, A1, INCMD, $\overline{\text{DTSTR}}$, $\overline{\text{DTREQ}}$, A2, A0, $\overline{\text{DTACK}}$, A4, R/$\overline{\text{W}}$.

10/ Functional tests are performed to verify functionality to MIL-STD-1553 RTU protocol.

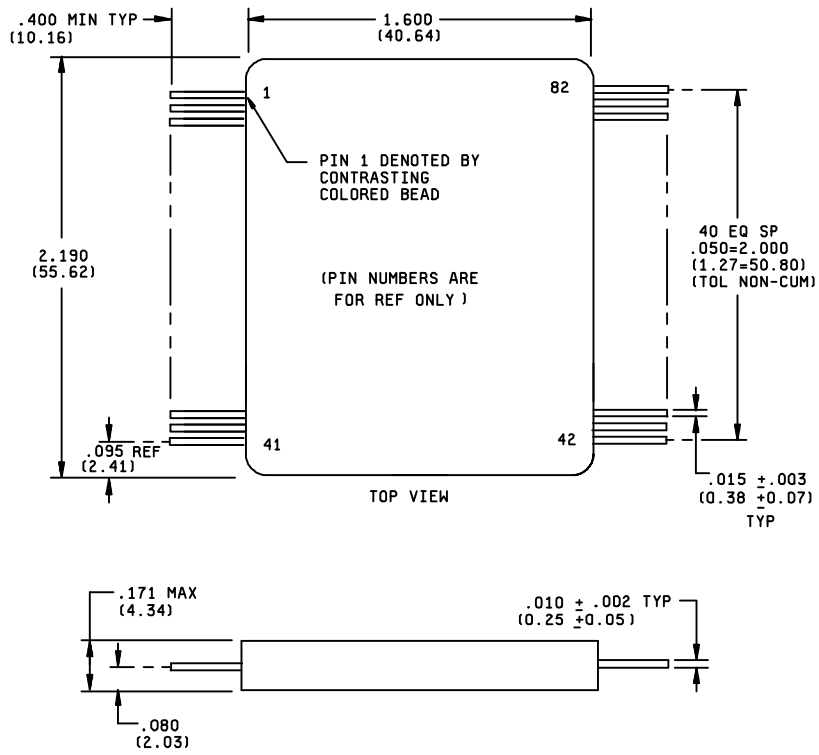
Case X



Inches	mm
.018	0.45
.050	1.27
.056	1.42
.075	1.91
.100	2.54
.11	2.8
.25	6.4
1.500	38.10
1.650	41.91
1.800	45.72
1.870	47.50
1.900	48.26
2.100	53.34

FIGURE 1. Case outline(s).

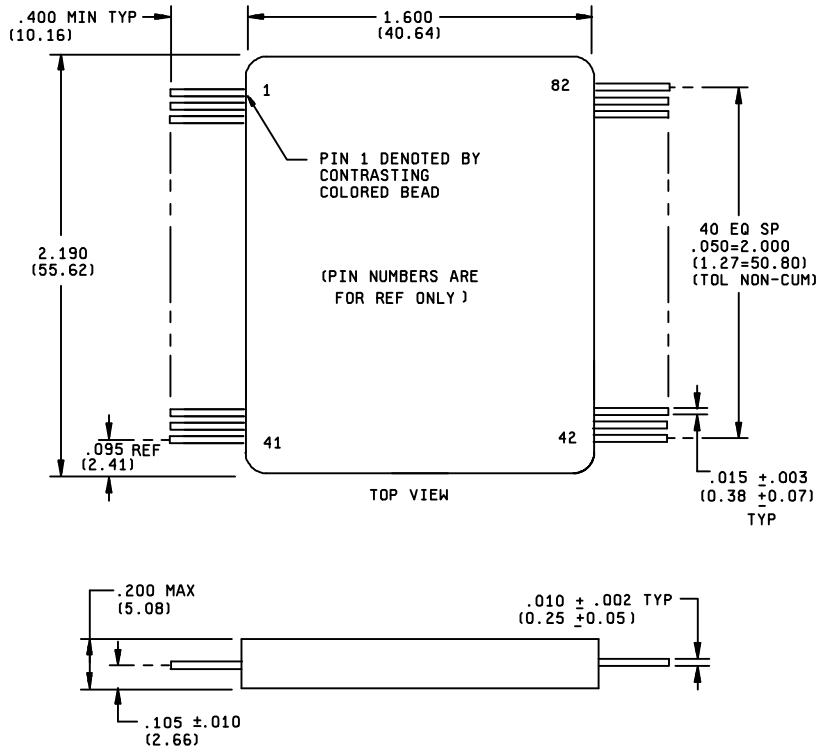
Case Y



Inches	mm
.002	0.05
.003	0.07
.010	0.25
.015	0.38
.050	1.27
.080	2.03
.095	2.41
.171	4.34
.400	10.16
1.600	40.64
2.000	50.80
2.190	55.62

FIGURE 1. Case outline(s) - Continued.

Case Z



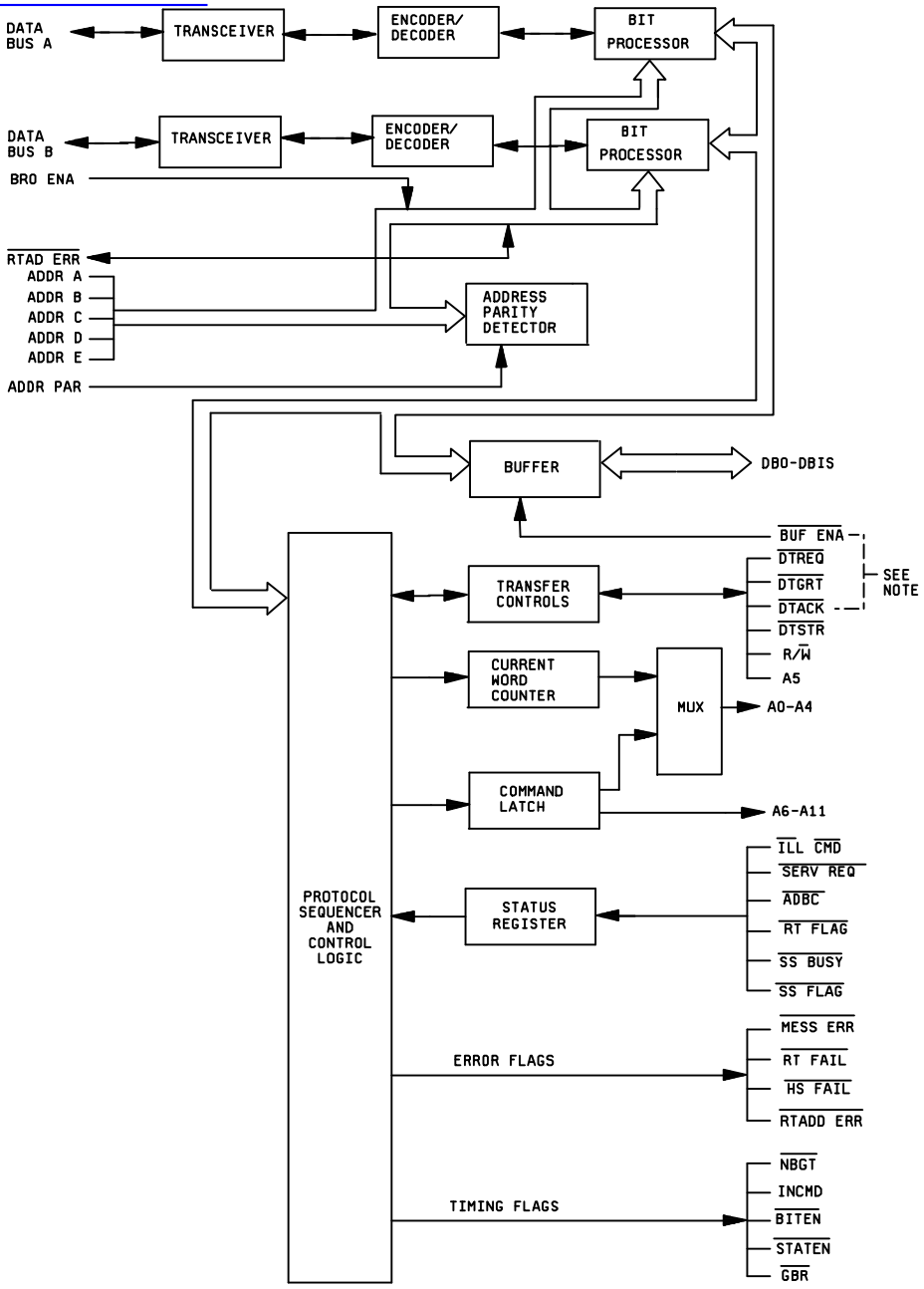
Inches	mm
.002	0.05
.003	0.07
.010	0.25
.015	0.38
.050	1.27
.095	2.41
.105	2.66
.200	5.08
.400	10.16
1.600	40.64
2.190	55.62

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three decimals and ±.100 (0.25 mm) for two place decimals.
4. Case Z is a conductive package.

FIGURE 1. Case outline(s) - Continued.

Device types	01, 02, and 03				
Case outlines	X	Y and Z	Case outlines	X	Y and Z
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	A10	NC	43	DB0	NBGT
2	A8	A10	44	DB2	STATEN
3	A6	A9	45	DB4	TXDATAOUT A
4	DB1	A8	46	DB6	TXDATAOUT A
5	DB3	A7	47	DB8	V_{EE} A
6	DB5	A6	48	DB10	V_{CC} A
7	DB7	DB0	49	DB12	V_L A
8	DB9	DB1	50	DB14	GNDA
9	DB11	DB2	51	V_L	RXDATAIN A
10	DB13	DB3	52	GND	RXDATA A
11	DB15	DB4	53	ADDRD	BITEN
12	BRO ENA	DB5	54	ADDRB	ME
13	ADDRE	DB6	55	ADDRP	SRQ
14	ADDRC	DB7	56	TXDATAOUT B	SSFLAG
15	ADDRA	DB8	57	V_{EE} B	ILLCMD
16	RTADERR	DB9	58	V_L B	BUSY
17	TXDATAOUT B	DB10			
18	V_{CC} B	DB11	59	RXDATAIN B	A11
19	GND B	DB12	60	A2	TEST 1
20	RXDATA	DB13	61	A0	TEST 2
21	A3	DB14	62	DTACK	RTFLAG
22	A1	DB15	63	A4	ADBC
23	DTGRT	V_L	64	R/W	RESET
24	INCMD	BRO ENA	65	GBR	DTREQ
25	HSFAIL	GND	66	12 MHz IN	BUF ENA
26	DTSTR	ADDRE	67	BUF ENA	RTFAIL
27	A5	ADDRD	68	RESET	12 MHz IN
28	RTFAIL	ADDRC	69	RTFLAG	A5
29	DTREQ	ADDRB	70	TEST 1	GBR
30	ADBC	ADDRA	71	BUSY	DTSTR
31	TEST 2	ADDRP	72	SSFLAG	R/W
32	A11	RTADERR	73	ME	HSFAIL
33	ILLCMD	TXDATAOUT B	74	RXDATAIN A	A4
34	SRQ	TXDATAOUT B	75	GNDA	INCMD
35	BITEN	V_{EE} B	76	V_{CC} A	DTACK
36	RXDATAIN A	V_{CC} B			
37	V_L A	V_L B	77	TXDATAOUT A	DTRGT
38	V_{EE} A	GND B	78	STATEN	A0
			79	- - -	A1
39	TXDATAOUT A	RXDATAIN B	80	- - -	A2
40	NBGT	RXDATAIN B	81	- - -	A3
41	A9	NC	82	- - -	NC
42	A7	NC			

FIGURE 2. Terminal connections.



NOTE: For most user applications, $\overline{\text{DTACK}}$ can be connected directly to $\overline{\text{BUF ENA}}$.

FIGURE 3. Block diagram.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 4, 7, 9
Final electrical parameters	1*, 2 ,3 ,4 ,5 ,6 ,9, 10, 11
Group A test requirements	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 shall be omitted.

c. Subgroup 4 (C_I and C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect input and output capacitance.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

TABLE III. Pin functions.

Function	Description
A10	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
A8	Latched output of the third most significant bit in the subaddress field of the command word.
A6	Latched output of the least significant bit (LSB) in the subgroups field of the command word.
DB1	Bi-directional parallel data bus bit 1.
DB3	Bi-directional parallel data bus bit 3.
DB5	Bi-directional parallel data bus bit 5.
DB7	Bi-directional parallel data bus bit 7.
DB9	Bi-directional parallel data bus bit 9.
DB11	Bi-directional parallel data bus bit 11.
DB13	Bi-directional parallel data bus bit 13.
DB15	Bi-directional parallel data bus bit 15 (MSB).
BRO ENA	Broadcast enable - When HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW , it prevents response to address 31 unless it was the assigned terminal address.
ADDRE	Input of the MSB of the assigned terminal address.
ADDRC	Input of the 3rd MSB of the assigned terminal address.
ADDRA	Input of the LSB of the assigned terminal address.
$\overline{\text{RTADERR}}$	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
$\overline{\text{TXDATAOUT}}$ B	LOW output to the primary side of the coupling transformer that connects to the channel B of the 1553 bus.
V_{CC} B	+15 volt input power supply connection for the B channel transceiver.
GND B	Power supply return connection for the B channel transceiver.
RXDATA	Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 bus.

TABLE III. Pin functions - Continued.

Function	Description
A3	Multiplexed address line output. When INCMD is LOW, or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.
A1	Multiplexed address line output. When INCMD is LOW, or A6 through A10 are all zeroes or all ones (mode command) , it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.
$\overline{\text{DTGRT}}$	Data transfer grant - Active LOW input signal from the subsystem that informs the RT, when DTREQ is asserted, to start transfer. Once the transfer is started, DTGRT can be removed.
INCMD	In command - HIGH level output signal used to inform the subsystem that the RT is presently servicing a command. When low, A0-A4 represent the word count of the present command. When high, A0-A4 represent the current word counter of non-mode commands.
$\overline{\text{HSFAIL}}$	Handshake fail - Output signal that goes LOW and stays LOW whenever the subsystem fails to supply DTGRT in time to do a successful transfer. Cleared by the next NBGT.
$\overline{\text{DTSTR}}$	DATA strobe - A LOW level output pulse (166 ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommend using the rising edge to clock data in.
A5	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred.
$\overline{\text{RTFAIL}}$	Remote terminal failure - latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Cleared by the start of the next message transmission (status word) and set if problem is again detected.
$\overline{\text{DTREQ}}$	Data transfer request - Active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay low until transfer timeout has occurred.
$\overline{\text{ADBC}}$	Accept dynamic bus control - Active LOW input signal from subsystem used to set the dynamic bus control acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
TEST 2	Factory test point - DO NOT USE.

TABLE III. Pin functions - Continued.

Function	Description
A11	Latched output of the T/$\overline{R}$ bit in the command word.
$\overline{\text{ILLCMD}}$	Illegal command - Active LOW input signal from the subsystem, strobes in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
$\overline{\text{SRQ}}$	Subsystem service request - Input from the subsystem used to control the service request bit in the status register. If LOW when the status word is updated, the service request bit will be set; if HIGH, it will be cleared.
$\overline{\text{BITEN}}$	Built-in-test word enable - LOW level output pulse (.5 µs), present when the built-in-test word is enabled on the parallel data bus.
$\overline{\text{RXDATAIN A}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
V_L A	+5 volt input power supply connection for the A channel transceiver.
V_{EE} A	-15 volt input power supply connection for the A channel transceiver.
$\overline{\text{TXDATAOUT A}}$	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
$\overline{\text{NBGT}}$	New bus grant - LOW level output pulse (166 ns) used to indicate the start of a new protocol sequence in response to the command word just received.
A9	Latched output of the 2nd MSB in the subaddress field of the command word.
A7	Latched output of the 2nd LSB in the subaddress field of the command word.
DB0	Bi-directional parallel data bus bit 0 (LSB).
DB2	Bi-directional parallel data bus bit 2.
DB4	Bi-directional parallel data bus bit 4.
DB6	Bi-directional parallel data bus bit 6.
DB8	Bi-directional parallel data bus bit 8.
DB10	Bi-directional parallel data bus bit 10.
DB12	Bi-directional parallel data bus bit 12.
DB14	Bi-directional parallel data bus bit 14.

TABLE III. Pin functions - Continued.

Function	Description
V_L	+5 volt input power supply connection for RTU digital logic section.
GND	Power supply return RTU digital logic connection.
ADDRD	Input of the 2nd MSB of the assigned terminal address.
ADDRB	Input of the 2nd LSB of the assigned terminal address.
ADDRP	Input of address parity bit. The combination of assigned terminal address and ADDRP must be odd parity for the RT to work.
TXDATAOUT B	HIGH, output to the primary side of the coupling transformer that connects to the B channel of the 1553 bus.
V_{EE} B	-15 volt input power supply connection for the B channel transceiver.
V_L B	+5 volt input power supply connection for the B channel transceiver.
$\overline{\text{RXDATAIN B}}$	Input from the LOW side of primary side of the coupling transformer that connects to the B channel of the 1553 bus.
A2	Multiplexed address line output. When INCMD is LOW, or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter.
A0	Multiplexed address line output. When INCMD is LOW, or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the MSB in the word count field of the command. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the LSB of the current word counter.
$\overline{\text{DTACK}}$	Data transfer acknowledge - Active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the DTGRT in response to DTREQ and is presently doing the transfer. Can be connected directly to (BUF ENA) for control of 3-state data buffers; and to 3-state address buffer control lines, if they are used.
A4	Multiplexed address line output. When INCMD is LOW or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the MSB of the current word counter.
R/$\overline{\text{W}}$	Read/$\overline{\text{Write}}$ - Output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input. The signal is HIGH only when DTREQ is active (LOW).

TABLE III. Pin functions - Continued.

Function	Description
$\overline{\text{GBR}}$	Good block received - LOW level output pulse (.5 µs) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.
12 MHz IN	12 MHz clock input - Input for the master clock used to run RTU circuits.
$\overline{\text{BUF ENA}}$	Buffer enable - Input used to enable or 3-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to DTACK if RT is sharing the same data bus as the subsystem.
$\overline{\text{RESET}}$	Input resets entire RT when low.
$\overline{\text{RTFLAG}}$	Remote terminal flag - Input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set:; if HIGH, it would be cleared. Normally connected to RTFAIL.
TEST 1	Factory test point - DO NOT USE.
$\overline{\text{BUSY}}$	Subsystem busy - Input from the from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands data will still be transferred to subsystem. For (device type 01 only) on recieve commands data will be requested from the subsystem in response to transmit command.
$\overline{\text{SSFLAG}}$	Subsystem flag, Input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH, it will be cleared.
$\overline{\text{ME}}$	Message error - Output signal that goes LOW and stays low whenever there is a format or word error with the received message over the 1553 data bus. Cleared by the next NBGT.
RXDATAIN A	Input from the HIGH side of the primary side of the coupling transformer that contacts to the A channel of the 1553 bus.
GNDA	Power supply return connection for the A channel transceiver.
V_{CC} A	+15 volt input power supply connection for the A channel transceiver.
$\overline{\text{TXDATAOUT A}}$	LOW output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
$\overline{\text{STATEN}}$	Status word enable - Low level active output signal present when the status word is enabled on the parallel data bus.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-01-31

Approved sources of supply for SMD 5962-87535 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8753501XA	19645	BUS-65112
5962-8753501XC	19645	BUS-65112
5962-8753501YA	19645	BUS-65117
5962-8753501YC	19645	BUS-65117
5962-8753502XA	88379	ARX2542-001-2
5962-8753502XC	88379	ARX2542-001-1
5962-8753502XX 3/	88379	ARX2542-001-3
5962-8753502YA	88379	ARX2542-202-2
5962-8753502YC	88379	ARX2542-202-1
5962-8753502YX 3/	88379	ARX2452-202-3
5962-8753503XA	88379	CT-2512-001-2
5962-8753503XC	88379	CT-2512-001-1
5962-8753503XX 3/	88379	CT-2512-001-3
5962-8753503ZA	88379	CT-2512-201-2
5962-8753503ZC	88379	CT-2512-201-1
5962-8753503ZX 3/	88379	CT-2512-201-3

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ This device is available with lead finishes A or C.

Vendor CAGE number	Vendor name and address
50821	ILC Data Device Corporation 105 Wilbur Place Bohemia, NY 11716
88379	Aeroflex Circuit Technology 35 South Service Road Plainview NY, 11803