

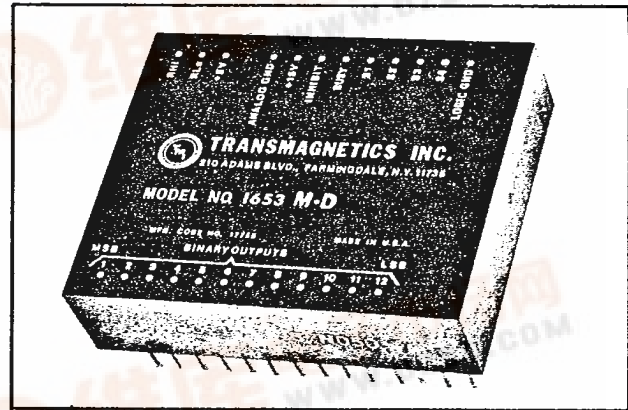
**MODEL
1653**

Revised September 1987

UNIVERSAL 12 BIT AUTO RANGING TRACKING SYNCHRO/RESOLVER-TO-DIGITAL CONVERTER

FEATURES:

- Resolution: 12 Bits
- Accuracy: 6 arc minutes
- Reference voltage: 5 - 125 Vrms
- Reference frequency: 44 to 1000 Hz
- Input Voltage: 8-100 Vrms
- No - 15VDC required
- No 180° Hang-up
- Reference and signal inputs are transformer isolated
- Available for 0°C to +80°C or -55°C to +105°C
- Hermetically sealed units on request
- Meets MIL-STD-202D: 101C, 105B, 106C, 107C, 202D, 204B and 205D
- High reliability 883B, or MIL-M-38510 units on request
- No special precautions are required against static electricity



DESCRIPTION:

This unique device automatically senses and compensates for wide variations of reference voltage, reference frequency, and input voltage with no loss of tracking accuracy or resolution even though the reference voltage and line-to-line voltages vary independently of each other. This innovation has eliminated the need for different converter modules thus simplifying designs and spares requirements. These converters are pin compatible with existing units in the field so that no wiring changes or additional components are required. In addition, the need for a -15 VDC supply has been eliminated. Our unusually sophisticated solid state tracking converter, continuously transforms synchro or resolver data into digital form that is error free at tracking rates up to 80 rpm. Type 2 servo loop error processing techniques insure that data is always fresh and continuously available except during "Converter Busy". The high resolution and accuracy, over the temperature range of -55°C to +105°C, offered by our modules qualifies them for industrial, commercial, military and avionics applications.

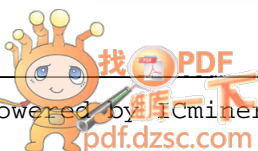
SPECIFICATIONS:

Resolution:	12 Bits
Accuracy**:	6 ± ½ LSB arc minutes
Speed:	80 RPM max.
Reference Voltage*:	5 - 125 Vrms
Reference Frequency:	44-1000 Hz
Input Voltage*:	8-100 Vrms
Fan Out:	10 TTL
Logic:	Parallel, positive logic, TTL levels, binary coded angle
Input Impedance:	50K min.
Operating Temperature:	"C": 0°C to +75°C; "M" -55°C to +105°C
Storage Temperature:	-55°C to +125°C
Potting:	All units are potted
Power Requirements:	+5 VDC 5% at 60mA +15 VDC 5% at 25mA
Weight:	13 oz potted

**Accuracy applies over the operating temperature range, ±5% power supply variations and 10% harmonic distortion.

*Reference voltage and L-L input voltage may vary independently of each other.

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Isolation: Transformer inputs are isolated from each other and from DC power common. Insulation resistance from any AC input to output is greater than 200 megohms at 200 VDC. Not applicable on solid state input unit.

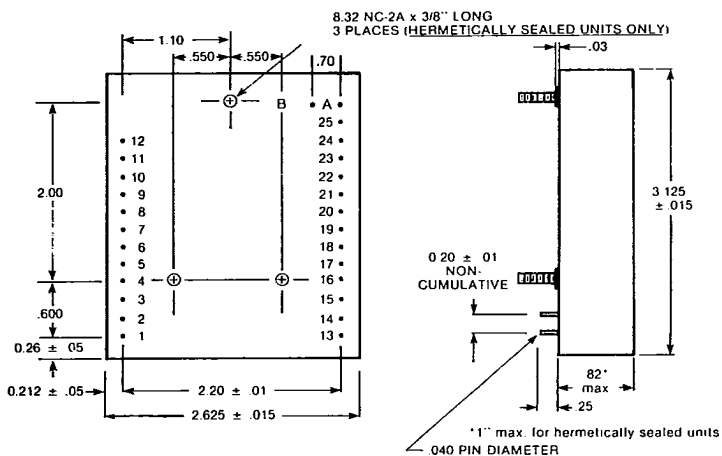
[查询"1653RC"供应商](#)

Grounds: Logic and analog grounds are common internally. A separate logic ground is available. See Part Number Designation. (Analog ground is +15 VDC return; Logic ground is +5 VDC return).

Converter Busy: The output is updated in 1 LSB steps whenever the input angle changes. Error free data can be transferred when "Converter Busy" is at logic "0". Logic "1" indicates that the output data is changing and that data is changing and that data should not be transferred.

Inhibit: Before transferring data, apply logic "0" to prevent output data from changing during transfer. The converter will ignore an "Inhibit" command during the "Converter Busy" period.

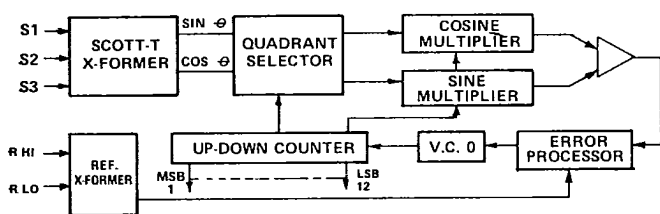
OUTLINE & CONNECTION



ALL DIMENSIONS IN INCHES

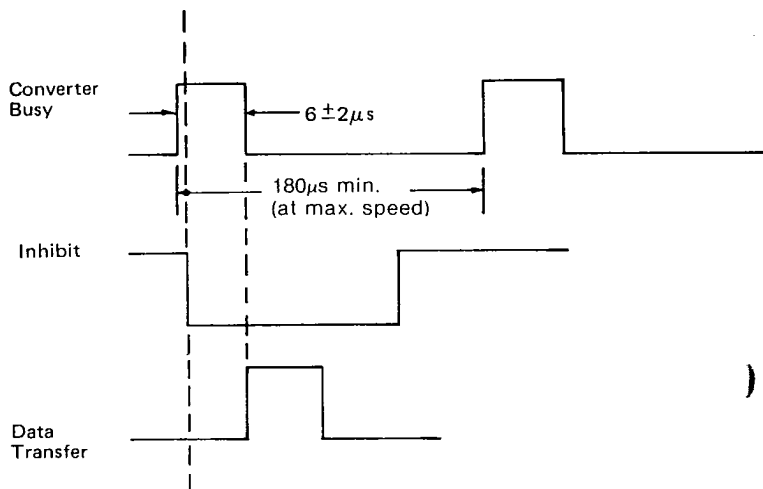
- | | |
|--------------|-------------------------------|
| 1 MSB (180°) | 13 R HI |
| 2 | 14 R LO |
| 3 | 15 +5 VDC |
| 4 | 16 N/A |
| 5 | 17 Analog GND |
| 6 | 18 +15 VDC |
| 7 BINARY | 19 Inhibit |
| 8 OUTPUTS | 20 Busy |
| 9 | 21 S1 |
| 10 | 22 S2 |
| 11 | 23 S3 |
| 12 LSB | 24 S4 (Resolvers only) |
| | 25 Logic GND (When specified) |

BLOCK DIAGRAM OF CONVERTER



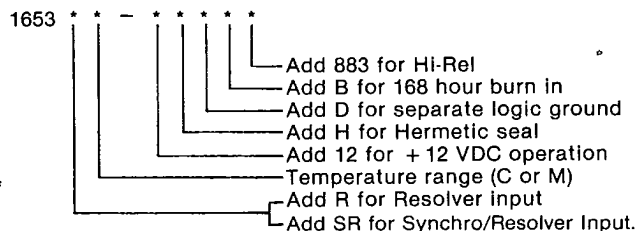
TIMING:

Timing at 80 RPM



NOTE: Data is immediately available when Converter Busy goes low.

PART NUMBER DESIGNATION:



For dual input units:
Synchro connections: S₁, S₂, S₃, connect A to B
Resolver connections: S₁, S₂, S₃, S₄, do not connect A to B



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