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1.2 <u>PIN</u> . The I	er (PIN). When a		e of Radiation Ha			d are reflected in the Part o are reflected in the PIN.
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Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designal	- Cas Cas outlir or (see 1.2	ne finish
\	V Drawing numbe	/ r	(000	(see 1.2.3	•	
arked with the a ecified RHA lev	appropriate RHA vels and are mar	designator. Devic ked with the appro	ce class M RHA opriate RHA des	marked device ignator. A das	es meet the MIL-PR sh (-) indicates a no	ecified RHA levels and are F-38535, appendix A n-RHA device.
1.2.2 <u>Device ty</u> Device		ice type(s) identify Generi	r the circuit funct	ion as follows	Circuit function	
01	<u> </u>		ACT163	•	· · · · · · · · · · · · · · · · · · ·	ounter, synchronous reset
1.2.3 <u>Device c</u> low. <u>Device</u>		The device class			entifying the produc	t assurance level as liste
М						STD-883 compliant, non-J RF-38535, appendix A
_	۲V	Cei	tification and qu	alification to M	IIL-PRF-38535	
Q oi					and as follows:	
	<u>line(s)</u> . The cas	e outline(s) are as	designated in N	11L-STD-1835	and as follows.	
		e outline(s) are as <u>criptive designator</u>	-	11L-STD-1835 ninals	Package style	
1.2.4 <u>Case out</u>	<u>letter Desc</u> E GE		<u>Terr</u> 2-T16 1 P3-F16 1		<u>Package style</u> Dual-in-line Flat pack	ess chip carrier
1.2.4 <u>Case out</u> <u>Outline</u> F 2 1.2.5 <u>Lead fini</u> e	letter Desc GE GE GE CC	criptive designator DIP1-T16 or CDIP DFP2-F16 or CDF QCC1-N20	<u>Ten</u> 2-T16 1 P3-F16 1	<u>ninals</u> 16 16 20	<u>Package style</u> Dual-in-line Flat pack Square leadle	
1.2.4 <u>Case out</u> <u>Outline</u> F 1.2.5 <u>Lead finis</u> A for dev <u>1</u> / Due to interr	letter Desc GE GE Sh. The lead fini- vice class M.	criptive designator DIP1-T16 or CDIP DFP2-F16 or CDF QCC1-N20 sh is as specified	<u>Tem</u> 2-T16 1 P3-F16 1 2 in MIL-PRF-385	<u>ninals</u> 16 20 35 for device o	<u>Package style</u> Dual-in-line Flat pack Square leadle classes Q and V or I	ess chip carrier MIL-PRF-38535, appendia at is characteristic of this
1.2.4 <u>Case out</u> <u>Outline</u> F 1.2.5 <u>Lead finis</u> A for dev <u>1</u> / Due to interr technology fam	letter Desc GE GE Sh. The lead fini- vice class M.	DIP1-T16 or CDIP DIP1-T16 or CDIP DFP2-F16 or CDF QCC1-N20 sh is as specified ns, device type 01	<u>Tem</u> 2-T16 1 P3-F16 1 2 in MIL-PRF-385	<u>ninals</u> 16 20 35 for device o	<u>Package style</u> Dual-in-line Flat pack Square leadle classes Q and V or I	MIL-PRF-38535, appendix

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Supply voltage range (Vcc) -0.5 V do to Vcc + 0.5 V dc 2/ DC input dode current (lw) (-0.5 V ≤ Vws 5Vcc + 0.5 V) ±20 mA DC output diode current (lw) (-0.5 V ≤ Vws 5Vcc + 0.5 V) ±20 mA DC output diode current (lw) (-0.5 V ≤ Vws 5Vcc + 0.5 V) ±20 mA DC output diode current (lw) (-0.5 V ≤ Vws 5Vcc + 0.5 V) ±20 mA DC output diode current (lcc), law) (ber pin) ±25 mA 3/ Maximum power dissipation (lcp) 500 mW Storage temporature range (Trm) ±25 vdc to +150 °C Lead temporature (soldening, 10 seconds) +175°C 4/ 14 Becommended operating conditions. 1/2/5/ Supply voltage range (Vcc) +4.5 V dc to +5.5 V dc Inform high level input voltage (Va) 0.0 V dc to Vcc Output voltage range (Vcc) +4.5 V dc to +5.5 V dc Imput voltage range (Vcc) +4.5 V dc to +5.5 V dc Minimum high level input voltage (Va) 0.0 V dc to Vcc Maximum low level input voltage (Va) 0.3 U dc g/ Minimum high level input voltage (Va) 125 mV/ins Maximum low level output current (lck) 42 mA 1.5 Digital logic testing for device classes Q and Y. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	Input voltage range -0.5 V do to Voc. + 0.5 V do 2/ Output voltage range -0.5 V do to Voc. + 0.5 V do 2/ DC input diode current (k) (-0.5 V S Vws SVcc.+ 0.5 V) ±20 mA DC output ourrent (ko)(-0.5 V S Vws SVcc.+ 0.5 V) ±20 mA DC output ourrent (ko)(-0.5 V S Vws SVcc.+ 0.5 V) ±20 mA DC output ourrent (ko)(-0.5 V S Vws SVcc.+ 0.5 V) ±20 mA DC voc or GND current (ko)(-0.5 V S Vws SVcc.+ 0.5 V) ±20 mA Storage temperature range (Trac) -65° C to +150°C Lead temperature (Ts) -45° C to +150°C Lead temperature (Ts) +175°C 4/ Supply voltage range (Voc) +4.5 V do to +5.5 V dc Input voltage range (Voc) +4.5 V do to Voc Output voltage range (Voc) -0.0 V do to Voc Output voltage range (Voc) -0.0 V do to Voc Output voltage range (Voc) -0.0 V do to Voc Maximum low level input voltage (Vu) 0.0 V do to Voc Maximum low level input voltage (Vu) 0.0 V do to Voc Maximum low level input voltage (Vol) -0.0 V do to Voc Maximum lingh level output current (los) -25 mN/ns Maximum lingh level output current (los) -	Supply voltage range (Voc)		051/ data - 701/	da
Output voltage range 0.5 V dc to Voc + 0.5 V dc 2/ DC input diode current (lox) (-0.5 V ≤ Vox ≤ Voc + 0.5 V) ±20 mA DC output diode current (lox) (-0.5 V ≤ Vox ≤ Voc + 0.5 V) ±20 mA DC output diode current (lox) (-0.5 V ≤ Vox ≤ Voc + 0.5 V) ±20 mA DC output diode current (lox) (-0.5 V ≤ Vox ≤ Voc + 0.5 V) ±20 mA DC output diode current (lox) (-0.5 V ≤ Vox ≤ Voc + 0.5 V) ±20 mA DC output diode current (lox) (-0.5 V ≤ Vox ≤ Voc + 0.5 V) ±20 mA DC output diode current (lox) (-0.5 V ≤ Vox ≤ Voc + 0.5 V) ±20 mA Maximum power dissipation (log) .450 mC Lead temperature (soldening, 10 seconds) .430 mV Stoppi voltage range (Vox) .45 V dc to +5.5 V dc Junction temperature (soldening, 10 seconds) .45 V dc to +5.5 V dc Input voltage range (Vox) .00 V dc to Voc Suppiv voltage range (Vox) .03 V dc dc Voc Maximum low level input voltage (Vin) .30 V dc dc Voc Maximum low level anawimm .30 V dc dc Voc Maximum low level output current (lox) .24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing .24 mA 1.5 Digital logic testing Michel performance and s	Output voltage range 0.5 V dc to Vcc + 0.5 V dc 2/ Dc input didde current ((k) (-0.5 V s/Wn s/Vcc + 0.5 V) ±20 mA Dc output didde current ((k) (-0.5 V s/Wn s/Vcc + 0.5 V) ±20 mA Dc output didde current ((k) (-0.5 V s/Wn s/Vcc + 0.5 V) ±20 mA Dc output didde current ((k) (-0.5 V s/Wn s/Vcc + 0.5 V) ±20 mA Dc output didde current ((k) (-0.5 V s/Wn s/Vcc + 0.5 V) ±20 mA Dc output didde current ((k) (-0.5 V s/Wn s/Vcc + 0.5 V) ±20 mA Maximum power dissipation (Pb) 500 mA Maximum power dissipation (Pb) 500 mA Supply voltage range (Vcc) +450 Vdc 10 Vcc Thermal resistance, junction-to-case (0,m) +100 Vdc to Vcc Supply voltage range (Vcc) +4.5 V dc to +5.5 V dc Unction temperature (s)(-0.004 cutage (Vn) 0.0 V dc to Vcc Maximum pin level input voltage (Vn) 0.0 V dc to Vcc Maximum pin level input voltage (Vn) 125 Vdc 20 Co Maximum lingh level output current (lex) 24 mA 15 Digital logic testing for device olassee 0 and V. Fault coverage measumement of manufacturing Iogic tests (MIL-STD-883, test method 5012) XX percent Z/ Viries otherwise noticd, iii voltages are referenced to CRID. For thom-in screening conditi				
DC input diode current (lw) (-0.5 V S V s V s V cc + 0.5 V) 120 mA DC cutput current (lco)(-0.5 V S V s V s V cc + 0.5 V) 120 mA DC cutput current (lco)(-0.5 V S V s V s V s V cc + 0.5 V) 120 mA DC cutput current (lco)(cor S V s V s V s V s V s V s V s V s V s V	DC input dice current (k) (-0.5 V ≤ Ver SVcc + 0.5 V) ±20 mA DC output ourrent (kc) (-0.5 V ≤ Ver SVcc + 0.5 V) ±20 mA DC output ourrent (kc) (-0.5 V ≤ Ver SVcc + 0.5 V) ±20 mA DC output ourrent (kc), (-0.5 V ≤ Ver SVcc + 0.5 V) ±20 mA DC vice of RN ourrent (kc), kew) (per pin) ±25 mA 3/ Maximum power dissipation (Po) 500 mW Storage temperature range (Tsra) ±65°C to ±150°C Lead temperature (Ts) ±175°C 4/ Supply voltage range (Vcc) ±175°C 4/ Supply voltage range (Vcc) ±1.5 V dc to ±5.5 V dc Input voltage range (Vcc) ±0.0 V dc to Vcc Output voltage range (Vcc) ±0.0 V dc to Vcc Maximum how level input voltage (VL) 0.0 V dc to Vcc Maximum low level input voltage (VL) 0.0 V dc to Vcc Maximum low level input voltage (VL) 0.0 V dc to Vcc Maximum low level input voltage (VL) ±25 mV/ns Maximum low level input current (Ex) ±24 mA<	Output voltage range		0.5 V 00 00 Vcc + 0.	.5 V 0C <u>2/</u>
DC output diode current (lox) (-0.5 V ≤ Vour ≤ Vcc + 0.5 V) ±50 mA DC output current (lox) (-0.5 V ≤ Vour ≤ Vcc + 0.5 V) ±50 mA DC vcc or GND current (lcc, leas) (per pin) ±50 mA Storage temperature range (Tsna) -65°C to +150°C Lead temperature (solidens, 10 seconds) +300°C Thermal resistance, junction-to-case (e.g.) See MIL-STD-1835 Junction temperature (solidens, 10 seconds) +4.5 V dc to +5.5 V dc hput voltage range (Vcc) +4.5 V dc to +5.5 V dc hput voltage range (Vac) -0.0 V dc to Vcc Output voltage range (Vac) -0.0 V dc to Vcc Minimum fing heve input voltage (Vin) .0.8 V dc Minimum fing heve input voltage (Vin) .0.8 V dc Maximum low level and wathin .0.2 V dc to Vcc Maximum ling heve input voltage (Vin) .25 mV/ns Maximum ling heve input voltage (Vin) .24 mA Maximum ling heve input current (lc.) .24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic testis (MIL-STD-383, test method 5012). XX percent Voltes acherosise node, all voltages an entereration to RND. .24 mA 1.5 Digital logic testis (MIL-STD-383, test method 5012). </td <td>DC cutput diode current (low) (-0.5 V ≤ Your ≤ Vcc + 0.5 V) +20 mA DC cutput current (low) (ere output pin) +250 mA DX cutront (low) (ere output pin) +250 mA DX cutront (low) (ere output pin) +250 mA Maximum power dissipation (Pc) -56°C to +150°C Lead temperature range (Tara) -65°C to +150°C Thermal resistance, junction-to-case (Quc) See MIL-STD-1835 Junction temperature (TJ) +1/2 5/ Supply voltage range (Voc) +4.5 V dc to +5.5 V dc Input voltage range (Voc) +4.5 V dc to +5.5 V dc Uptut voltage range (Voc) +4.6 V dc to Vcc Output voltage range (Voc) -40.0 V dc to Vcc Minimum high low linput voltage (Vn) 0.8 V dc Minimum high low linput voltage (Vn) 25°C to +125°C Input edge range (Voc) -44.5 V dc to 19.5 V dc Input voltage range (Voc) -44.5 V dc to 19.5 V dc Input voltage range (Va) -0.0 V dc fo/ Cc Cutput voltage range (Va) -0.0 V dc fo/ Cc Supply voltage rate (Av/A) maximum -25 mVns Maximum lingh low linput voltage (Vn) -25 mVns Maximum lingh low low output current (lox) +24 mA</td> <td>DC input diode current (l_{W}) (-0.5 V < V_{W} < V_{co} + 0.5 V)</td> <td></td> <td>U.3 V UC IO VCC + U</td> <td>.5 V UC <u>2</u>/</td>	DC cutput diode current (low) (-0.5 V ≤ Your ≤ Vcc + 0.5 V) +20 mA DC cutput current (low) (ere output pin) +250 mA DX cutront (low) (ere output pin) +250 mA DX cutront (low) (ere output pin) +250 mA Maximum power dissipation (Pc) -56°C to +150°C Lead temperature range (Tara) -65°C to +150°C Thermal resistance, junction-to-case (Quc) See MIL-STD-1835 Junction temperature (TJ) +1/2 5/ Supply voltage range (Voc) +4.5 V dc to +5.5 V dc Input voltage range (Voc) +4.5 V dc to +5.5 V dc Uptut voltage range (Voc) +4.6 V dc to Vcc Output voltage range (Voc) -40.0 V dc to Vcc Minimum high low linput voltage (Vn) 0.8 V dc Minimum high low linput voltage (Vn) 25°C to +125°C Input edge range (Voc) -44.5 V dc to 19.5 V dc Input voltage range (Voc) -44.5 V dc to 19.5 V dc Input voltage range (Va) -0.0 V dc fo/ Cc Cutput voltage range (Va) -0.0 V dc fo/ Cc Supply voltage rate (Av/A) maximum -25 mVns Maximum lingh low linput voltage (Vn) -25 mVns Maximum lingh low low output current (lox) +24 mA	DC input diode current (l_{W}) (-0.5 V < V_{W} < V_{co} + 0.5 V)		U.3 V UC IO VCC + U	.5 V UC <u>2</u> /
DC Utput current (lcor) (per output pin) ±50 mA DC Vico (SND current (lcor, law) (per pin) ±250 mA 3/ Maximum power dissipation (Po) 500 mW Storage temperature range (Trac) +65°C to ±15°°C Lead temperature (coldering, 10 seconds) +30°C Thermal resistance, luncinon-to-case (e.gc.) See MLL-STD-1835 Junction temperature (To) +175°C 4/ 14 Bacommanded operating conditions. 1/2/5/ Supply voltage range (Vw) +0.0 V dc to Vsc Output voltage range (Vw) 0.0 V dc to Vsc Output voltage range (Vw) 0.0 V dc to Vsc Maximum high level input voltage (Vw) 0.0 V dc to Vsc Maximum high level input voltage (Vw)	DC Cutput current (lon) (per output pin) #50 mA DC Vac or RND current (loc, low) (per pin) #250 mA Storage temperature range (Tan) #50 mA Storage temperature range (Tan) #50 mA Junction temperature (Ta) #50 mA Supply voltage range (Vac) #4.5 V dc to 45.5 V dc Plant voltage range (Var) 0.0 V dc to Vac Maximum low level piny voltage (Ta) 0.0 V dc to Vac Maximum low level piny voltage (Ta)				
DC Vco or GND current (loc, law) (per pin) ±250 mA 3/ Maximum power dissipation (Po) 500 mW Storage temperature range (Taro) +65°C to +15°C Lead temperature (addening, 10 seconds) +15°C d/ Thermal resistance, junction-to-case (Suc) See MIL-STD-1835 Junction temperature (Tu) +175°C d/ 1.4 Recommended operating conditions: 1/ 2/ 5/ Supply voltage range (Vxc) Supply voltage range (Vxc) +0.0 V dc to Vcc Output voltage range (Vxc) +0.0 V dc to Vcc Maximum low level input voltage (Vn) 0.8 V dc d/ Cutput voltage range (Vxc) -0.8 V dc d/ Maximum low level input voltage (Vn) 0.8 V dc d/ Cutput voltage range (Vxc) -0.8 V dc d/ Maximum low level output current (loc) -24 mA Maximum low level maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins. this value represents the maximum total current flowing	DC Vcc or GND current (tcc, laso) (per pin) ±250 mA §/ Maximum power dissipation (Pc) 500 mW Storage temperature range (Tsra) +50°C to +150°C Lead temperature (soldening, 10 seconds) +175°C 4/ Junction temperature (T) 500 mW Supply voltage range (Vcc) +175°C 4/ Supply voltage range (Vcc) +4.5 V dc to +5.5 V dc Input voltage range (Vcc) +0.0 V dc to Vcc Cuptur voltage range (Vcc) +0.0 V dc to Vcc Maximum for level number range (Tc) -0.0 V dc to Vcc Cuptur voltage range (Vcc) +0.0 V dc to Vcc Maximum low level number range (Tc) -0.0 V dc to Vcc Maximum low level number range (Tc) -0.0 V dc to Vcc Maximum low level number range (Tc) -0.0 V dc to Vcc Iftom voltage range (Vxl) -0.0 V dc to Vcc Maximum low level number range (Tc) -0.0 V dc to Vcc Iftom Vis level number range (Tc) -0.0 V dc to Vcc Into veloce number range (Vcl) -24 mA Maximum low level number current (tc) -24 mA Maximum low level number current (tc) -24 mA Is Digital logic testing for device classes Q and Y. Fault coverage measurement of manufac				
Maximum power dissipation (Po) 500 mW Storage temperature range (Tera) -65°C to +15°°C Lead temperature (Coldering, 10 seconds) +300°C Thermal resistance, junction-to-case (©uc) See MIL STD-1835 Junction temperature (Ta) +175°C 4/ 14 Becommanded operating conditions. 1/2/5/ Supply voltage range (Vac) +4.5 V dc to +5.5 V dc Output voltage range (Vac) +0.0 V dc to Vac Output voltage range (Vac) 0.8 V dc Minimum high level input voltage (Var) 0.8 V dc Minimum high level input voltage (Var) 0.8 V dc Minimum high level input voltage (Var) -55°C to +125°C Input degrate (a/A/3) maximum -55°C to +125°C Input degrate (a/A/3) maximum -24 mA 15 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing 24 mA 15 Digital logic tests (MIL-STD-883, test method 5012) XX percent Z/ 16 Digital logic tests (MIL-STD-883, test method 5012) XX percent Z/ 17 Portackages with method of of ML-STD-883. and A/D 18 Digital logic tests (MIL-STD-883, test method 5012) XX percent Z/	Maximum power dissipation (Po) 500 mW Storage temperature range (Tarso) -65°C to ±15°C Lead temperature (coldering, 10 seconds) +300°C Thermal resistance, junction-to-case (Suc) See MIL:STD-1835 Junction temperature (TJ) ±12'5' Supply voltage range (Vac) +45.5 V dc to ±5.5 V dc Input voltage range (Vac) +45.5 V dc to ±5.5 V dc Maximum high level input voltage (Vu) 0.0 V dc to Vacc Maximum high level input voltage (Vu) 30.0 V dc g/ Case operating temperature range (To) 55°C to ±155°C Input voltage range (Vac) 55°C to ±150°C Maximum high level input voltage (Vu) 28 mV/ns Maximum low level put voltage (To) 55°C to ±155°C Input voltage range (Vac) 28 mV/ns Maximum low level output current (br) 24 mA Maximum low level output current (br) 24 mA 15 Digital legic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent Values with multipk VC- and GND pins, this value regresents the maximum total current lowing into or out of all Vcc and GND pins, this value regresents the maximum total current lowing into or out of all Vcc and GND pins, this value	DC Vcc or GND current (loc love) (per pin)	••••••••••••••••••••••••••••••	+250 mA 2/	
Storage temperature range (Tsro) -65°C to +15°C Lead temperature (soldening, 10 seconds) +30°C Thermal resistance, junction-to-case (§uc) See MIL-STD-1835 Junction temperature (TJ) +175°C 4/ 14 Bacommended operating conditions: 1/2/5/ Supply voltage range (Vxc) +4.5 V dc to +5.5 V dc Induit voltage range (Vxc) +0.0 V dc to Vcc Output voltage range (Vxc) -0.0 V dc to Vcc Minimum hiph level input voltage (Vx) 0.0 V dc to Vcc Maximum tow level input voltage (Vxc) -0.8 V dc dc / Case operating temperature (art (TC)) -2.8 TV/ns Maximum tow level output current (loc) -2.4 mA Maximum tow level output current (loc) -2.4 mA Maximum tow level output current (loc) -2.4 mA 15 Digital logic testing for device classese O and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-683, test method 5012) XX percent 7/ Viries otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and QND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 500 of MIL-STD-8	Storage temperature range (Tars) -65°C to +150°C Lead temperature (addeting, 10 seconds) -30°°C Thermal resistance, junction-to-case (0,c) See MIL-STD-1835 Junction temperature (TJ) +175°C 4/ Supply voltage range (Vac) +4.5 V dc to +5.5 V dc Input voltage range (Vac) +4.5 V dc to +5.5 V dc Naminum Noi New Figure Voltage (Var) 0.8 V dc Maximum Noi New Figure (TG) -30.0 V dc to Vacc Maximum Noi New Figure (TG) -30.0 V dc to Vacc Maximum Noi New Figure (TG) -30.0 V dc to Vacc Maximum Noi New Figure (TG) -30.0 V dc to Vacc Maximum Noi New Figure (TG) -30.0 V dc to Vacc Maximum Noi New Figure (TG) -30.0 V dc to Vacc Maximum Noi New Figure (TG) -24 mA Max				
Lead temperature (solidering, 10 seconds) +300°C Thermal resistance, junction-to-case (Souc) See MIL-STD-1835 Junction temperature (T_i) +175°C 4/ 14 Recommended operating conditions: 1/2/5/ Supply voltage range (Vc) +14.5 V dc to +5.5 V dc Input voltage range (Vc) +0.0 V dc to Vcc 0.0 V dc to Vcc Maximum how level input voltage (Vn) 0.0 V dc to Vcc 0.8 V dc Maximum high level linput voltage (Vn) 0.9 V dc 0.9 V dc to Vcc Maximum high level output current (Ico) -24 mA -35°C to +125°C Maximum logi level output current (Ico) -24 mA Maximum logi level output current (Ico) -24 mA Maximum logi level output current (Ico) -24 mA Maximum level segreg measurement of manufacturing Icoic tests (MIL-STD-883, test method 5012) XX percent Z/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Vulses otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum incleaving conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above	Lead temperature (soldering, 10 seconds) +300°C Thermal resistance, junction-to-case (b ₁ c) See ML-STD-1835 Junction temperature (T ₁) +175°C 4/ Supply voltage range (Vac) +4.5 V dc to +5.5 V dc Input voltage range (Vac) +4.5 V dc to +5.5 V dc Output voltage range (Vac) +0.0 V dc to Vacc Output voltage range (Vac) 0.8 V dc Minimum hole level input voltage (Va) 0.0 V dc to Vacc Maximum hole level input voltage (Va) 0.0 V dc to Vacc Maximum hole level input voltage (Va) 0.0 V dc to Vacc Maximum hole level output current ((c)) -24 MA 15 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent Z/ Vinless otherwises noted, all voltage and referenced to GND. For packages with multiple Vac and GND pins, this value represents the maximum total current flowing into or out of all Vac ad GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. </th <th></th> <th></th> <th></th> <th></th>				
Thermal resistance, junction-to-case (Quc). See MIL-STD-1835 Junction temperature (T_i) +175°C g/ 1.4 Becommended operating conditions. 1/2/5/ Supply voltage range (Voc) +14.5 V dc to +5.5 V dc Input voltage range (Voc) +0.0 V dc to Voc Output voltage range (Voc) 0.0 V dc to Voc Maximum low level input voltage (Vu) 0.0 V dc to Voc Maximum low level input voltage (Vu) 0.0 V dc to Voc Maximum low level input voltage (Vu) 0.0 V dc to Voc Maximum low level input voltage (Vu) 0.0 V dc to Voc Maximum low level input voltage (Vu) 0.0 V dc to Voc Maximum low level output current (Col) 24 mA Maximum low level output current (Col) 24 mA 15 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent Z/ Vulses otherwise noted, all voltages are referenced to GND. For packages with multiple Voc and GND pins, this value represents the maximum total current flowing into or out of all Voc and GND pins. Maximum lovelise may degrade performance and affect reliability. Unless otherwise specified. the values listed above shall apply over the full Voc and Teresonmended operating range. For packages with multiple	Thermal resistance, junction-to-case (Guc)				
Junction temperature (T_i) +175°C 4/ 1.4 Bacommended operating conditions. 1/2/5/ Supply voltage range (Vac) +14.5 V dc to +5.5 V dc Input voltage range (Vac) +0.0 V dc to Vac 0.0 V dc to Vac Output voltage range (Vac) 0.0 V dc to Vac 0.0 V dc to Vac Maximum low level input voltage (Va) 0.0 V dc to Vac 0.0 V dc to Vac Maximum low level input voltage (Va) 0.0 V dc to Vac 0.0 V dc to Vac Maximum low level input voltage (Va) 0.0 V dc to Vac 0.0 V dc to Vac Maximum low level input voltage (Va) 0.0 V dc to Vac 0.0 V dc to Vac Maximum low level output current (loc) 24 mA 44.5 V mod Maximum low level output current (loc) 24 mA 1.5 Digital logic testing for device classes 0 and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent Z/ 7 Stressee above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Vulses otherwise noted, all voltages are referenced to GND. For packages with multiple Vac and GND pins, this value represents the maximum total current flowing into or out of all Vacc and GND pins. Navie Vac and GND pins. Maximum junction temperature shall not be exc	Junction temperature (T ₂)				
1.4 Becommended operating conditions. 1/2/5/ Supply voltage range (Vac) +1.5 V dc to +5.5 V dc Output voltage range (Vac) +0.0 V dc to Vac Output voltage range (Vac) +0.0 V dc to Vac Output voltage range (Vac) +0.0 V dc to Vac Maximum low level input voltage (Vac) 0.0 V dc to Vac Maximum high level input voltage (Vac) 0.0 V dc to Vac Immuno voltage range (Vac) 0.0 V dc to Vac Maximum high level output current (Icu) 25 mV/ns Maximum low level output current (Icu) -24 mA Maximum low level output current (Icu) -24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012). XX percent Z/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vac and GND pins, this value represents the maximum total current flowing into or out of all Vac and GND pins. Waximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of WIL-STD-883. Unless otherwise specified. the values listed above shall apply over the full Vac and To recommended operating range.	1.4 Bacommended operating conditions. 1/2/5/ Supply voltage range (Va) +4.5 V dc to 45.5 V dc Input voltage range (Va) +0.0 V dc to Vac Maximum how level input voltage (Vi,) 0.8 V dc Maximum how level input voltage (Vi,) 0.8 V dc Maximum how level input voltage (Vi,) 0.8 V dc Maximum how level input voltage (Vi,) 0.8 V dc Imput edge rate (Av/At) maximum 55°C to +125°C Input edge rate (Av/At) maximum 125 mV/ns Maximum high level output current ((a) -24 mA Maximum high level output current ((a) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent Z/ Vulness otherwise noted, all voltages are referenced to GND. For packages with multiple Vac and GND pins, this value represents the maximum total current flowing into or out of all Vac and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-843. Unless otherwise specified, the values listed above shall apply over the full Vac and Tc recommended operating range. For dynamic operation, a Vi, 1evel between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a Vi	$ $ unction temperature (T_i)	••••••	See MIL-STD-1835	1
Supply voltage range (Voc) +4.5 V dc to 4.5.5 V dc Input voltage range (Voc) +0.0 V dc to Vcc Output voltage range (Voc) +0.0 V dc to Vcc Maximum low level input voltage (Vil) .0.0 V dc to Vcc Maximum high level input voltage (Vil) .0.0 V dc to Vcc Immum high level input voltage (Vil) .0.0 V dc g/ Case operating temperature range (Co.) .55°C to +12°C Input edge rate (Av/A) maximum (forn Vil) (forn Vil) .0.0 V dc g/ Maximum high level output current (Ici) .24 mA Maximum low level output current (Ici) .24 mA 15 Digital logic testing for device classes 0 and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012). XX percent Z/ Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a Vil Vie Detwen 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a Vil evel betwen 2.0 and 3.	Supply voltage range (Vc) +4.5 V dc to +5.5 V dc Input voltage range (Var) +0.0 V dc to Vcc Output voltage range (Var) +0.0 V dc to Vcc Maximum low level input voltage (Var) 0.8 V dc Minimum high level input voltage (Var) 3.0 V dc f Case operating temperature range (TC) 55°C to +125°C Input edge rate (<i>Xv</i> /3) maximum 55°C to +125°C Input edge rate (<i>Xv</i> /3) maximum 125 mV/ns Maximum high level output current (lcs) -24 mA Maximum low level output current (lcs) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range.		•••••••••••••••••••••••••••••••••••••••	+1/5°C <u>4</u> /	
Input voltage range (Viw) +0.0 V do to Vcc Output voltage range (Vom) +0.0 V do to Vcc Maximum low level input voltage (Vi_) 0.8 V dc Case operating temperature range (TC) 3.0 V dc g/ Input edge rate (AvXI) maximum 55°C to +128°C input edge rate (AvXI) maximum 55°C to +128°C input edge rate (AvXI) maximum 125 mV/ns Maximum high level output current (Io+) -24 mA Maximum low level output current (Io+) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-983, test method 5012) XX percent Viness otherwise noted, all voltages are referenced to GND. 50°C to +120°C For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum incole networks onted, all voltages are referenced to all apply over the full Vcc and Tc recommended operating range. For dynamic operation, a Vi+ level between 2:0 and 3:0 V may be recognized by this device as a high logic level input. For static operation, a Vi+ level between 2:0 and 3:0 V may be recognized by this device as a high logic level input. For static operation, a Vi+ level between 2:0 and 3:0 V may be recognized by this device as a high logic level input. For static operation, a Vi+ level between 2:0 and 3:0 V may be recognized by this device as a high logic level input. For static operati	Input voltage range (Vw) -0.0 V do to Voc Output voltage range (Vw) 0.0 V do to Voc Maximum low level input voltage (Vn) 0.0 V do to Voc Minimum high level input voltage (Vn) 0.0 V do to Voc Stresses apperating temperature range (Tc) -3.0 V do g/ Input edge rate (AVA) maximum -55°C to +122°C Input edge rate (AVA) maximum -24 mA Maximum high level output current (Ion) -24 mA Maximum low level output current (Ion) -24 mA Is Digital logic testing for device classes 0 and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent Z/ Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Voc and GND pins, this value represents the maximum total current flowing into or out of all Voc and GND pins. Null voltage level input voltage level voltage level voltage and level volt	.4 Recommended operating conditions. 1/2/5/			
Output voltage (Vaur) +0.0 V dc to Vacc Maximum low level input voltage (Va) 0.8 V dc Gase operating temperature range (Tc) 0.8 V dc Input edge rate (a/A)d maximum -55°C to +125°C Input edge rate (a/A)d maximum 125 mV/ns Maximum ligh level output current (loc) -24 mA Maximum low level output current (loc) -24 mA Maximum low level output current (loc) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of ML-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a Vai level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system. Values will not affect their system. Values will be add	Output voltage (Var) 0.0 V dc to Vocc Maximum Now level input voltage (Vu.) 0.8 V dc Gase operating temperature range (TC) 0.5 V to C b + 125°C Input edge ing temperature range (TC) 55°C to + 125°C Input edge ing temperature range (TC) 55°C to + 125°C Maximum high level output current (Icor) 24 mA Maximum low level output current (Icor) 24 mA 1.5 Digital logic testing for device classes O and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-583, test method 5012) XX percent Z/ Vines collevels Maximum levels any degrade performance and affect reliability. XX percent Z/ Unless otherwise noted, all voltages are referenced to GMD. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V- level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a V- level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a V- level between 2.0 and 3.0 V may be recognized by this device as a				dc
Output voltage range (Vom) +0.0 V dc to Voc Maximum low level input voltage (Vin) 0.8 V dc Gase operating temperature range (Tc) 0.8 V dc (from Vin = 0.8 V to 2.0 V, 2.0 V to 0.8 V) 125 mV/ns Maximum ligh level output current (low) -24 mA Maximum low level output current (low) -24 mA Maximum low level output current (low) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7/ Vulees may degrade performance and affect reliability. Vulees otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 504 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a Vii 220 V will be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system. Values will be added when they become available from the qualified source. SIZE SiZE A Size Size Size Size	Output voltage (Var) -0.0 V dc to Vocc Maximum Now level input voltage (Var) 0.8 V dc Gase operating temperature range (TC) -55°C to +125°C Input deg rate (2x/3/b) maximum -55°C to +125°C Input deg rate (2x/3/b) maximum -24 mA Maximum high level output current (Iox) -24 mA Maximum low level output current (Iox) -24 mA 1.5 Digital logic testing for device classes O and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-583, test method 5012) XX percent Z/ Vine scale and all voltages are referenced to GMD. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Voc and GND pins. Maximum incrition temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise soled, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a Va level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a Va level between available from the qualified source. Values will not affect their system. Values will be added when they become available from the qualified source. StantDARD SIZE A 5962-91723 MicROCIRCUT DRAWING REVISION LEVEL SHEET 3 </td <td>Input voltage range (V_{IN})</td> <td></td> <td> +0.0 V dc to Vcc</td> <td></td>	Input voltage range (V _{IN})		+0.0 V dc to Vcc	
Maximum low level input voltage (ViL) 0.8 V dc Minimum high level input voltage (ViL) 3.0 V dc Gase operating temperature range (Tc) 55°C to +125°C Input edge rate (a//Δ) maximum 55°C to +125°C Iftom Wile = 0.8 V to 2 V, 2.0 V to 0.8 V) 125 mV/ns Maximum high level output current (loc) -24 mA Maximum low level output current (loc) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent Z/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance operation, a ViL eVel between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system. Values will be added when they become available from the qualified source. SiZE Sig2-91723 DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET	Maximum tow level input voltage (VL) 0.8 V dc Minimum high level input voltage (VL) 0.8 V dc Gase operating temperature range (Tc) -55°C to +125°C Input edge rate (Δ/Δ) maximum 125 mV/ns Maximum high level output current (Icit) -24 mA Maximum low level output current (Icit) -24 mA Maximum low level output current (Icit) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7/ Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum incition temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 504 of MIL-STD-883. Unless otherwise specific, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V ₁₄ Evel between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify the this will not affect their system. Values will be added when they become available from the qualified source. StanDARD SIZE A 5962-91722 MicROCIRCUT DRAWING REVISION LEVEL SHEET A	Output voltage range (Vout)		+0.0 V dc to Vcc	
Minimum high level input voltage (Vm) 3.0 V dc 6/ Case operating temperature range (C) -55°C to +125°C Input edge rate (Zw/A) maximum -25 mV/ns (from Vm = 0.8 V to 2.0 V, 2.0 V to 0.8 V) -24 mA Maximum ligh level output current (Ici) -24 mA Maximum low level output current (Ici) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent Z/ Vulees otherwise noted, all voltages are referenced to GND. XX percent Z/ For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of ML-STD-883. 40 V may be recognized by this device as a high logic level input. For static operation, a Vm Evel between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system. Values will be added when they become available from the qualified source. SIZE Sig2E Sig2E Sig2E-91723 DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET SHEET SHEET	Minimum high level input voltage (Viri) 3.0 V dc 6/ Case operating temperature range (Tc) -55°C to +125°C Input edge rate (ΔV/Δ) maximum (from Viri = 0.8 V to 2.0 V; 2.0 V to 0.8 V) 125 mV/ns Maximum high level output current (Ici) -24 mA Maximum low level output current (Ici) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012). XX percent Z/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burm-in screening conditions in accordance with method 5004 of ML-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a Viri level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a Viri level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify the this will not affect their system. Values will be added when they become available from the qualified	Maximum low level input voltage (VIL)		0.8 V dc	
Case operating temperature range (Tc)	Case operating temperature range (Tc)	Minimum high level input voltage (VIH)		3.0 V dc <u>6</u> /	
Input edge rate (Δv/Δt) maximum (from W _H = 0.8 V to 2.0 V, 2.0 V to 0.8 V)	Input edge rate (Δν/Δ!) maximum (from W = 0.8 V to 2.0 V, 2.0 V to 0.8 V)	Case operating temperature range (Tc)		55°C to +125°C	
Maximum high level output current (loc) -24 mA Maximum low level output current (loc) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify that this will no affect their system. Values will be added when they become available from the qualified source. SiZE	Maximum high level output current ((or)) -24 mA Maximum low level output current ((or)) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7 Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify the this will not affect their system. Values will be added when they become available from the qualified source. SIZE A S962-91723 SIZE A DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000 REVISION LEVEL A SHEET A	Input edge rate (∆v/∆t) maximum			
Maximum high level output current (loc) -24 mA Maximum low level output current (loc) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify that this will no affect their system. Values will be added when they become available from the qualified source. SiZE	Maximum high level output current ((or)) -24 mA Maximum low level output current ((or)) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7 Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify the this will not affect their system. Values will be added when they become available from the qualified source. SIZE A S962-91723 SIZE A DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000 REVISION LEVEL A SHEET A	(from $V_{IN} = 0.8$ V to 2.0 V, 2.0 V to 0.8 V)		125 mV/ns	
Maximum low level output current (loc) +24 mA 1.5 Digital logic testing for device classes Q and V. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. XX percent 7/ Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise as a high logic level input. For static operation, a Vi _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a Vi _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a Vi _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Values will be added when they become available from the qualified source. Size Sige2-91723 DEFENSE SUPPLY CENTER COLUMBUS COULDENT COLUMBUS REVISION LEVEL SHEET	Maximum low level output current (loc) +24 mA 1.5 Digital logic testing for device classes Q and Y. Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) XX percent 7/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. XX percent 7/ Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a V _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a V _H level between available from the qualified source. Values will be added when they become available from the qualified source. SIZE A S962-91722 S962-91722 A DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000 REVISION LEVEL A SHEET A SHEET A SHEET				
Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)				
Image: Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a VH = 2.0 V will be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system. Values will be added when they become available from the qualified source. Standard SIZE A 5962-91723 DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET	Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _H ≥ 2.0 V will be recognized by this device as a high logic level input. For static operation, a V _H ≥ 2.0 V will be recognized by this device as a high logic level input. For static operation, a V _H ≥ 2.0 V will be recognized by this device as a high logic level input. Users are cautioned to verify the this will not affect their system. Values will be added when they become available from the qualified source. STANDARD SIZE A 5962-9172: A SHEET A SHEET A SHEET	1.5 Digital logic testing for device classes Q and V.			
Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system. Values will be added when they become available from the qualified source. Standard SIZE A 5962-91723 DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET	Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple V _{CC} and GND pins, this value represents the maximum total current flowing into or out of all V _{CC} and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _H ≥ 2.0 V will be recognized by this device as a high logic level input. For static operation, a V _H ≥ 2.0 V will be recognized by this device as a high logic level input. For static operation, a V _H ≥ 2.0 V will be recognized by this device as a high logic level input. Users are cautioned to verify the this will not affect their system. Values will be added when they become available from the qualified source. STANDARD SIZE A 5962-9172: A SHEET A SHEET A SHEET	Fault coverage measurement of manufacturing			
Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple V _{CC} and GND pins, this value represents the maximum total current flowing into or out of all V _{CC} and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full V _{CC} and T _C recommended operating range. For dynamic operation, a V _H level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a V _H level between 2.0 and 3.0 V may be recognized by this device as a recautioned to verify that this will not affect their system. Values will be added when they become available from the qualified source. Standard Size A 5962-91723 DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET	Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. For packages with multiple Vcc and GND pins, this value represents the maximum total current flowing into or out of all Vcc and GND pins. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883. Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _H ≥ 2.0 V will be recognized by this device as a high logic level input. For static operation, a V _H ≥ 2.0 V will be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system. Values will be added when they become available from the qualified source. STANDARD SIZE A 5962-91723 DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET A 3	logic tests (MIL-STD-883, test method 5012)		XX percent 7/	
Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a V _{IH} ≥ 2.0 V will be the encognized by this device as a high logic level input. For static operation, a V _{IH} ≥ 2.0 V will be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system. Values will be added when they become available from the qualified source. STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS. OHIO 43216-5000	Unless otherwise specified, the values listed above shall apply over the full Vcc and Tc recommended operating range. For dynamic operation, a ViH level between 2.0 and 3.0 V may be recognized by this device as a high logic level input. For static operation, a ViH ≥ 2.0 V will be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system. Values will be added when they become available from the qualified source. STANDARD SIZE MICROCIRCUIT DRAWING A DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL A 3	maximum levels may degrade performance and affect reliability Unless otherwise noted, all voltages are referenced to GND. For packages with multiple V _{CC} and GND pins, this value repre- and GND pins. Maximum junction temperature shall not be exceeded except f	y. esents the maxir	num total current flowing	into or out of all V _{CC}
STANDARD A 5962-91723 MICROCIRCUIT DRAWING A 5962-91723 DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET	STANDARD MICROCIRCUIT DRAWINGA5962-91723DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000REVISION LEVEL ASHEET 3	Unless otherwise specified, the values listed above shall apply For dynamic operation, a V _{IH} level between 2.0 and 3.0 V may static operation, a V _{IH} \geq 2.0 V will be recognized by this device this will not affect their system.	be recognized l as a high logic	by this device as a high l	ogic level input. For
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS OHIO 42216-5000 REVISION LEVEL SHEET	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000REVISION LEVEL ASHEET 3		_		5962-91723
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是 APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883	-	Test Method Standard Microcircuits.
MIL-STD-973	-	Configuration Management.
MIL-STD-1835	-	Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's). MIL-HDBK-780 - Standard Microcircuit Drawings.

2.2 <u>Non-Government publications</u>. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-9172 3
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3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.4.5 State diagram. The state diagram shall be as specified on figure 4.

3.2.6 <u>Ground bounce waveforms and test circuit</u>. The ground bounce waveforms and test circuit shall be as specified on figure 5.

3.2.7 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 6.

3.2.8 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535.

3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 <u>Certificate of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change for device class M</u>. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

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3.9 <u>Verification and review for device class M</u>. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 <u>Microcircuit group assignment for device class M</u>. Device class M devices covered by this drawing shall be in microcircuit group number 40 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (2) $T_A = +125^{\circ}C$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-91723
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Test and MIL-STD-883 test method <u>1</u> /	Symbol	Test condition -55°C ≤ Tc ≤ +1 +4.5 V ≤ Vcc ≤ +	25°C	Device type and	Vcc	Group A subgroups	Limi	ts <u>3</u> /	Uni
		unless otherwise s	specified	Device class			Min	Max	
Positive input clamp voltage	Vic+	For input under test, in =		All _Q, V	0.0 V	1	0.4	1.5	V
3022	4/5/		M, D, L, R	All V	0.0 V	1	0.4	1.5	
Negative input clamp voltage	Vic.	For input under test, In =	-1.0 mA	All Q, V	Open	1	-0.4	-1.5	V
3022	4/5/		M, D, L, R	All V	Open	1	-0.4	-1.5	
High level output voltage	Vон	For all inputs affecting test, V _{IN} = 3.0 V or 0.		All All	4.5 V	1, 2, 3	4.4		V
3006	<u>4/5/6</u> /	For all other inputs, V _{IN} = V _{CC} or GND		All All	5.5 V		5.4		
		юн = -50 μА	M, D, L, R	All All	5.5 V	1	5.4		
		For all inputs affecting test, VIN = 3.0 V or 0.		All All	4.5 V	1, 2, 3	3.7		
		For all other inputs, $V_{IN} = V_{CC}$ or GND	M, D, L, R	All	4.5 V	1	3.7		1
		$l_{OH} = -24 \text{ mA}$	·	All	5.5 V	1, 2, 3	4.7		
		For all inputs affecting test, VIN = 3.0 V or 0.		All	5.5 V	1, 2, 3	3.85		1
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -50 \text{ mA} 7/$	M, D, L, R	All All	5.5 V	1	3.85		
Low level output VoL voltage	Vol	For all inputs affecting test, $V_{IN} = 3.0 \text{ V or } 0$		All	4.5 V	1, 2, 3		0.1	v
3007	<u>4/ 5/6</u> /	For all other inputs, $V_{IN} = V_{CC}$ or GND		All All	5.5 V	1		0.1	1
		$lo_L = 50 \ \mu A$	M, D, L, R	All All	5.5 V	1		0.1	1
		For all inputs affecting test, VIN = 3.0 V or 0		All M	4.5 V	1		0.4	1
		For all other inputs, $V_{IN} = V_{CC}$ or GND	M, D, L, R	All All	4.5 V	1		0.4	
		$I_{OL} = 24 \text{ mA}$	L <u>., ,,</u> ,	All M	4.5 V	2, 3		0.5	
				All M	5.5 V	1		0.4	
				 All	4.5 V	2, 3 1, 3	+	0.5	+
				Q, V	4.5 V	2		0.4	1
				All	5.5 V	1, 3		0.4	1
				Q, V	5.5 V	2	1	0.4	1
		For all inputs affecting test, VIN = 3.0 V or 0		All All	5.5 V	1, 2, 3	1	1.65	
		For all other inputs, $V_{IN} = V_{CC}$ or GND	M, D, L, R	All All	5.5 V	1		1.65	1
See footnotes at en	d of table.	$I_{OL} = 50 \text{ mA} \frac{7}{2}$	L			I	I	I	
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Test and MIL-STD-883 test method 1/	Symbol	Test conditions <u>2</u> -55°C ≤ T _C ≤ +125° +4.5 V ≤ V _{CC} ≤ +5.5	°C type	Vcc	Group A subgroups	Limi	ts <u>3</u> /	Un
		unless otherwise spec	1			Min	Мах	
nput capacitance 3012	Cin	See 4.4.1c T _C = +25°C	All All	GND	4		10.0	pF
Power dissipation capacitance	C _{PD} 8/	See 4.4.1c T _c = +25°C, f = 1 MHz	Ail	5.0 V	4		50]
Quiescent supply current delta,	Δlcc	For input under test, VIN = Vcc - 2.1 V	All Q, V	5.5 V	3		1.6	m/
TTL input levels 3005	<u>4/5/</u> 9/	For all other inputs, VIN = Vcc or GND			1,2		1.0	
••••	2		All M	5.5 V	1, 2, 3		1.6	
			, D All , R All	5.5 V	1		1.6 3.5	
Quiescent supply current outputs	Іссн	For all inputs,	<u>, n Ali</u> Ali Q, V	5.5 V	1	<u> </u>	2.0	مىر
high 3005	4/5/				2		40.0	1
			All M	5.5 V	1		8.0	1
					2, 3		160.0	
		· · · · · · · · · · · · · · · · · · ·	M All D All	5.5 V	1		100.0	 m/
		L	, R				3.5	1
Quiescent supply current outputs low	lcc∟ <u>4/5</u> /	For all inputs, V _{IN} = V _{CC} or GND	Ali Q, V	5.5 V	2		2.0	∆ىر
3005			All	5.5 V	1		8.0	
			М		2,3		160.0	
			M Ali	5.5 V	1		100.0	
			D All				1.0	m⁄
nput leakage current high	4H	For input under test,	, R All Q, V	5.5 V	1		<u>3.5</u> 0.1	μА
3010	<u>4/</u> 5/	For all other inputs, $V_{IN} = V_{CC}$ or GND			2		1.0	
			All M	5.5 V	1		0.1	1
					2, 3		1.0	
		M, D,	L, R All All	5.5 V	1		0.1	
ee footnotes at end	of table.		SIZE					
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Test and ML-STD-883 test method <u>1</u> /	Symbol	Test cond -55°C ≤ Tc +4.5 V ≤ Vc	≤+125°C	Device type and	Vcc	Group A subgroups	Limi	ts <u>3</u> /	Uni
		unless otherw	vise specified	Device class			Min	Max	
nput leakage current low	հւ	For input under V _{IN} = GND	test,	All Q, V	5.5 V	1		-0.1	مرر
3009	<u>4/5</u> /	For all other inp VIN = Vcc or GN				2		-1.0	
				All M	5.5 V	1		-0.1	
						2, 3		-1.0	
			M, D, L, R	All All	5.5 V	1		-0.1	1
Low level ground bounce noise	V _{GBL} 10/	$V_{LD} = 2.5 V$ $I_{OL} = +24 mA$ (See figure 5)	97 19 2.	All Q, V	4.5 V	4		1500	m
High level ground bounce noise	V _{GBH} <u>10</u> /	V _{LD} = 2.5 V Іон = -24 mA (See figure 5)		All Q, V	4.5 V	4		1500	m۱
Latch-up input/output over-voltage	lcc (O/V1)	t _w ≥ 100 µs, t _{coo} 5 µs ≤ t _r ≤ 5 ms 5 µs ≤ t _t ≤ 5 ms		All Q, V	5.5 V	2		200	m⁄
	11/	V _{test} = 6.0 V V _{CCQ} = 5.5 V V _{over} = 10.5 V							
Latch-up input/output	lcc	tw ≥ 100 µs, t _{coo} 5 عدر 5 s ≤ tr	ı ≥ tw	All Q, V	5.5 V	2		200	m/
positive over- current	(O/I1+)	5 µs ≤ t _f ≤5 ms V _{test} = 6.0 V V _{CCQ} = 5.5 V							
Latch-up	lcc	ار t _w ≥ 100 t _w s, t _{coo}		All	5.5 V	2		200	m
input/output negative over- current	(O/I1-)	5 μs ≤ tr ≤5 ms 5 μs ≤ tr ≤5 ms V _{test} = 6.0 V		Q, V				200	
	11/	Vccq = 5.5 V hrigger = -120 mA							
Latch-up supply over-voltage	lcc	t _w ≥ 100 µs, t _{coo} 5 عبر t _r ≤ 5 ms	l ≥ t _w	All Q, V	5.5 V	2		100	m
	(O/V2)	5 μs ≤ tr ≤5 ms V _{test} = 6.0 V V _{CCQ} = 5.5 V							
Functional tests	<u>4/5/</u>	V _{over} = 9.0 V V _{IL} = 0.4 V		All	4.5 V	7,8	L	н	-
3014	12/	V _{IH} = 3.0 V Verify output	M, D, L, R	All All	-	7	L	H	
		Vout		All	5.5 V	7, 8	L	н	-
See footnotes at en	d of table.]		M		L			
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Test and ML-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ Tc ≤ +125°C +4.5 V ≤ Vcc ≤ +5.5 V	Device type and	Vcc	Group A subgroups	Limi	ts <u>3</u> /	Ur	
test method <u>1</u> /		unless otherwise specified	Device class			Min	Max		
Propagation delay time, CP to Qn	tenl telh	$C_L = 50 \text{ pF minimum}$ $R_L = 500\Omega$	Ali M	4.5 V	9	1.0	9.5	n	
(count mode) 3003	<u>4/5/</u> <u>13</u> /	(See figure 6) M, D, L, R	All All		9	1.0	9.5		
			All M		10, 11	1.0	10.5		
			All Q, V		<u>9, 11</u> 10	1.0 1.0	9.5 10.5	-	
Propagation delay time, CP to Qn	tphL tpLH	C _L = 50 pF R _L = 500Ω	Ali M	4.5 V	9	1.0	9.0	n	
(load mode) 3003	<u>4/5/</u> <u>13</u> /	(See figure 6) M, D, L, R	All		9	1.0	9.0		
		L	All M		10, 11	1.0	10.0	1	
			All		9, 11	1.0	9.0]	
Propagation delay	•	C _L = 50 pF minimum	Q, V All	4.5 V	<u> </u>	1.0 1.0	10.0		
time, CP to TC	tPHL tPLH	R _L = 500Ω	All M All	4.5 V	99	1.0	12.0	n:	
(CET = H) 3003	<u>4/5/</u> <u>13</u> /	(See figure 6) M, D, L, R			9 10, 11	1.0	12.0		
			M All			1.0	13.0		
			Q, V		<u>9, 11</u> 10	1.0	13.0	1	
Propagation delay time, CET to TC	tphL tplH	$C_L = 50 \text{ pF minimum}$ $R_L = 500\Omega$	All M	4.5 V	9	1.0	9.0	n	
3003	<u>4/5/</u> <u>13</u> /	(See figure 6) M, D, L, R	All All		9	1.0	9.0		
			All M		10, 11	1.0	9.5		
			Ali		9, 11	1.0	9.0	-	
Maximum clock	fmax	$C_L = 50 \text{ pF minimum}$ $R_L = 500\Omega$	Q, V All	4.5 V	<u>10</u> 9	1.0 95.0	9.5	MH	
frequency 3003	<u>14</u> /	(See figure 6)	M		10, 11	85.0			
			Ail		9, 11	95.0			
			Q, V		10	85.0			
Input setup time, high or low	ts <u>14</u> /	$C_L = 50 \text{ pF minimum}$ $R_L = 500 \Omega$	Ali M	4.5 V	9	8.5		n	
PE to CP		(See figure 6)			10, 11	11.5			
			All Q, V		<u>9, 11</u> 10	8.5 11.5			
ee footnotes at end	STAND		SIZE						
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Test and ML-STD-883	Symbol	Test conditions <u>2</u> / -55°C ≤ Tc ≤ +125°C	Device type	Vcc	Group A subgroups	Limi	ts <u>3</u> /	Unit
test method 1/	}	+4.5 V ≤ Vcc ≤ +5.5 V	and		9			
		unless otherwise specified	Device			Min	Max	1
nput setup time,	ts	$C_{L} = 50 \text{ pF minimum}$	class All	4.5 V	9	10.0		ns
high or low Pn to CP	<u>14</u> /	R∟ = 500Ω (See figure 6)	м		10, 11	13.5		-
			All		0.11	10.0	l	4
			Q, V		<u>9, 11</u> 10	10.0 13.5		{
nput setup time, high or low	ts <u>14</u> /	$C_L = 50 \text{ pF minimum}$ $R_L = 500\Omega$	All	4.5 V	9	10.0		ns
SR to CP	-	(See figure 6)			10, 11	13.5	1	
			All		9, 11	10.0]
nput setup time,	•		Q, V	4.5.1	10	13.5	ļ	
high or low CEP, CET to CP	ts <u>14</u> /	$C_L = 50 \text{ pF minimum}$ $R_L = 500\Omega$	All M	4.5 V	9	5.5		ns
CEF, CET IO CF		(See figure 6)	All		<u> </u>	7.0 5.5		-
			Q, V		10	7.0		-
nput hold time, high or low	t _h <u>14</u> /	$C_L = 50 \text{ pF} \text{ minimum}$ $R_L = 500\Omega$	All	4.5 V	9, 10, 11	0.0		ns
PE to CP Input hold time,	<u> </u>	(See figure 6)						1
high or low Pn to CP	t _n <u>14</u> /	$C_L = 50 \text{ pF minimum}$ $R_L = 500 \Omega$ (See figure 6)	All All	4.5 V	9, 10, 11	0.5		ns
Input hold time,	th	$C_L = 50 \text{ pF minimum}$	All	4.5 V	9, 10, 11	0.0		ns
high or low SR to CP	<u>14</u> /	R∟ = 500Ω (See figure 6)	Ali					
Input hold time,	th	$C_L = 50 \text{ pF} \text{ minimum}$	All	4.5 V	9	0.0		ns
high or low CEP, CET to CP	<u>14</u> /	R∟ = 500Ω (See figure 6)	M		10.11	0.5		4
			All	}	10, 11 9, 10	0.5		-
			Q, V		11	0.5	1	-
Clock pulse width, high and low	t _w <u>14</u> /	$C_L = 50 \text{ pF minimum}$ $R_L = 500\Omega$	All	4.5 V	9, 10, 11	5.0		ns
(count, load modes)		(See figure 6)						
herein. All inpu Each input/outp designated sha a. V _{IC} (pos) ta b. V _{IC} (neg) ta c. All I _{CC} and placed in t Additional detail	ts and out ut, as appi Il be high k ests, the G ests, the V Δlcc tests, he circuit s led informa	eferenced MIL-STD-883 (e.g. ΔI buts shall be tested, as applicab- licable, shall be tested at the spe- evel logic, low level logic, or ope ND terminal can be open. $T_C =$ c_C terminal shall be open. $T_C =$ the output terminal shall be ope such that all current flows throug ation on qualified devices (i.e. pin VQC) upon request.	le, to the test ecified tempe n, except as +25°C. n. When per h the meter.	s in table rature, foi follows: forming th	I herein. r the specified linese tests, the o	imits. Ou current m	utput term eter shal	ninals I be
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里的 3902-91723011012A [共型 的 Table I. <u>Electrical performance characteristics</u> - Continued.

- 3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at 4.5 V \leq V_{CC} \leq 5.5 V.
- 4/ RHA samples do not have to be tested at -55°C and +125°C prior to irradiation.
- 5/ When performing postirradiation electrical measurements for RHA level, $T_A = +25^{\circ}C$. Limits shown are guaranteed at $T_A = +25^{\circ}C \pm 5^{\circ}C$.
- 6/ For dynamic operation, a V_{IH} level between 2.0 V and 3.0 V may be recognized by this device as a high logic level input. For static operation, a V_{IH} ≥ 2.0 V will be recognized by this device as a high logic level input. Users are cautioned to verify that this will not affect their system.
- <u>7</u>/ Transmission driving tests are performed at $V_{CC} = 5.5$ V with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IL} = 3.0$ V or 0.8 V.
- <u>8</u>/ Power dissipation capacitance (C_{PD}) determines the no load power consumption, $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC}) f$ + (lcc x Vcc) + (n x d x Δ lcc x Vcc). The dynamic current consumption, ls = (C_{PD} + C_L) Vccf + lcc + (n x d x Δ lcc). For both P_D and ls: n is the number of device inputs at TTL levels; f is the frequency of the input signal; and d is the duty cycle of the input signal.
- 9/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at V_{IN} = V_{CC} 2.1 V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.
- 10/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (l_{OL} maximum and l_{OH} maximum = i.e, ±24 mA) and 50 pF of load capacitance (see figure 5). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_r = 3.5 \pm 1.5$ ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 MQ impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (see figure 5). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level with a maximum number of outputs switching.
- $\frac{11}{V_{\text{over}}}$ See JEDEC STD. 17 for electrically induced latch-up test methods and procedures. The values listed for V_{trigger}, I_{trigger} and V_{over}, are to be accurate within ±5 percent.
- 12/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L < 2.5; high inputs = 3.0 V and low inputs = 0.4 V. The input voltage levels have the allowable tolerances in accordance with MIL-STD-883 already incorporated. The V_{IH} level used for functional testing shall be 3.0 V ±0 percent.
- <u>13</u>/ AC limits at $V_{CC} = 5.5$ V are equal to limits at $V_{CC} = 4.5$ V and guaranteed by testing at $V_{CC} = 4.5$ V. Minimum AC limits for $V_{CC} = 5.5$ V are 1.0 ns and guaranteed by guardbanding the $V_{CC} = 4.5$ V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.
- 14/ This parameter shall be guaranteed, if not tested, to the limits in table I, herein.

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Device type		01	
Case			
outlines	E, F	2	
Terminal number	Terminal symbol		
1 2 3 4 5 6 7 8 9 10 11 12 13 14	SR CP P0 P1 P2 P3 CEP GND PE CET Q3 Q2 Q1 Q0	NC SR CP P0 P1 NC P2 P3 CEP GND NC PE CET Q3	
15	тс	Q2	
16	Vcc	NC	
17		Q1	
18		Q0	
19		тс	
20		Vcc	
		L	

PIN Description		
Terminal Symbol	Description	
CEP	Count enable parallel control input	
CET	Count enable trickle control input	
CP	Clock pulse timing input (active rising edge)	
SR	Synchronous master reset control input (active low)	
<u>Pn</u> (n = 0 to 3)	Parallel data inputs	
PE	Parallel enable control input (active low)	
Qn (n = 0 to 3)	Flip-flop outputs	
тс	Terminal count output	

FIGURE 1. Terminal connections.

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SR	PE	CET	CEP	Function
L	х	х	×	Reset (Qn = L, TC = L) (See note 1)
н	L	х	x	Load (Qn = Pn) (See notes 1 and 2)
н	Н	н	н	Count (See notes 1, 2, and 3)
н	H	L	x	No change (See notes 1, 2, and 4)
н	Н	х	L	No change (See notes 1, 2, and 4)

H = High voltage level

L = Low voltage level

X = Irrelevant

NOTES:

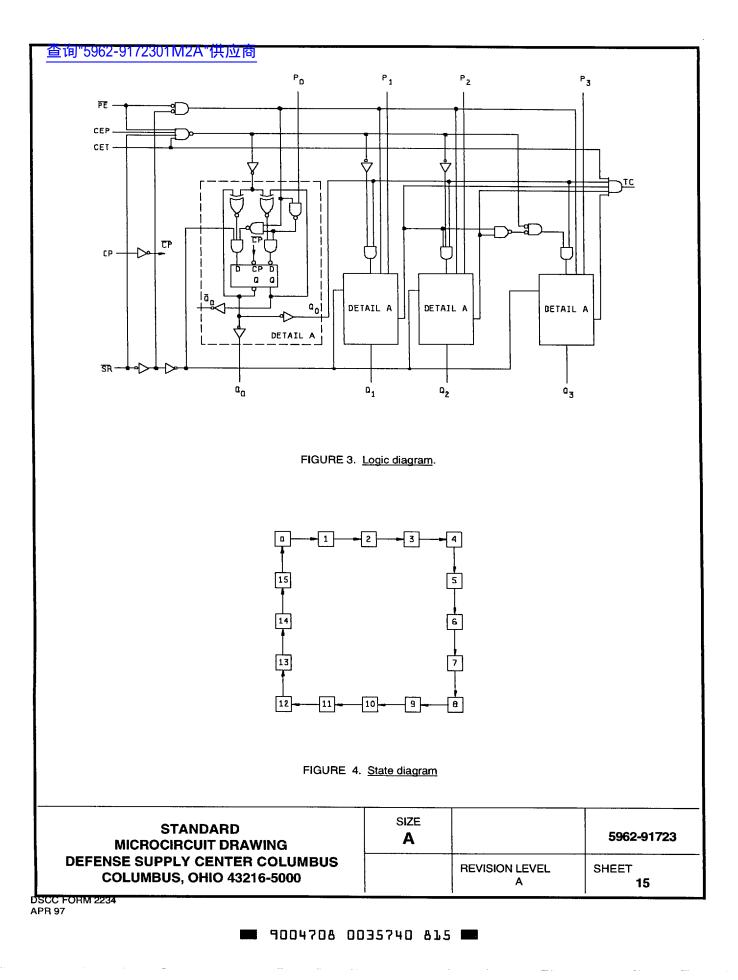
- 1. Action occurs on the rising edge of the clock (CP) input when the appropriate setup, hold, and pulse width timing requirements have been met in table I herein.
- 2. TC = H, whenever the conditions satisfy the logic equation, TC = Q0 Q1 Q2 Q3 CET are valid. For any other conditions, TC = L. The TC output will react to the CET input independent of the clock input. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers, or counters.
- 3. For the counting sequence, see the state diagram on figure 4.
- 4. Outputs maintain their current output state. For TC, the conditions in note 3 apply.

FIGURE 2. Truth table.

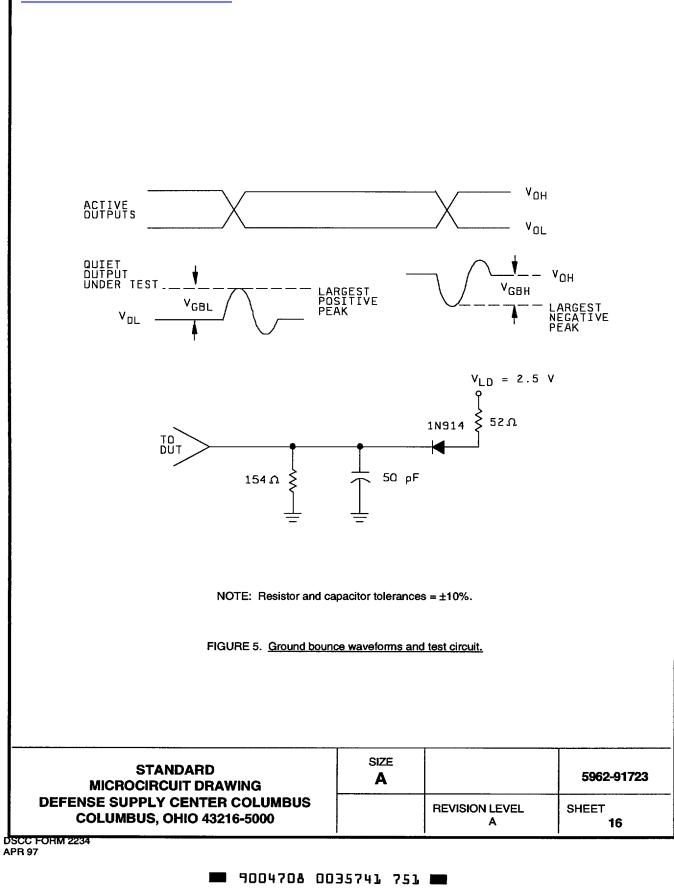
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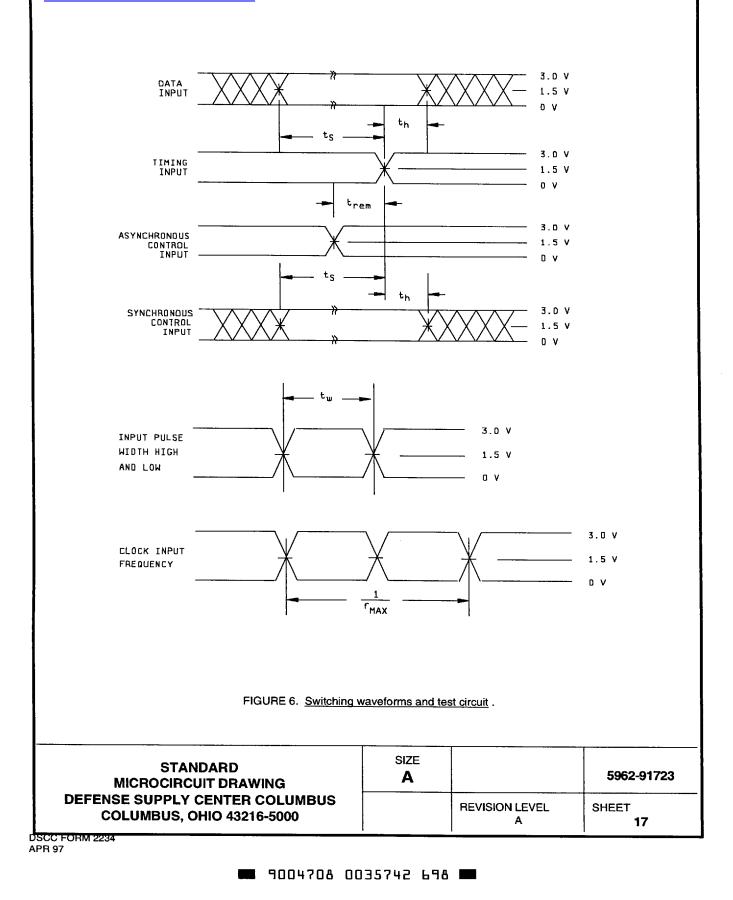
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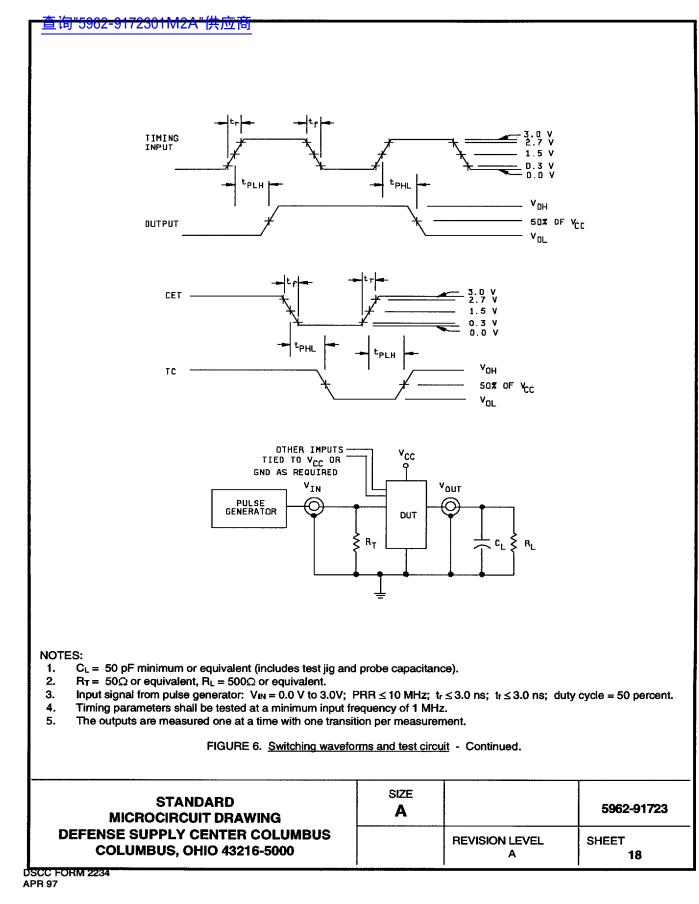






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4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1
Final electrical parameters (see 4.2)	<u>1</u> / 1, 2, 3, 7, 8, 9, 10, 11	<u>1</u> / 1, 2, 3, 7, 8, 9, 10, 11	<u>2</u> / 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

TABLE II. Electrical test requirements.

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Latch-up and ground bounce tests are required for device classes Q and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground-bounce tests, test all applicable pins on five devices with zero failures.
- c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

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For device class M, subgroup 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

- 4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:
 - a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - b. $T_A = +125$ °C, minimum.
 - c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 <u>Additional criteria for device classes Q and V</u>. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.
- d. RHA tests for device class M for levels M, D, L, R, F, G, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- e. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.
- f. For device classes Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

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4.4.4.1 <u>Total dose irradiation testing</u>. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, and as specified herein:

Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

- 1. Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ ±20%, and all outputs are open.
- 2. Inputs tested low, Vcc = 5.5 V dc +5%, Rcc = $10\Omega \pm 20\%$, V_{IN} = 0.0 V dc, R_{IN} = 1 k $\Omega \pm 20\%$, and all outputs are open.

4.4.4.1.1 Accelerated aging test. Accelerated aging shall be performed on class M, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end point electrical parameter limits shall be as specified in table I herein and shall be the preirradiation end point electrical parameter limit at 25° C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

4.5 <u>Methods of inspection</u>. Methods of inspection shall be specified as follows:

4.5.1 <u>Voltage and current</u>. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor- prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 <u>Record of users</u>. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 <u>Approved sources of supply for device class M</u>. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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Approved sources of supply for SMD 5962-91723 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9172301MEA	27014	54ACT163DMQB
5962-9172301MFA	27014	54ACT163FMQB
5962-9172301M2A	27014	54ACT163LMQB
5962R9172301MEA	27014	54ACT163DMQB-RH
5962R9172301MFA	27014	54ACT163FMQB-RH
5962R9172301M2A	27014	54ACT163LMQB-RH
5962R9172301VEA	27014	54ACT163JRQMLV
5962R9172301VFA	27014	54ACT163WRQMLV
5962R9172301V2A	27014	54ACT163ERQMLV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE __number_

27014

Vendor name and address

National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090 Point of contact: 5 Foden Road South Portland, ME 04106-1706

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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