MC14016B

Quad Analog Switch/Quad Multiplexer

The MC14016B quad bilateral switch is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/√Cycle, f ≥ 1.0 kHz typical
- Pin–for–Pin Replacements for CD4016B, CD4066B (Note improved transfer characteristic design causes more parasitic coupling capacitance than CD4016)
- For Lower R_{ON}, Use The HC4016 High–Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

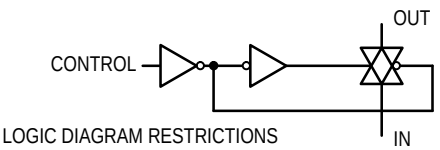
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

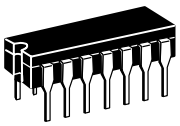
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

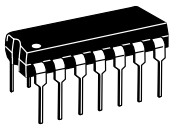
LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



LOGIC DIAGRAM RESTRICTIONS
$V_{SS} \le V_{in} \le V_{DD}$
$V_{SS} \le V_{out} \le V_{DD}$



L SUFFIX
CERAMIC
CASE 632



P SUFFIX
PLASTIC
CASE 646

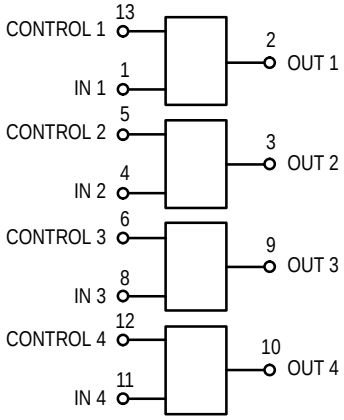
D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

BLOCK DIAGRAM



V_{DD} = PIN 14
V_{SS} = PIN 7

Control	Switch
0 = V_{SS}	Off
1 = V_{DD}	On

REV 3
1/94

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Figure	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Input Voltage Control Input	1	V_{IL}	5.0 10 15	— — —	— — —	— — —	1.5 1.5 1.5	0.9 0.9 0.9	— — —	— — —	Vdc
		V_{IH}	5.0 10 15	— — —	— — —	3.0 8.0 13	2.0 6.0 11	— — —	— — —	— — —	Vdc
Input Current Control	—	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	± 1.0	µAdc
Input Capacitance Control Switch Input Switch Output Feed Through	—	C_{in}	 — — — —	 — — — —	 — — — —	 — — — —	 5.0 5.0 5.0 0.2	 — — — —	 — — — —	 — — — —	pF
Quiescent Current (Per Package)	2,3	I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
"ON" Resistance ($V_C = V_{DD}$, R_L = 10 kΩ) (V_{in} = + 5.0 Vdc) (V_{in} = – 5.0 Vdc) V_{SS} = – 5.0 Vdc (V_{in} = ± 0.25 Vdc) (V_{in} = + 7.5 Vdc) (V_{in} = – 7.5 Vdc) V_{SS} = – 7.5 Vdc (V_{in} = ± 0.25 Vdc) (V_{in} = + 10 Vdc) (V_{in} = + 0.25 Vdc) V_{SS} = 0 Vdc (V_{in} = + 5.6 Vdc) (V_{in} = + 15 Vdc) (V_{in} = + 0.25 Vdc) V_{SS} = 0 Vdc (V_{in} = + 9.3 Vdc)	4,5,6	R_{ON}	 5.0 7.5 10 15	 — — — — — — — — — — — — — —	 600 600 600 360 360 360 600 600 600 360 360 360	— — — — — — — — — — — — — —	 300 300 280 240 240 180 260 310 310 260 260 300	 660 660 660 400 400 400 660 660 660 400 400 400	— — — — — — — — — — — — — —	 840 840 840 520 520 520 840 840 840 520 520 520	Ohms
Δ "ON" Resistance Between any 2 circuits in a common package ($V_C = V_{DD}$) (V_{in} = ± 5.0 Vdc, V_{SS} = – 5.0 Vdc) (V_{in} = ± 7.5 Vdc, V_{SS} = – 7.5 Vdc)	—	ΔR_{ON}	 5.0 7.5	 — —	 — —	 — —	 15 10	 — —	 — —	 — —	Ohms
Input/Output Leakage Current ($V_C = V_{SS}$) (V_{in} = + 7.5, V_{out} = – 7.5 Vdc) (V_{in} = – 7.5, V_{out} = + 7.5 Vdc)	—	—	 7.5 7.5	 — —	 ±0.1 ±0.1	 — —	 ±0.0015 ±0.0015	 ±0.1 ± 0.1	 — —	 ± 1.0 ± 1.0	µAdc

NOTE: All unused inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

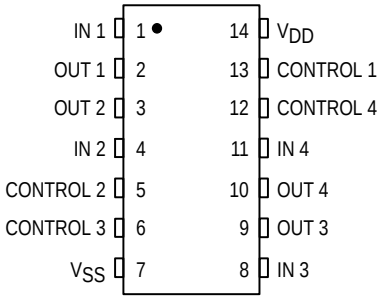
** For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

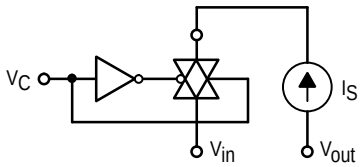
ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Propagation Delay Time (V_{SS} = 0 Vdc) V_{in} to V_{out} (V_C = V_{DD}, R_L = 10 kΩ)	7	t_{PLH}, t_{PHL}	5.0 10 15	— — —	15 7.0 6.0	45 15 12	ns
Control to Output (V_{in} ≤ 10 Vdc, R_L = 10 kΩ)	8	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	 5.0 10 15	 — — —	 34 20 15	 90 45 35	ns
Crosstalk, Control to Output (V_{SS} = 0 Vdc) (V_C = V_{DD}, R_{in} = 10 kΩ, R_{out} = 10 kΩ, f = 1.0 kHz)	9	—	5.0 10 15	— — —	30 50 100	— — —	mV
Crosstalk between any two switches (V_{SS} = 0 Vdc) (R_L = 1.0 kΩ, f = 1.0 MHz, crosstalk = $20\log_{10}\frac{V_{out1}}{V_{out2}}$)	—	—	5.0	—	– 80	—	dB
Noise Voltage (V_{SS} = 0 Vdc) (V_C = V_{DD}, f = 100 Hz) (V_C = V_{DD}, f = 100 kHz)	10,11	—	5.0 10 15 5.0 10 15	— — — — — —	24 25 30 12 12 15	— — — — — —	nV/√Cycle
Second Harmonic Distortion (V_{SS} = – 5.0 Vdc) (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	—	—	5.0	—	0.16	—	%
Insertion Loss (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = – 5.0 Vdc, RMS centered = 0.0 Vdc, f = 1.0 MHz) $I_{loss} = 20\log_{10}\frac{V_{out}}{V_{in}}$) ($R_L$ = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	12	—	5.0	 — — — —	 2.3 0.2 0.1 0.05	 — — — —	dB
Bandwidth (– 3.0 dB) (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = – 5.0 Vdc, RMS centered @ 0.0 Vdc) (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	12,13	BW	5.0	 — — — —	 54 40 38 37	 — — — —	MHz
OFF Channel Feedthrough Attenuation (V_{SS} = – 5.0 Vdc) (V_C = V_{SS}, $20\log_{10}\frac{V_{out}}{V_{in}}$ = –50 dB) (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	—	—	5.0	 — — — —	 1250 140 18 2.0	 — — — —	kHz

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

PIN ASSIGNMENT





V_{IL}: V_C is raised from V_{SS} until $V_C = V_{IL}$.
at $V_C = V_{IL}$: $I_S = \pm 10$ μA with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.

V_{IH}: When $V_C = V_{IH}$ to V_{DD}, the switch is ON and the R_{ON} specifications are met.

Figure 1. Input Voltage Test Circuit

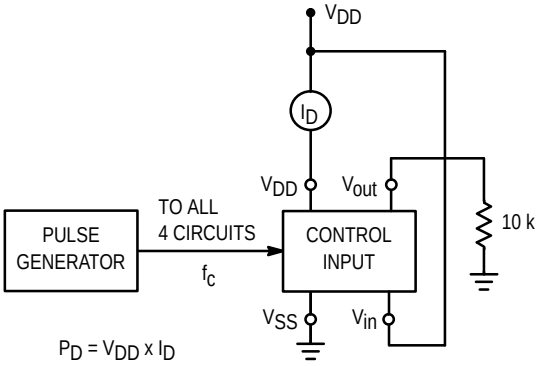


Figure 2. Quiescent Power Dissipation Test Circuit

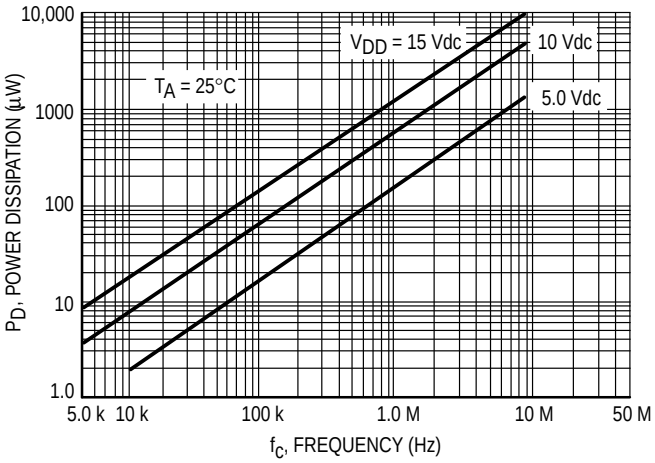


Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)

TYPICAL R_{ON} versus INPUT VOLTAGE

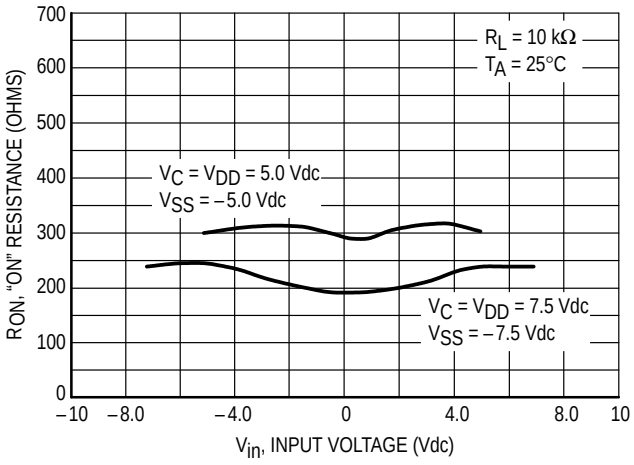


Figure 4. V_{SS} = – 5.0 V and – 7.5 V

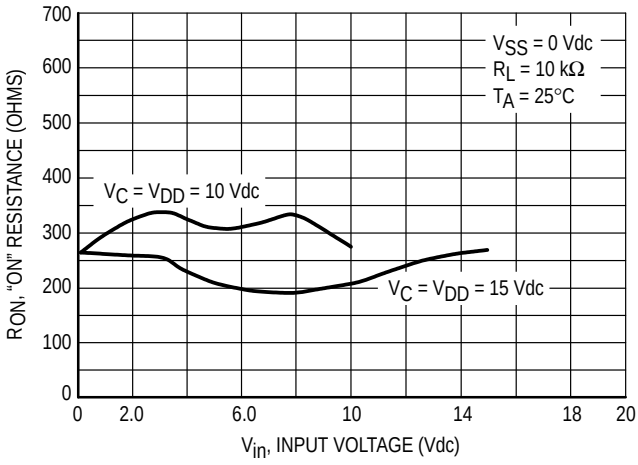


Figure 5. V_{SS} = 0 V

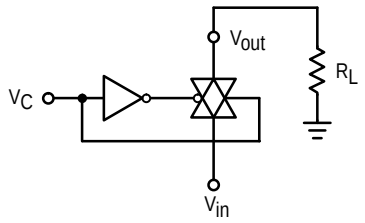


Figure 6. R_{ON} Characteristics Test Circuit

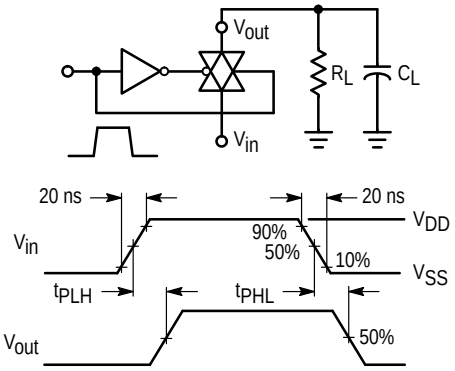


Figure 7. Propagation Delay Test Circuit and Waveforms

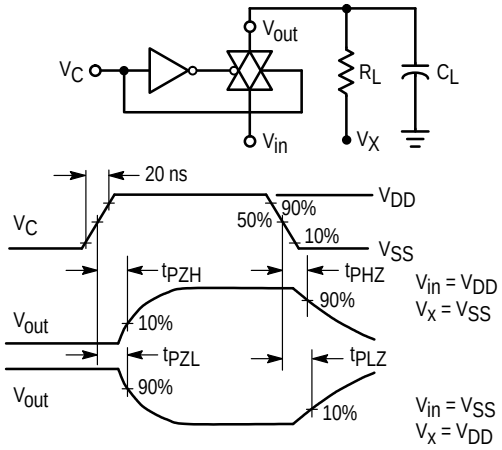


Figure 8. Turn–On Delay Time Test Circuit and Waveforms

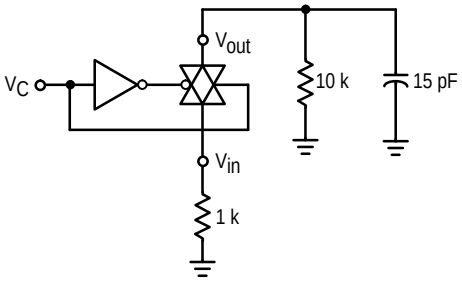


Figure 9. Crosstalk Test Circuit

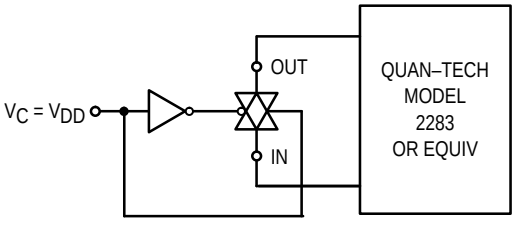


Figure 10. Noise Voltage Test Circuit

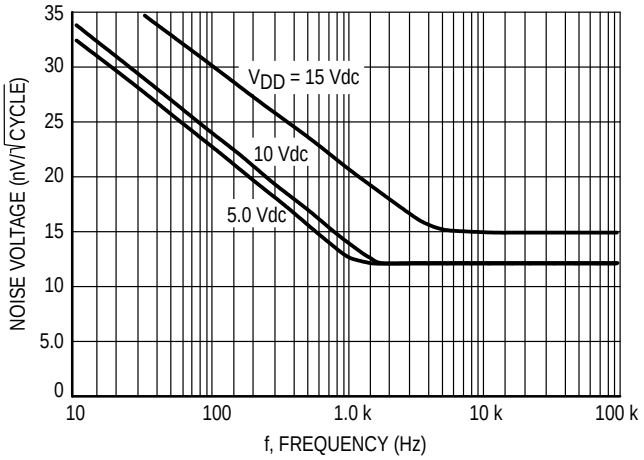


Figure 11. Typical Noise Characteristics

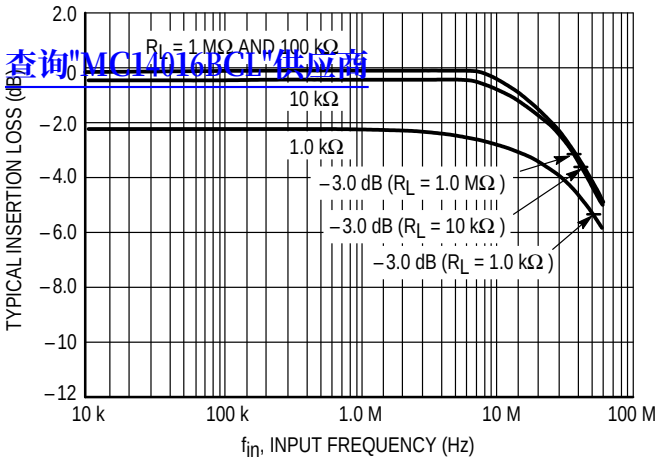


Figure 12. Typical Insertion Loss/Bandwidth Characteristics

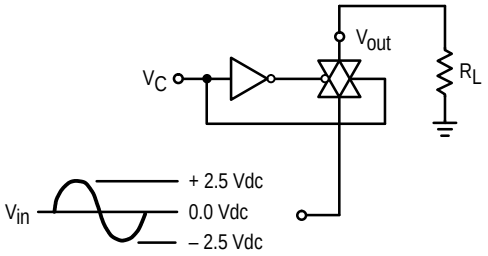


Figure 13. Frequency Response Test Circuit

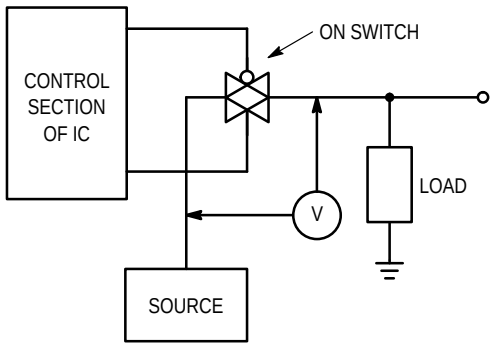


Figure 14. ΔV Across Switch

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0–to–5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V logic high at the control inputs; V_{SS} = GND = 0 V logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS}.

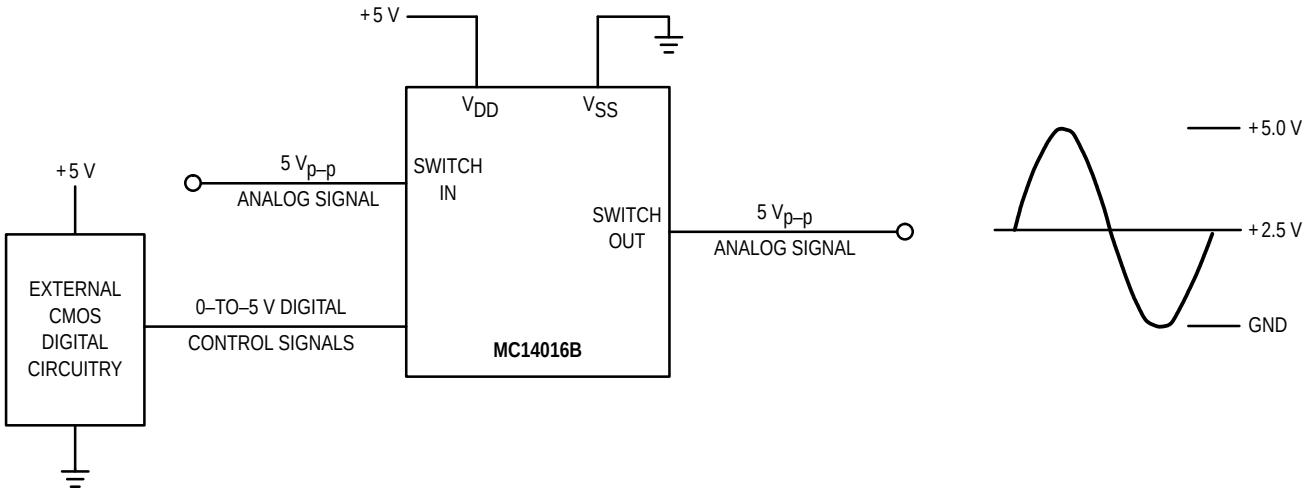


Figure A. Application Example

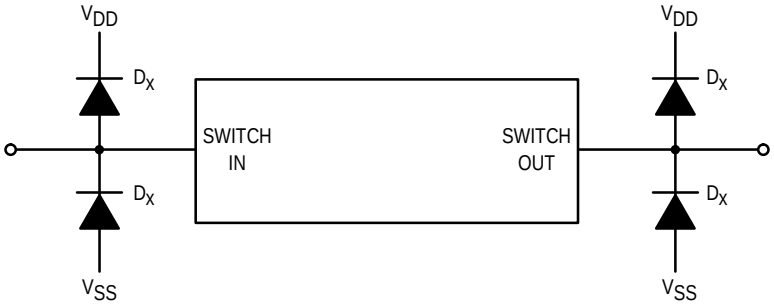
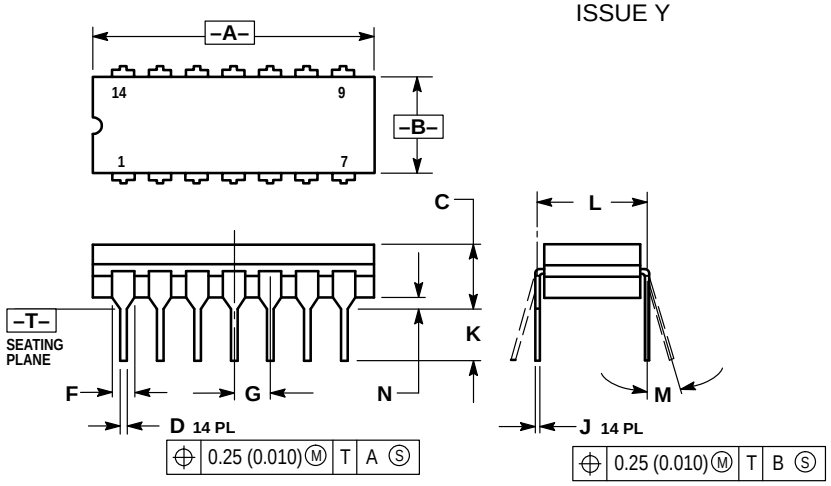


Figure B. External Germanium or Schottky Clipping Diodes

OUTLINE DIMENSIONS

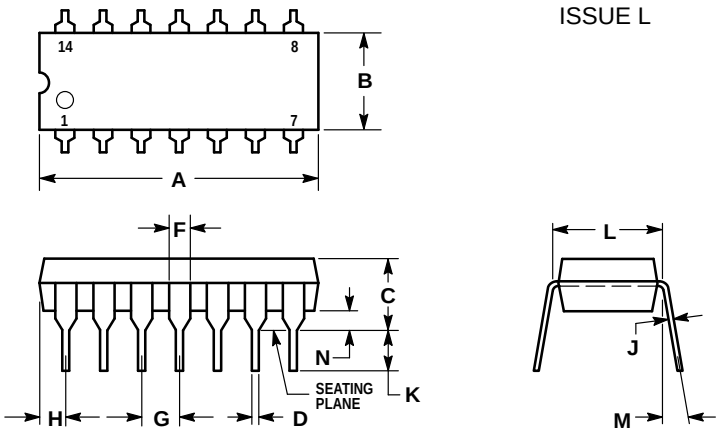
L SUFFIX
CERAMIC DIP PACKAGE
CASE 632–08
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L

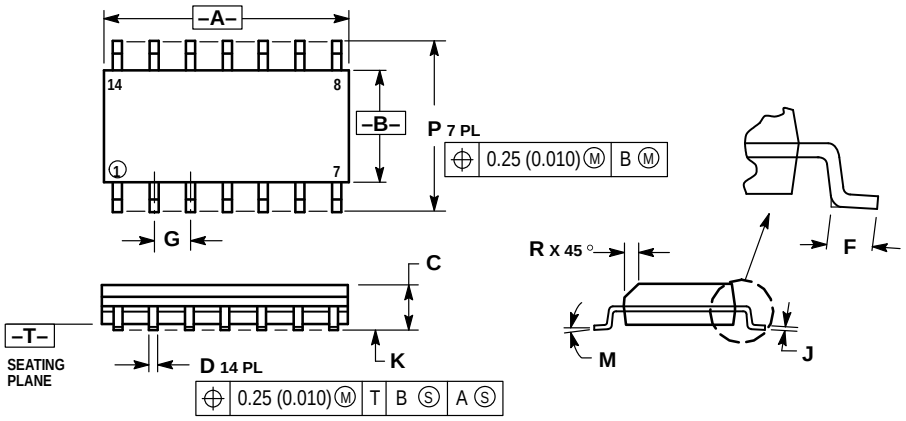


NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298