**Freescale Semiconductor**
Technical Data

Document Number: MRF6V2010N
Rev. 1, 5/2007



# RF Power Field Effect Transistor

## N-Channel Enhancement-Mode Lateral MOSFETs

**MRF6V2010NR1**
**MRF6V2010NBR1**

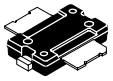
**10-450 MHz, 10 W, 50 V**
**LATERAL N-CHANNEL**
**BROADBAND**
**RF POWER MOSFETs**

Designed primarily for CW large-signal output and driver applications with frequencies up to 450 MHz. Devices are unmatched and are suitable for use in industrial, medical and scientific applications.

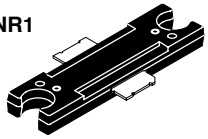
- Typical CW Performance at 220 MHz: $V_{DD}$ = 50 Volts, $I_{DQ}$ = 30 mA, $P_{out}$ = 10 Watts
  Power Gain — 23.9 dB
  Drain Efficiency — 62%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 220 MHz, 10 Watts CW Output Power

**Features**

- Integrated ESD Protection
- Excellent Thermal Stability
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 200°C Capable Plastic Package
- RoHS Compliant
- TO-270-2 in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.
- TO-272-2 in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



**CASE 1265-08, STYLE 1**
**TO-270-2**
**PLASTIC**
**MRF6V2010NR1**



**CASE 1337-03, STYLE 1**
**TO-272-2**
**PLASTIC**
**MRF6V2010NBR1**

**Table 1. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | -0.5, +110 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | -0.5, +10 | Vdc |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 200 | °C |

**Table 2. Thermal Characteristics**

| Characteristic | Symbol | Value (1,2) | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case<br>Case Temperature 81°C, 10 W CW | $R_{\theta JC}$ | 3.0 | °C/W |

1. MTTF calculator available at http://www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.



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**Table 3. ESD Protection Characteristics**

| Test Methodology | Class |
|---|---|
| Human Body Model (per JESD22-A114) | 2 (Minimum) |
| Machine Model (per EIA/JESD22-A115) | A (Minimum) |
| Charge Device Model (per JESD22-C101) | IV (Minimum) |

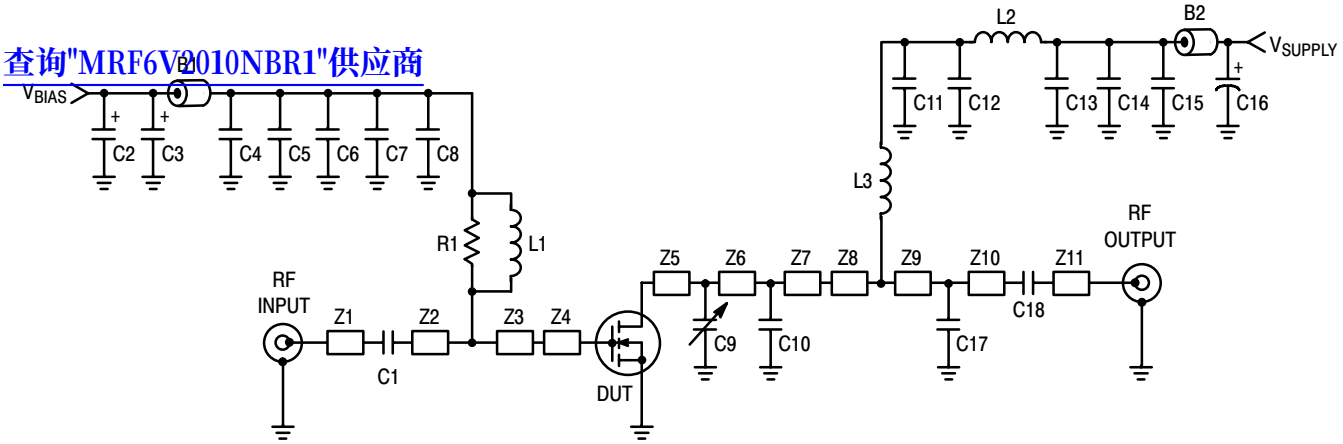
**Table 4. Moisture Sensitivity Level**

| Test Methodology | Rating | Package Peak Temperature | Unit |
|---|---|---|---|
| Per JESD 22-A113, IPC/JEDEC J-STD-020 | 3 | 260 | °C |

**Table 5. Electrical Characteristics** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Off Characteristics** | | | | | |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 2.5 | mA |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 50 | μAdc |
| Drain-Source Breakdown Voltage ($I_D$ = 5 mA, $V_{GS}$ = 0 Vdc) | $V_{(BR)DSS}$ | 110 | — | — | Vdc |
| Gate-Source Leakage Current ($V_{GS}$ = 5 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | — | — | 10 | μAdc |
| **On Characteristics** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 28 μAdc) | $V_{GS(th)}$ | 1 | 1.68 | 3 | Vdc |
| Gate Quiescent Voltage ($V_{DD}$ = 50 Vdc, $I_D$ = 30 mAdc, Measured in Functional Test) | $V_{GS(Q)}$ | 1.5 | 2.68 | 3.5 | Vdc |
| Drain-Source On-Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 70 mAdc) | $V_{DS(on)}$ | — | 0.26 | — | Vdc |
| **Dynamic Characteristics** | | | | | |
| Reverse Transfer Capacitance ($V_{DS}$ = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc) | $C_{rss}$ | — | 0.13 | — | pF |
| Output Capacitance ($V_{DS}$ = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc) | $C_{oss}$ | — | 7.3 | — | pF |
| Input Capacitance ($V_{DS}$ = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc) | $C_{iss}$ | — | 16.3 | — | pF |
| **Functional Tests** (In Freescale Test Fixture, 50 ohm system) $V_{DD}$ = 50 Vdc, $I_{DQ}$ = 30 mA, $P_{out}$ = 10 W, f = 220 MHz, CW | | | | | |
| Power Gain | $G_{ps}$ | 22.5 | 23.9 | 25.5 | dB |
| Drain Efficiency | $\eta_D$ | 58 | 62 | — | % |
| Input Return Loss | IRL | — | -14 | -9 | dB |

ATTENTION: The MRF6V2010N and MRF6V2010NB are high power devices and special considerations must be followed in board design and mounting. Incorrect mounting can lead to internal temperatures which exceed the maximum allowable operating junction temperature. Refer to Freescale Application Note AN3263 (for bolt down mounting) or AN1907 (for solder reflow mounting) **PRIOR TO STARTING SYSTEM DESIGN** to ensure proper mounting of these devices.




| | | | |
|---|---|---|---|
| Z1 | 0.235″ x 0.082″ Microstrip | Z7 | 0.062″ x 0.270″ Microstrip |
| Z2 | 1.190″ x 0.082″ Microstrip | Z8 | 0.198″ x 0.082″ Microstrip |
| Z3 | 0.619″ x 0.082″ Microstrip | Z9 | 5.600″ x 0.082″ Microstrip |
| Z4 | 0.190″ x 0.270″ Microstrip | Z10 | 0.442″ x 0.082″ Microstrip |
| Z5 | 0.293″ x 0.270″ Microstrip | Z11 | 0.341″ x 0.082″ Microstrip |
| Z6 | 0.120″ x 0.270″ Microstrip | PCB | Arlon GX-0300-55-22, 0.030″, $\varepsilon_r$ = 2.55 |

**Figure 1. MRF6V2010NR1(NBR1) Test Circuit Schematic**

**Table 6. MRF6V2010NR1(NBR1) Test Circuit Component Designations and Values**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| B1, B2 | 95 Ω, 100 MHz Long Ferrite Beads | 2743021447 | Fair-Rite |
| C1, C8, C11, C18 | 1000 pF Chip Capacitors | ATC100B102JT50XT | ATC |
| C2 | 10 μF, 35 V Tantalum Capacitor | T491D106K035AT | Kemet |
| C3 | 22 μF, 35 V Tantalum Capacitor | T491X226K035AT | Kemet |
| C4, C13 | 39 K pF Chip Capacitors | ATC200B393KT50XT | ATC |
| C5, C14 | 22 K pF Chip Capacitors | ATC200B223KT50XT | ATC |
| C6, C15 | 0.1 μF Chip Capacitors | CDR33BX104AKYS | Kemet |
| C7, C12 | 2.2 μF, 50 V Chip Capacitors | C1825C225J5RAC | Kemet |
| C9 | 0.6-4.5 pF Variable Capacitor, Gigatrim | 27271SL | Johanson |
| C10 | 12 pF Chip Capacitor | ATC100B120JT500XT | ATC |
| C16 | 470 μF, 63 V Electrolytic Capacitor | ESMG630ELL471MK205 | United Chemi-Con |
| C17 | 27 pF Chip Capacitor | ATC100B270JT500XT | ATC |
| L1 | 17.5 nH Inductor | B06T | CoilCraft |
| L2, L3 | 82 nH Inductors | 1812SMS-82NJ | CoilCraft |
| R1 | 120 Ω, 1/4 W Chip Resistor | CRCW12061200FKTA | Vishay |

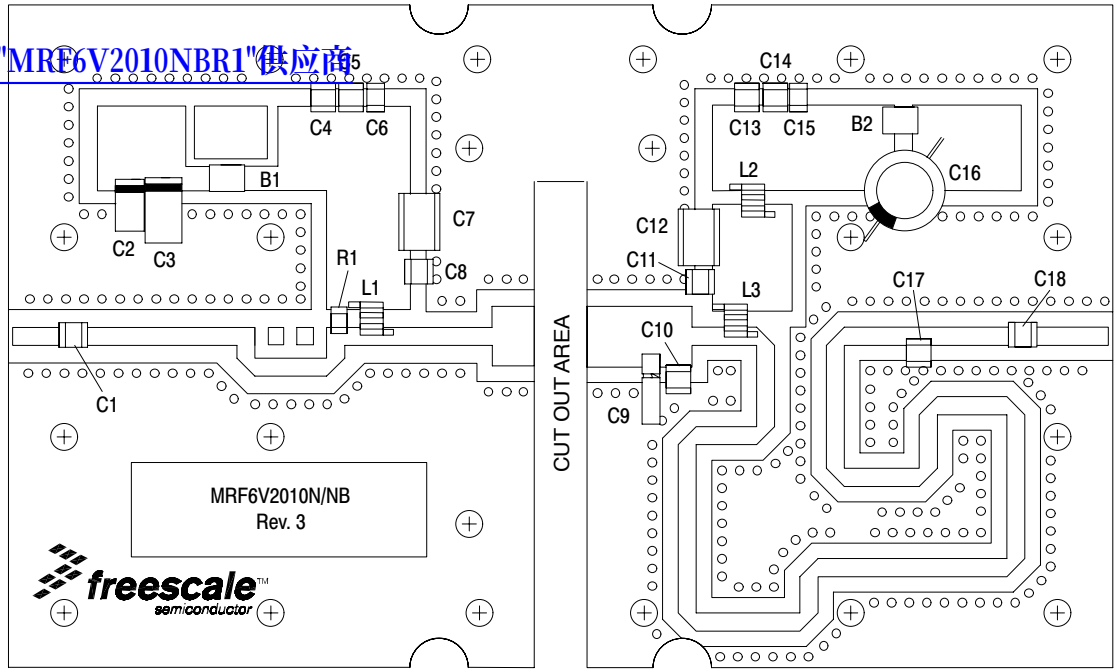



**Figure 2. MRF6V2010NR1(NBR1) Test Circuit Component Layout**

## TYPICAL CHARACTERISTICS



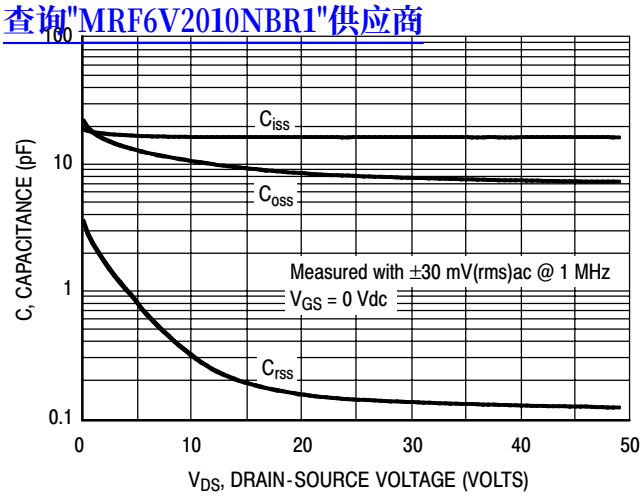



**Figure 3. Capacitance versus Drain-Source Voltage**

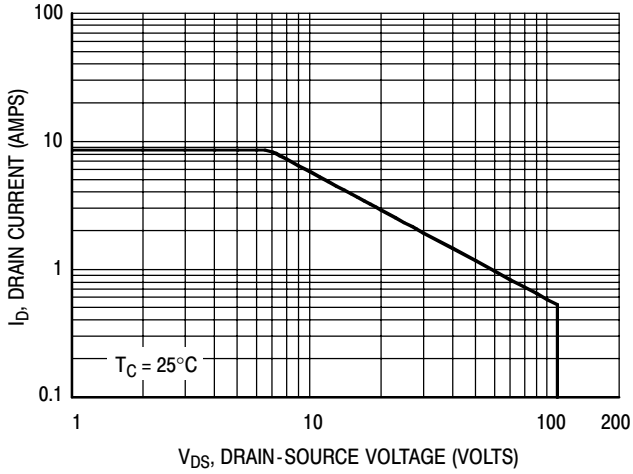



**Figure 4. DC Safe Operating Area**

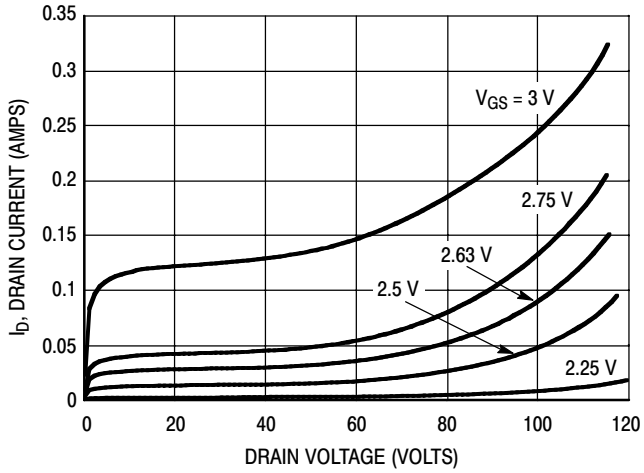



**Figure 5. DC Drain Current versus Drain Voltage**

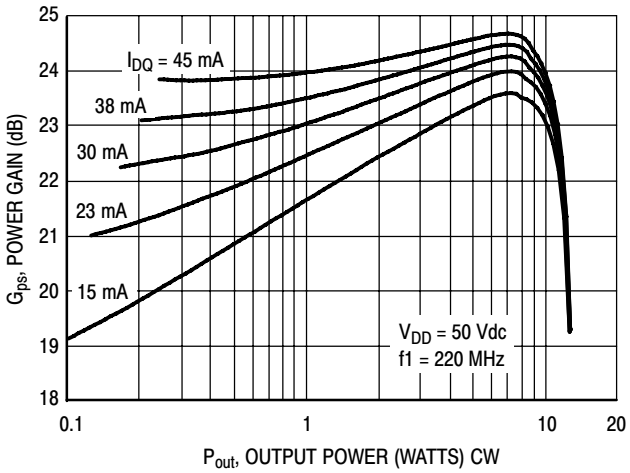



**Figure 6. CW Power Gain versus Output Power**

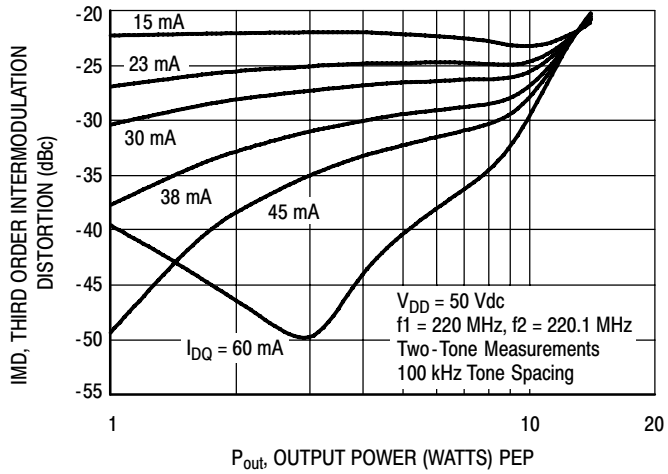



**Figure 7. Third Order Intermodulation Distortion versus Output Power**

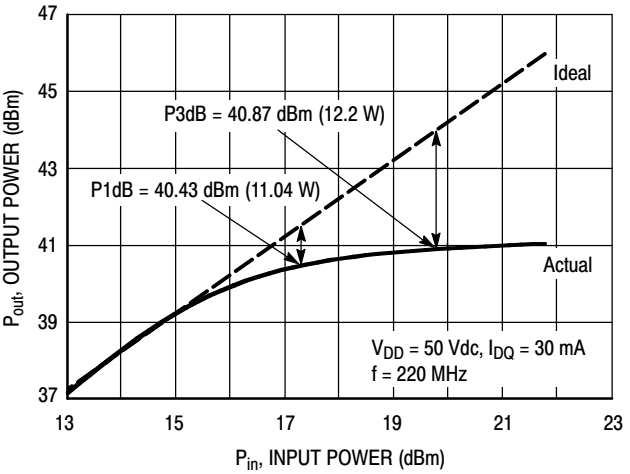



**Figure 8. CW Output Power versus Input Power**

## TYPICAL CHARACTERISTICS



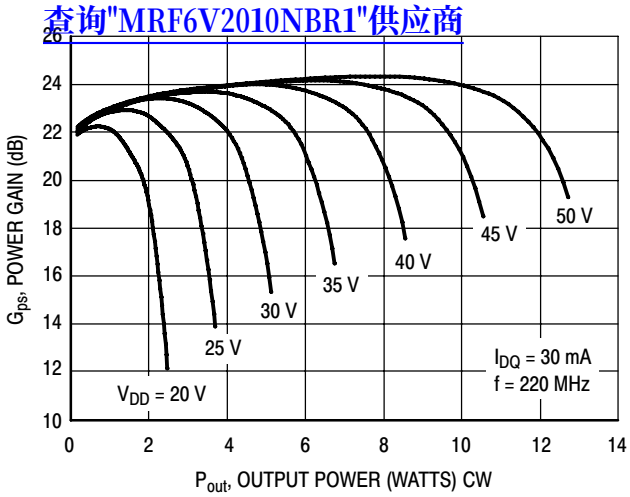



**Figure 9. Power Gain versus Output Power**

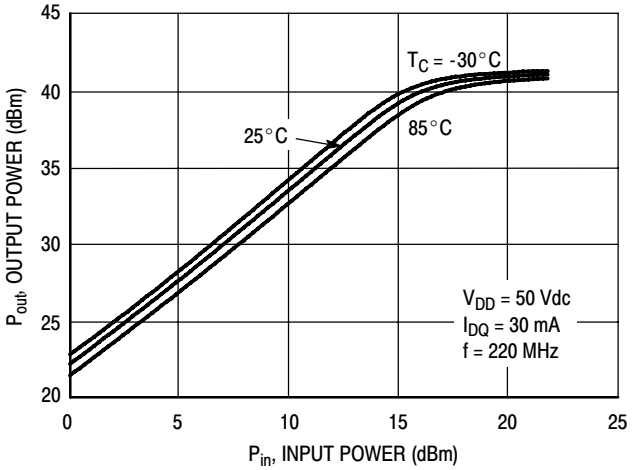



**Figure 10. Power Output versus Power Input**

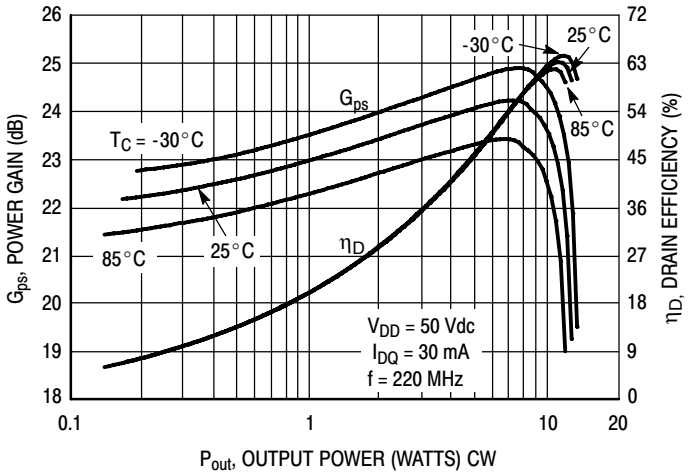
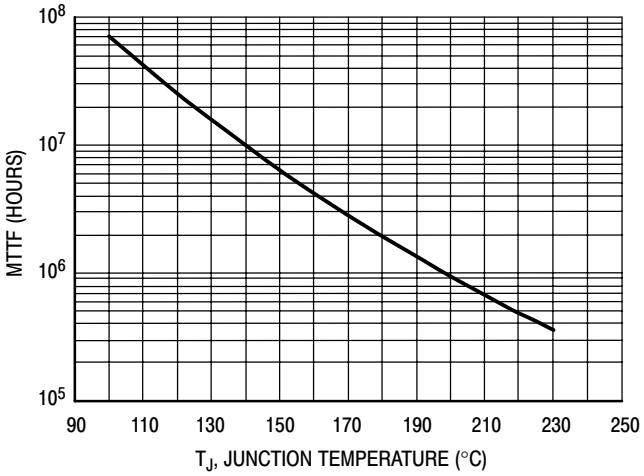


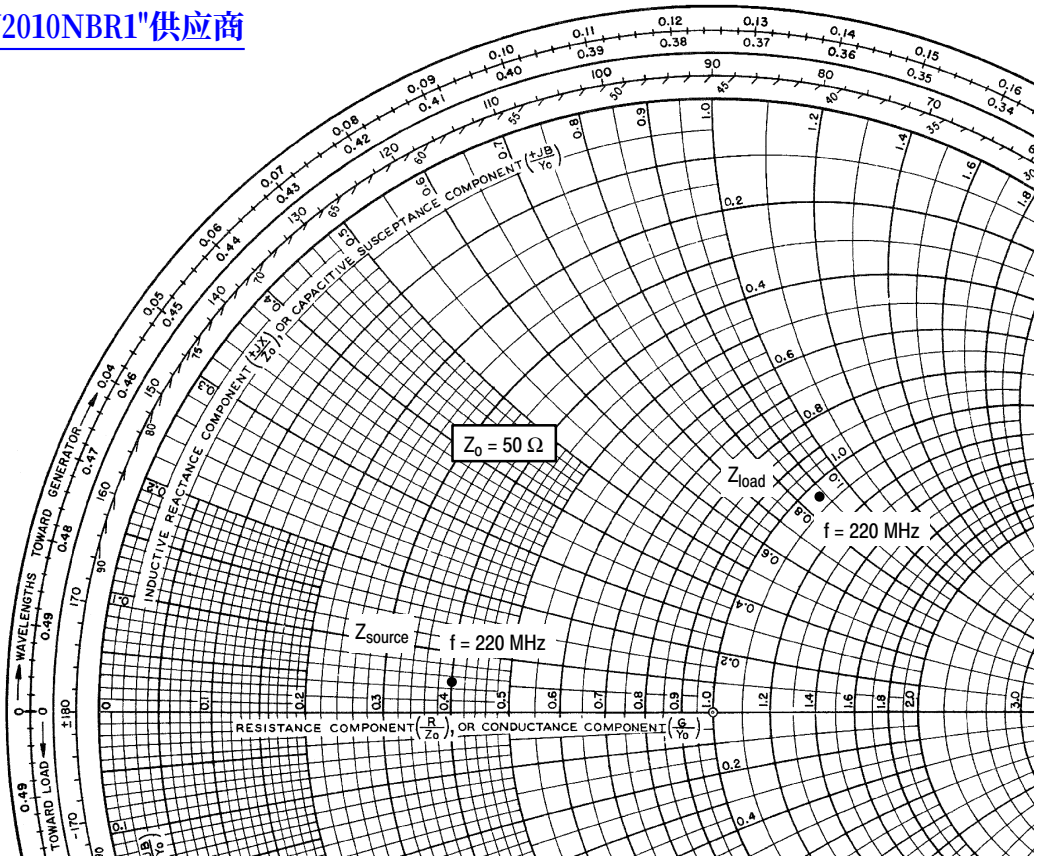

**Figure 11. Power Gain and Drain Efficiency versus CW Output Power**




This above graph displays calculated MTTF in hours when the device is operated at $V_{DD}$ = 50 Vdc, $P_{out}$ = 10 W CW, and $\eta_D$ = 62%.

MTTF calculator available at http:/www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

**Figure 12. MTTF versus Junction Temperature**




$V_{DD}$ = 50 Vdc, $I_{DQ}$ = 30 mA, $P_{out}$ = 10 W CW

| f MHz | $Z_{source}$ Ω | $Z_{load}$ Ω |
|---|---|---|
| 220 | 20 + j25 | 75 + j44 |

$Z_{source}$ = Test circuit impedance as measured from gate to ground.

$Z_{load}$ = Test circuit impedance as measured from drain to ground.

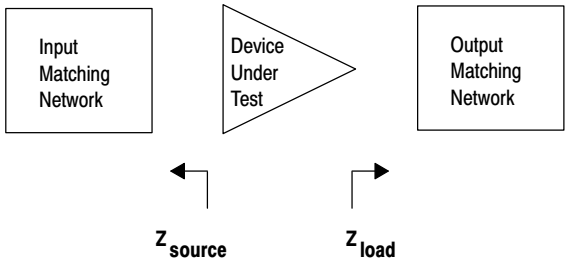
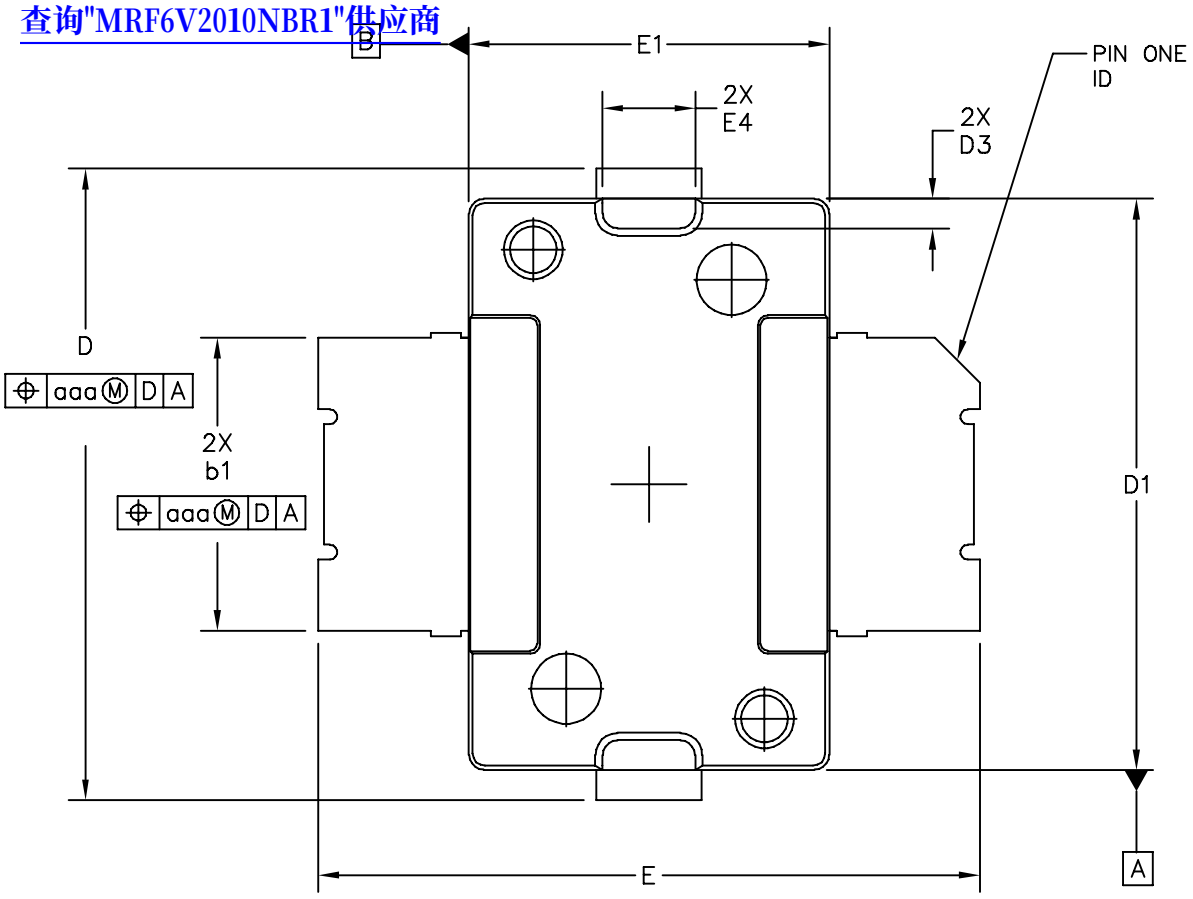
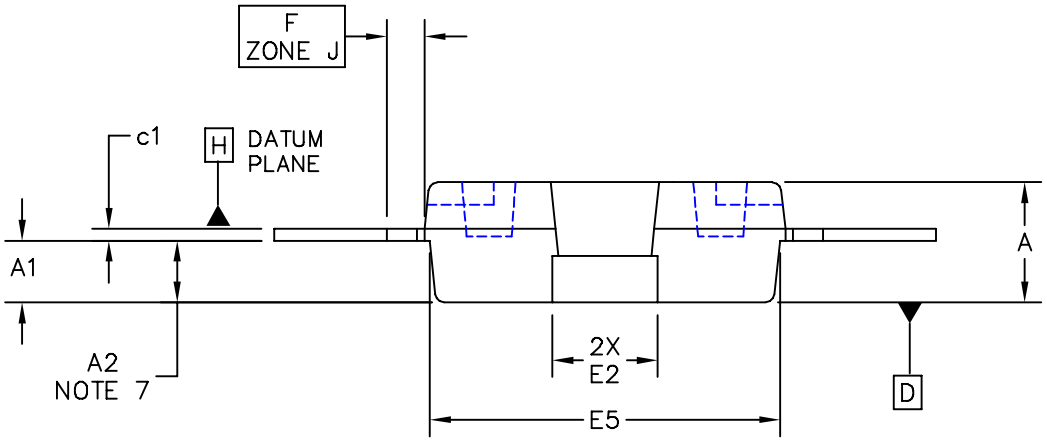



**Figure 13. Series Equivalent Source and Load Impedance**

## PACKAGE DIMENSIONS



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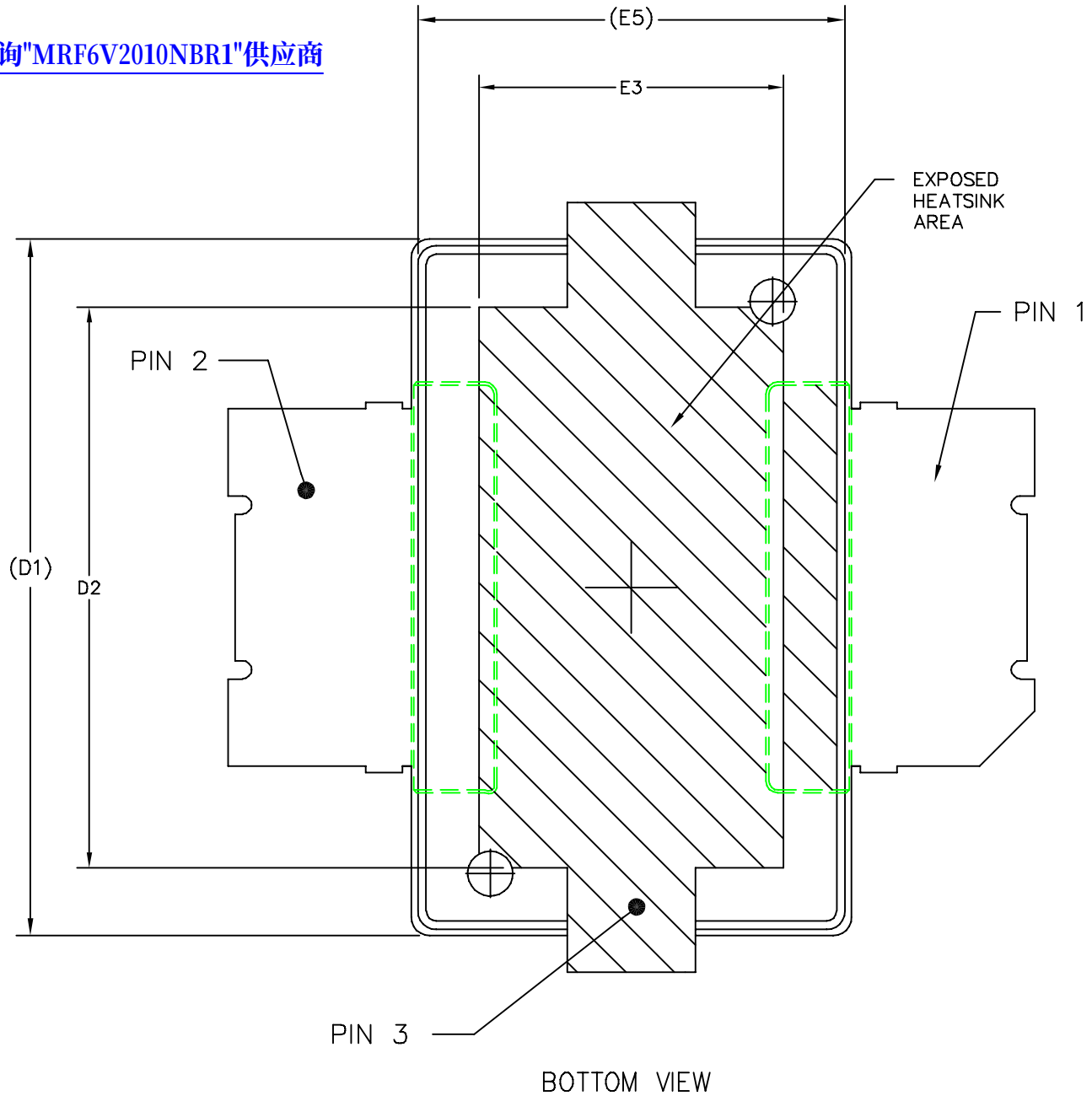
|---|---|---|
| TITLE: TO-270 SURFACE MOUNT | DOCUMENT NO: 98ASH98117A | REV: J |
| | CASE NUMBER: 1265-08 | 01 APR 2005 |
| | STANDARD: NON-JEDEC | |

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| | CASE NUMBER: 1265-08 | 01 APR 2005 |
| | STANDARD: NON-JEDEC | |

NOTES:
1. CONTROLLING DIMENSION: INCH.



2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1 AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION "A2" APPLIES WITHIN ZONE "J" ONLY.

8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH FOR DIMENSION "D" AND 0.080 INCH FOR DIMENSION "E2". DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –D–.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

| DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX | DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX |
|---|---|---|---|---|---|---|---|---|---|
| A | .078 | .082 | 1.98 | 2.08 | F | .025 BSC | | 0.64 BSC | |
| A1 | .039 | .043 | 0.99 | 1.09 | b1 | .193 | .199 | 4.90 | 5.06 |
| A2 | .040 | .042 | 1.02 | 1.07 | c1 | .007 | .011 | 0.18 | 0.28 |
| D | .416 | .424 | 10.57 | 10.77 | aaa | .004 | | 0.10 | |
| D1 | .378 | .382 | 9.60 | 9.70 | | | | | |
| D2 | .290 | .320 | 7.37 | 8.13 | | | | | |
| D3 | .016 | .024 | 0.41 | 0.61 | | | | | |
| E | .436 | .444 | 11.07 | 11.28 | | | | | |
| E1 | .238 | .242 | 6.04 | 6.15 | | | | | |
| E2 | .066 | .074 | 1.68 | 1.88 | | | | | |
| E3 | .150 | .180 | 3.81 | 4.57 | | | | | |
| E4 | .058 | .066 | 1.47 | 1.68 | | | | | |
| E5 | .231 | .235 | 5.87 | 5.97 | | | | | |



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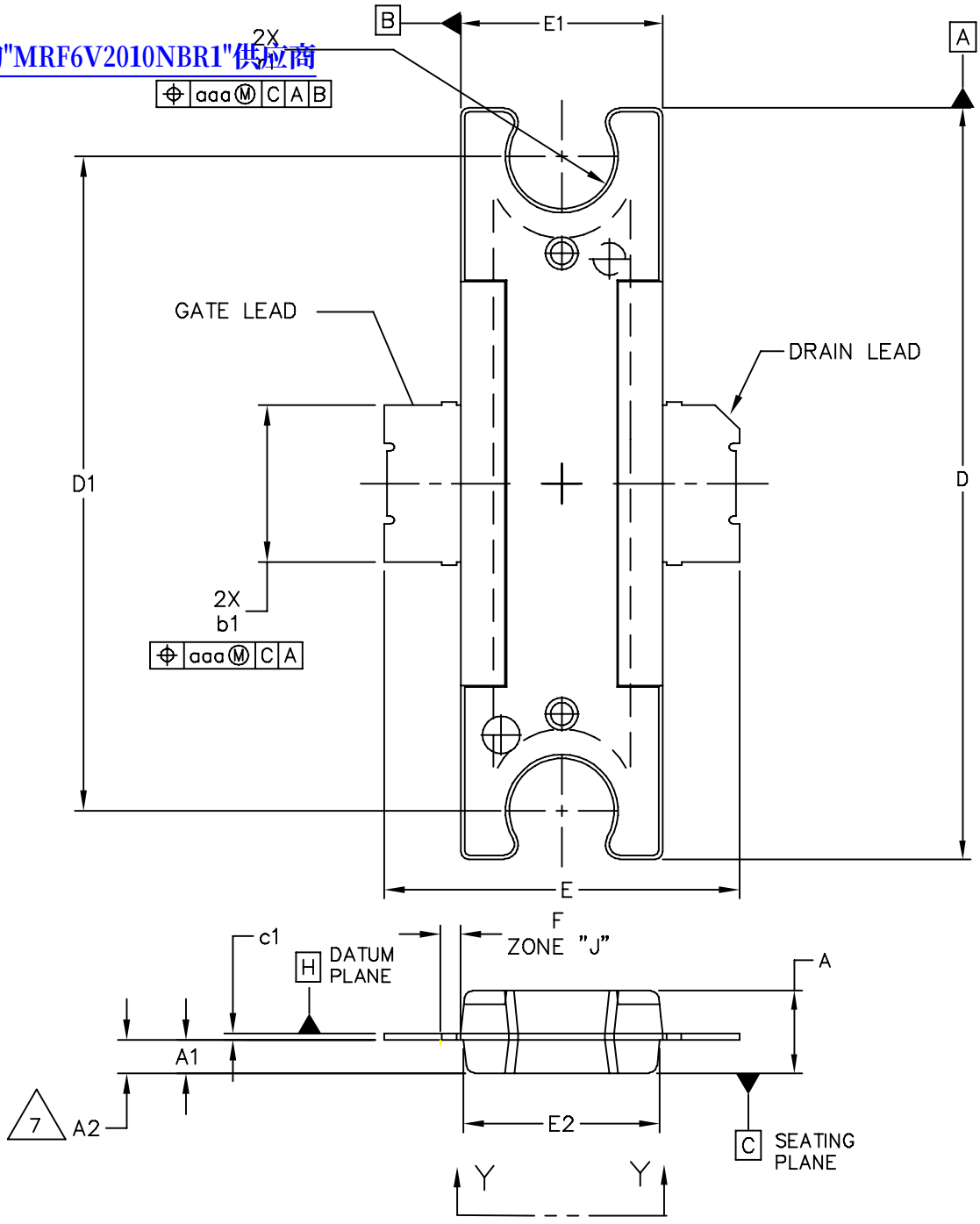
| | STANDARD: NON–JEDEC | |

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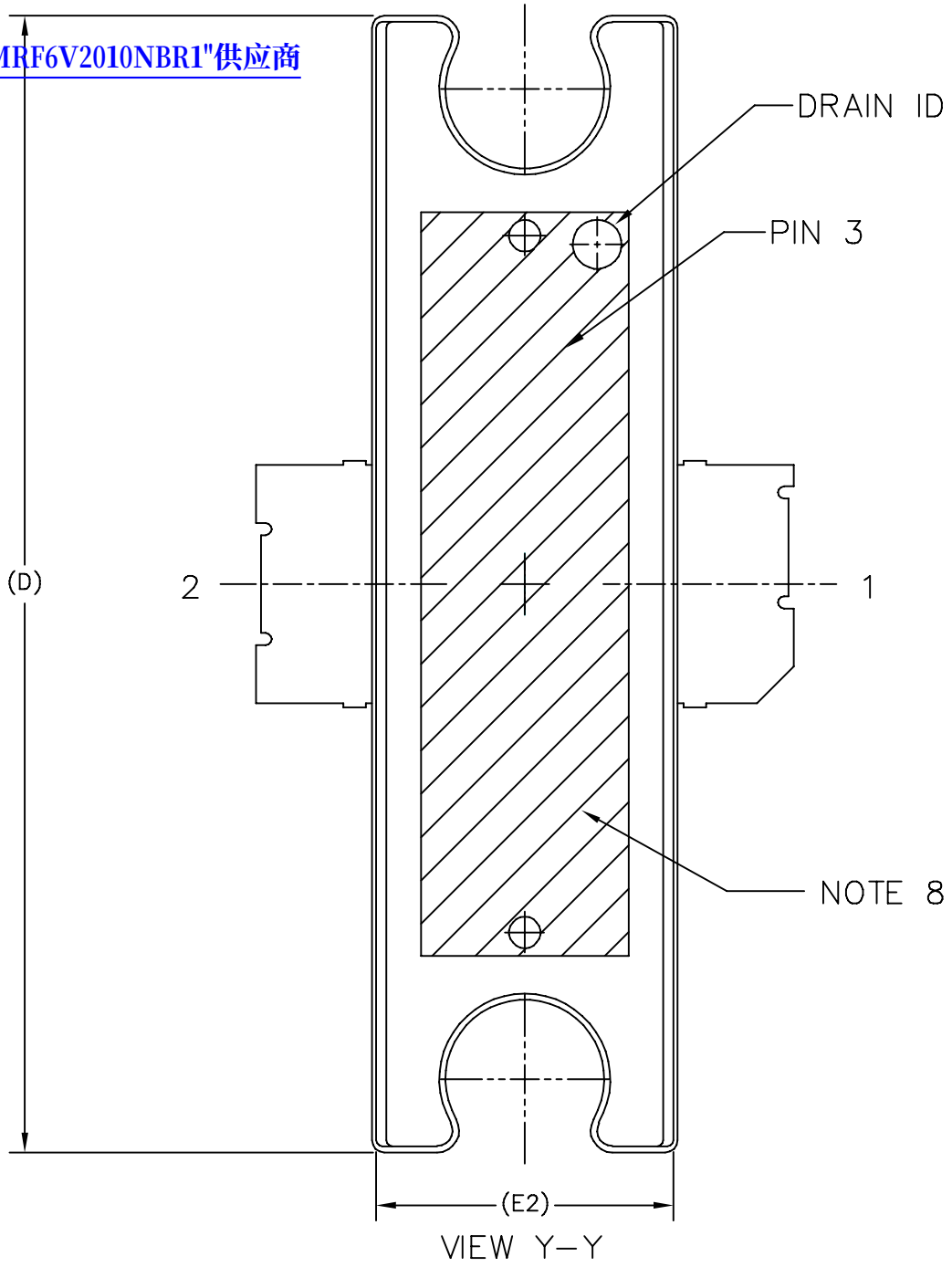
| | CASE NUMBER: 1337-03 | 21 MAR 2005 |
| | STANDARD: NON-JEDEC | |

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| TITLE: TO–272 2 LEAD | DOCUMENT NO: 98ASA99191D | REV: C |
| | CASE NUMBER: 1337–03 | 21 MAR 2005 |
| | STANDARD: NON–JEDEC | |

NOTES:

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6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

| DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX | DIM | INCH MIN | INCH MAX | MILLIMETER MIN | MILLIMETER MAX |
|---|---|---|---|---|---|---|---|---|---|
| A | .100 | .104 | 2.54 | 2.64 | b1 | .193 | .199 | 4.90 | 5.05 |
| A1 | .039 | .043 | 0.99 | 1.09 | c1 | .007 | .011 | .18 | .28 |
| A2 | .040 | .042 | 1.02 | 1.07 | r1 | .063 | .068 | 1.60 | 1.73 |
| D | .928 | .932 | 23.57 | 23.67 | aaa | | .004 | | .10 |
| D1 | .810 BSC | | 20.57 BSC | | | | | | |
| E | .438 | .442 | 11.12 | 11.23 | | | | | |
| E1 | .248 | .252 | 6.30 | 6.40 | | | | | |
| E2 | .241 | .245 | 6.12 | 6.22 | | | | | |
| F | .025 BSC | | 0.64 BSC | | | | | | |



| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE: | DOCUMENT NO: 98ASA9919D | REV: C |
|---|---|---|
| TO–272<br>2 LEAD | CASE NUMBER: 1337–03 | 21 MAR 2005 |
| | STANDARD: NON–JEDEC | |

## PRODUCT DOCUMENTATION



Refer to the following documents to aid your design process.

**Application Notes**

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

**Engineering Bulletins**

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|---|---|---|
| 0 | Feb. 2007 | • Initial Release of Data Sheet |
| 1 | May 2007 | • Corrected Test Circuit Component part numbers in Table 6, Component Designations and Values for C1, C8, C11, C18, C4, C13, C5, and C14, p. 3<br>• Corrected Series Impedance $Z_{source}$ and $Z_{load}$ values, Fig. 13, Series Equivalent Source and Load Impedance, p. 7 |

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