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MPC8313E PowerQUICC™ II Pro Processor Hardware Specifications

This document provides an overview of the MPC8313E PowerQUICC™ II Pro processor features, including a block diagram showing the major functional components. The MPC8313E is a cost-effective, low-power, highly integrated host processor that addresses the requirements of several printing and imaging, consumer, and industrial applications, including main CPUs and I/O processors in printing systems, networking switches and line cards, wireless LANs (WLANs), network access servers (NAS), VPN routers, intelligent NIC, and industrial controllers. The MPC8313E extends the PowerQUICC™ family, adding higher CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and package size.

Contents

1 Overview

The MPC8313E incorporates the e300c3 core, which includes 16 Kbytes of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8313E has interfaces to dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers, a DDR1/DDR2 SDRAM memory controller, an enhanced local bus controller, a 32-bit PCI controller, a dedicated security

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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engine, a USB 2.0 dual-role controller and an on-chip full-speed PHY, a programmable interrupt controller, dual I^2C controllers, a 4-channel DMA controller, and a general-purpose I/O port. A block diagram of the MPC8313E is shown in Figure 1.

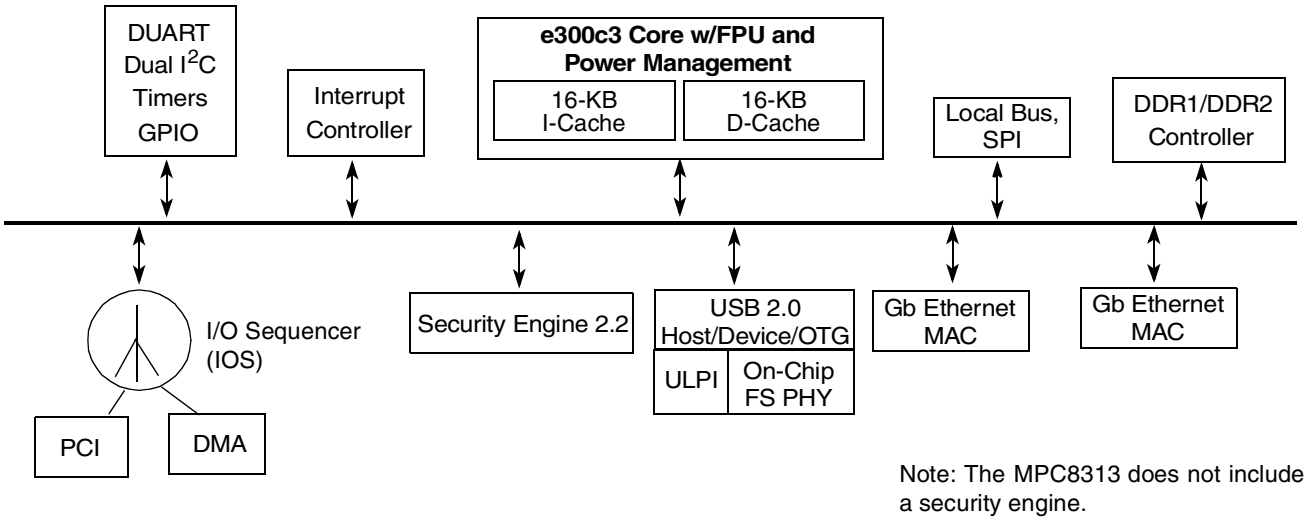


Figure 1. MPC8313E Block Diagram

The MPC8313E's security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

1.1 MPC8313E Features

The following features are supported in the MPC8313E.

- Embedded PowerPC™ e300 processor core; operates at up to 333 MHz.
- High-performance, low-power, and cost-effective host processor
- DDR1/DDR2 memory controller—one 16-/32-bit interface at up to 333 MHz supporting both DDR1 and DDR2
- e300c3 core, built on Power Architecture™ technology, with 16-Kbyte instruction cache and 16-Kbyte data cache, a floating point unit, and two integer units
- Peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit enhanced local bus interface with up to 66-MHz operation, and USB 2.0 (full speed) with an on-chip PHY.
- Security engine provides acceleration for control and data plane security protocols
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

1.2 Serial Interfaces

The following interfaces are supported in the MPC8313E.

- Dual UART, dual I^2C, and an SPI interface

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE Std. 802.11i™, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-224, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8313E DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 333-MHz
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 1-Gbit devices with x8/x16/x32 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus OR one 32-bit device or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.5 PCI Controller

The MPC8313E PCI controller includes the following features:

- PCI specification revision 2.3 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Complies with USB Specification, Rev. 2.0
- Supports operation as a stand-alone USB device
  - — Supports one upstream facing port
  - — Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - — Supports USB root hub with one downstream-facing port
  - — Enhanced host controller interface (EHCI) compatible
- Supports full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB-2.0 full-speed PHY

1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Stds. 802.3™, 802.3u™, 802.3x™, 802.3z™, 802.3au™, and 802.3ab™
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std. 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std. 802.2™, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues

- Full- and half-duplex Ethernet support (1000 Mbps supports only full-duplex):
- IEEE Std. 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1™ virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
- Per-frame VLAN control word or default VLAN for each eTSEC
- Extracted VLAN control word passed to software separately
- Retransmission following a collision
- CRC generation and verification of inbound/outbound packets
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
- Exact match on primary and virtual 48-bit unicast addresses
- VRRP and HSRP support for seamless router fail-over
- Up to 16 exact-match MAC addresses supported
- Broadcast address (accept/reject)
- Hash table match on up to 512 multicast addresses
- Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status

1.8 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.9 Power Management Controller (PMC)

The MPC8313E power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI Power Management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (magic packet), USB, GPIO, and PCI (PME input as host)

1.10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.11 DMA Controller, Dual I^2C, DUART, Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters).
- Supports misaligned transfers

There are two I^2C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. The FCM provides a glueless interface to parallel-bus NAND Flash E2PROM devices. The FCM contains three basic configuration register groups–BR*n*, OR*n*, and FMR. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8313E. The MPC8313E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	
PLL supply voltage		AV_{DD}	–0.3 to 1.26	V	
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		NV_{DD}/LV_{DD}	–0.3 to 3.6	V	
eTSEC, USB		LV_{DDA}/LV_{DDB}	–0.3 to 3.6	V	
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Enhanced Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DDA} + 0.3) or –0.3 to (LV_{DDB} + 0.3)	V	4, 5
	Local bus, DUART, SYS_CLK_IN, system control, and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	6

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T_{STG}	–55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DDA}/LV_{DDB} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. $(L,M,O)V_{IN}$ and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8313E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Current requirement
SerDes (Lynx) internal digital power	XCOREVDD	1.0	V	100 mA
SerDes (Lynx) internal digital power	XCOREVSS	0.0	V	
SerDes (Lynx) I/O digital power	XPADVDD	1.0	V	10mA
SerDes (Lynx) I/O digital power	XPADVSS	0.0	V	
SerDes (Lynx) analog power for PLL	SDAVDD	1.0	V	10 mA
SerDes (Lynx) analog power for PLL	SDAVSS	0.0	V	
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3	V	2–3 mA
Dedicated 1.0 V analog power for USB PLL	USB_PLL_PWR1	1.0	V	2–3 mA
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	
Dedicated USB power for USB Bias circuit	USB_VDDA_BIAS	3.3	V	4–5 mA
Dedicated USB ground for USB Bias circuit	USB_VSSA_BIAS	0.0	V	
Dedicated power for USB Transceiver	USB_VDDA	3.3	V	75 mA
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	
Core supply voltage	V_{DD}	1.0	V	560 mA
Internal core logic constant power	V_{DDC}	1.0	V	454 mA

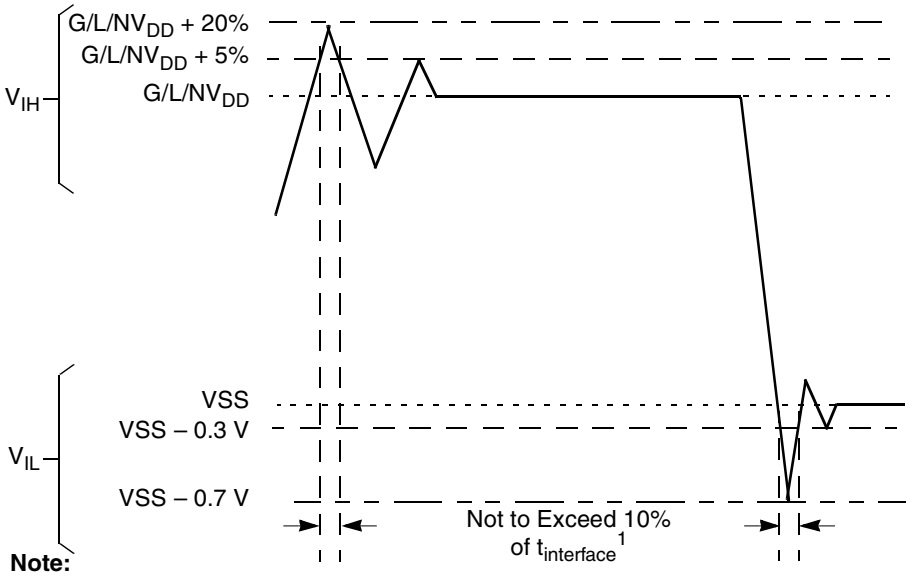
Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value[1]	Unit	Current requirement
Analog power for e300 core APLL	AV_{DD1}	1.0	V	10 mA
Analog power for system APLL	AV_{DD2}	1.0	V	10 mA
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5/1.8	V	425 mA
Differential reference voltage for DDR controller	MV_{REF}	1/2 DDR Supply	V	
Standard I/O Voltage	NV_{DD}	3.3	V	27 mA
eTSEC2 IO Supply	LV_{DDA}	2.5/3.3	V	85 mA
eTSEC1/USB DR IO Supply	LV_{DDB}	2.5/3.3	V	85 mA
Supply for eLBCIOs	LV_{DD}	3.3	V	60 mA
Analog and Digital Ground	VSS	0.0	V	

Notes:

1. GVDD, OVDD, AVDD, and VDD must track each other and must vary in the same direction–either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8313E.



Note:

1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/NV_{DD}/LV_{DD}$

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8313E for the 3.3-V signals, respectively.

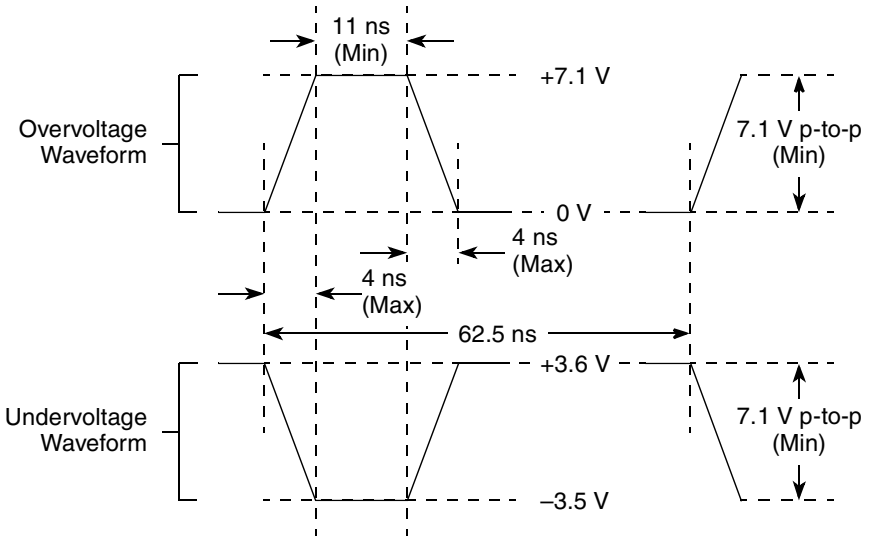


Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NV_{DD} = 3.3 V
PCI signals	25	
DDR signal	18	GV_{DD} = 2.5 V
DDR2 signal	18	GV_{DD} = 1.8 V
DUART, system control, I2C, JTAG,SPI	42	NV_{DD} = 3.3 V
GPIO signals	42	NV_{DD} = 3.3 V
eTSEC signals	42	LV_{DDA}, LV_{DDB} = 2.5/3.3 V
USB Signals	42	LV_{DDB} = 2.5/3.3 V

2.2 Power Sequencing

The MPC8313E does not require the core supply voltage and IO supply voltages to be applied in any particular order. Note that during the power ramp-up, before the power supplies are stable, there might be a period when IO pins are actively driven. After the power is stable, as long as $\overline{\text{PORESET}}$ is asserted, most IO pins are tri-stated. In order to minimize the time that IO pins are being actively driven, it is

recommended to apply core voltage before IO voltage and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up.

3 Power Characteristics

The estimated typical power dissipation for this family of MPC8313E devices is shown in Table 4, and Table 5 shows the estimated typical I/O power dissipation.

Table 4. MPC8313E Power Dissipation [1]

Core Frequency (MHz)	CSB Frequency (MHz)	Typical [2, 3]	Maximum [2,3]	Unit
267	133	680	880	mW
333	167	820	1020	mW

Note:
1. The values do not include I/O supply power or AV_{dd}.
2. Typical power is based on a voltage of V_{dd} = 1.05V, a junction temperature of T_j = 105°C, and an artificial smoker test.
3. These are preliminary estimates

1

Table 5. MPC8313E Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LV_{DDA}/LV_{DDB} (3.3V)	LV_{DDA}/LV_{DDB} (2.5V)	LV_{DDB} (3.3V)	Unit	Comments
DDR 1, 60% utilzation, 50% read/write Rs = 22Ω Rt = 50Ω single pair of clock Capacitive Load: Data = 8pF, Control Address = 8pF, Clock = 8pF	333MHz, 32 bits	—	0.355					W	
	266MHz, 32 bits	—	0.323					W	
	200MHz, 32 bits	—	0.291					W	
DDR 2, 60% utilization, 50% read/write Rs = 22Ω Rt = 75Ω single pair of clock Capacitive Load: Data = 8pF, Control Address = 8pF, Clock = 8pF	333MHz, 32 bits	0.266	—					W	
	266MHz, 32 bits	0.246	—					W	
	200MHz, 32bits	0.225	—					W	
PCI I/O load = 50pF	33 MHz			0.120				W	
	66 MHz			0.249				W	
Local bus I/O load = 20pF	66 MHz			0.056				W	
	50 MHz			0.040				W	

Table 5. MPC8313E Typical I/O Power Dissipation (continued)

TSEC I/O load = 20pF	MII, 25MHz				0.008			W	Multiple by number of interface used
	RGMII, 125MHz					0.044		W	
USBDR controller load = 20pF	60 MHz						0.078	W	
Other I/O				0.015				W	

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8313E.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8313E.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	NV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN Input current	0 V ≤ V_{IN} ≤ NV_{DD}	I_{IN}	—	±10	μA
PCI_SYNC_IN Input current	0 V ≤ V_{IN} ≤ 0.5 V or NV_{DD} – 0.5 V ≤ V_{IN} ≤ NV_{DD}	I_{IN}	—	±10	μA
PCI_SYNC_IN Input current	0.5 V ≤ V_{IN} ≤ NV_{DD} – 0.5 V	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

Table 7. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYS_CLK_IN/PCI_CLK frequency	$f_{SYS\_CLK\_IN}$	25	—	66	MHz	1
SYS_CLK_IN/PCI_CLK cycle time	$t_{SYS\_CLK\_IN}$	15	—	—	ns	—
SYS_CLK_IN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

5.1 RESET DC Electrical Characteristics

Table 8 provides the DC electrical characteristics for the RESET pins.

Table 8. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$		±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

5.2 RESET AC Electrical Characteristics

Table 9 provides the reset initialization AC timing specifications.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to SYS_CLK_IN when the device is in PCI host mode	32	—	$t_{SYS\_CLK\_IN}$	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$/ $\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and $\overline{\text{CFG\_SYS\_CLK\_IN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	$t_{SYS\_CLK\_IN}$	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	

Table 9. RESET Initialization Timing Specifications (continued)

Time for the device to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of $\overline{\text{CFG\_CLKIN\_DIV}}$.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR2 SDRAM component(s) when GV_{DD}(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V	
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 12 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 13 provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 13. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.3	2.7	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.15$	$GV_{DD} + 0.3$	V	
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.15$	V	
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 14 provides the DDR capacitance when GV_{DD} (typ)=2.5 V.

Table 14. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 15 provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ)$=1.8 V.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ±5%

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	

Table 17 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ)$=2.5 V.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ±5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	

Table 18 provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 18. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 2.5 ±5%

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ//MDM	t_{CISKEW}			ps	1, 2
333 MHz		–750	750		
266 MHz		–750	750		
200 MHz		–1250	1250		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = +/–(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 19. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	6	10	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
333 MHz		2.1	—		
266 MHz		2.5	—		
200 MHz		3.5	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
333 MHz		800	—		
266 MHz		900	—		
200 MHz		1000	—		
MDQ//MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
333 MHz		900	—		
266 MHz		1100	—		
200 MHz		1200	—		

Table 19. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Host Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

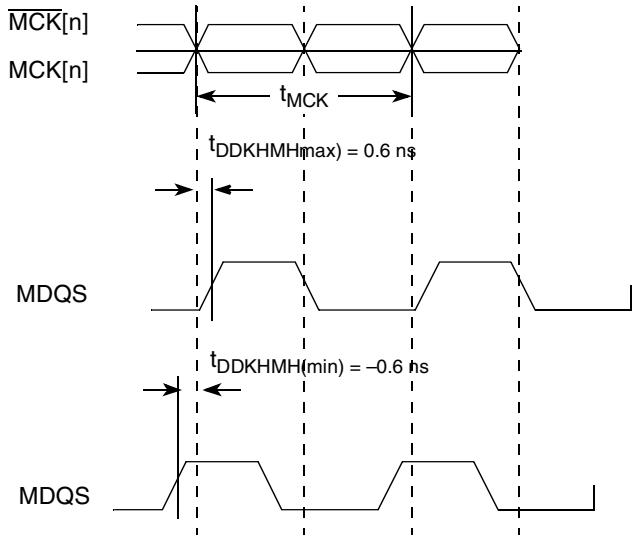


Figure 4. Timing Diagram for t_{DDKHMH}

Figure 5 shows the DDR and DDR2 SDRAM output timing diagram.

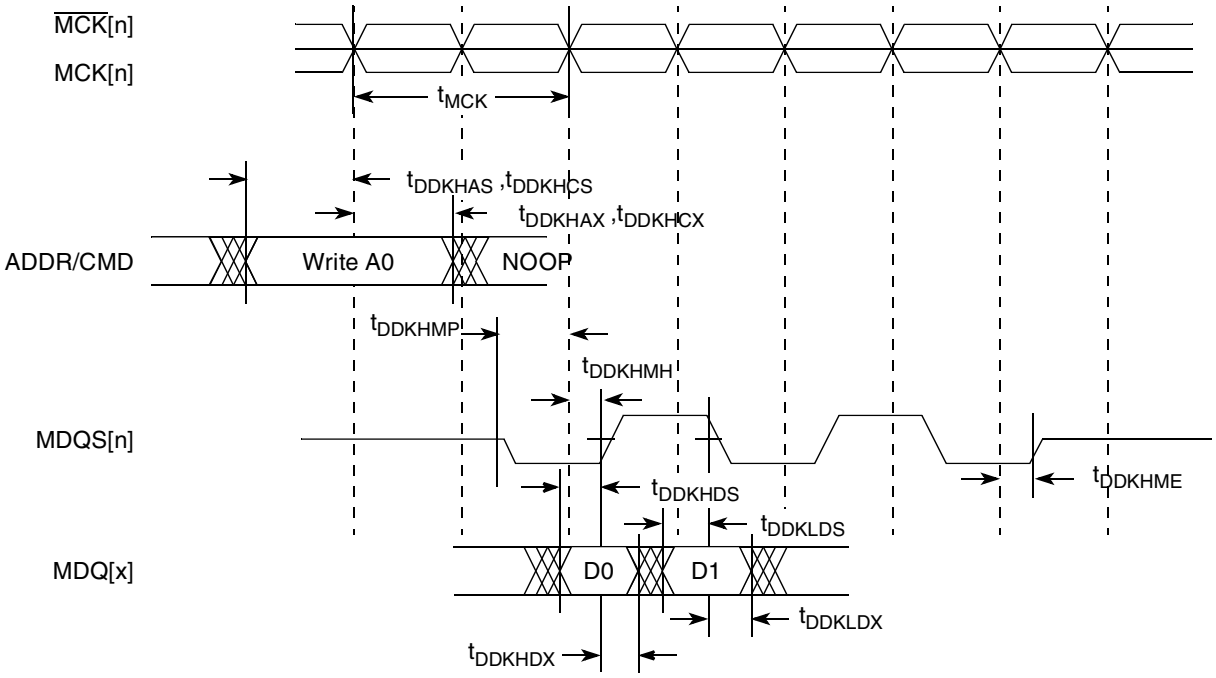


Figure 5. DDR and DDR2 SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

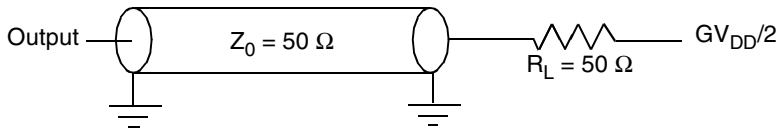


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

Table 20 provides the DC electrical characteristics for the DUART interface.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	NV_{DD} + 0.3	V
Low-level input voltage NVDD	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	NV_{DD} – 0.2	—	V

Table 20. DUART DC Electrical Characteristics (continued)

Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current ($0 V \le V_{IN} \le NV_{DD}$)	I_{IN}	—	± 5	µA

7.2 DUART AC Electrical Specifications

Table 21 provides the AC timing parameters for the DUART interface.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the MII (media independent interface), RGMII (reduced gigabit media independent interface), SGMII (serial gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII interface is defined for 3.3V, while the RMII, RGMII, SGMII, and RTBI interfaces can be operated at 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 TSEC DC Electrical Characteristics

All RGMII, SGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 22 and Table 23. The potential applied to the input of a MII, RGMII, SGMII, or RTBI receiver may exceed the potential of the receiver's power supply (that is, a RGMII driver powered from a 3.6-V supply driving V_{OH} into a RGMII receiver powered from a 2.5-V supply). Tolerance for dissimilar RGMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 22. MII/RGMII/RTBI (When Operating at 3.3V) DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DDA}/LV_{DDB}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DDA} or LV_{DDB} = Min	2.40	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DDA} or LV_{DDB} = Min	VSS	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN} [1] = LV_{DDA} or LV_{DDB}		—	40	µA
Input low current	I_{IL}	V_{IN} [1] = VSS		–600	—	µA

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 23. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DDA}/LV_{DDB}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DDA} or LV_{DDB} = Min	2.00	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DDA} or LV_{DDB} = Min	VSS – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DDA} or LV_{DDB} = Min	1.7	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DDA} or LV_{DDB} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} [1] = LV_{DDA} or LV_{DDB}		—	10	µA
Input low current	I_{IL}	V_{IN} [1] = VSS		–15	—	µA

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 MII, RGMII, SGMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RMII, RGMII, SGMII, and RTBI are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

Table 24 provides the MII transmit AC timing specifications.

Table 24. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} /NV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns

Table 24. MII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DDA}/LV_{DDB} /NV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 7 shows the MII transmit AC timing diagram.

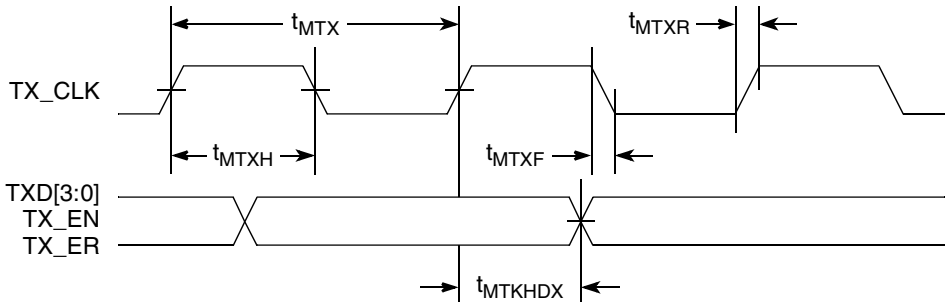


Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

Table 25 provides the MII receive AC timing specifications.

Table 25. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} /NV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns

Table 25. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DDA}/LV_{DDB} /NV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load for TSEC.

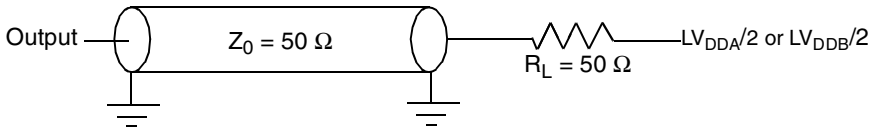


Figure 8. TSEC AC Test Load

Figure 9 shows the MII receive AC timing diagram.

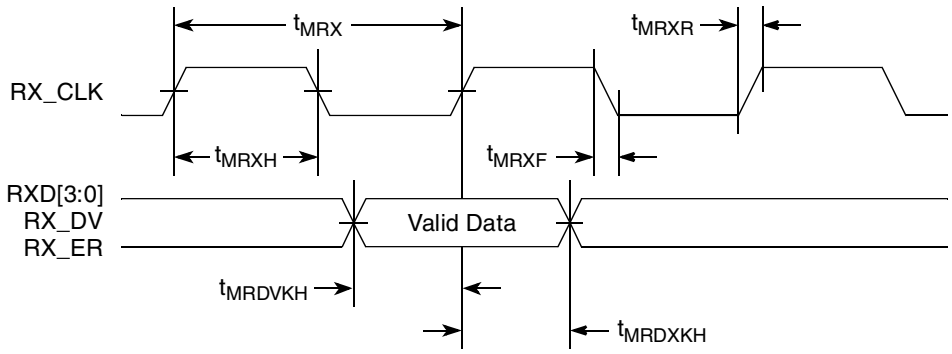


Figure 9. MII Receive AC Timing Diagram RMII AC Timing Specifications

8.2.1.3 RMII Transmit AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

Table 26 provides the RMII transmit AC timing specifications.

Table 26. RMII Transmit AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	-	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the RMII transmit AC timing diagram.

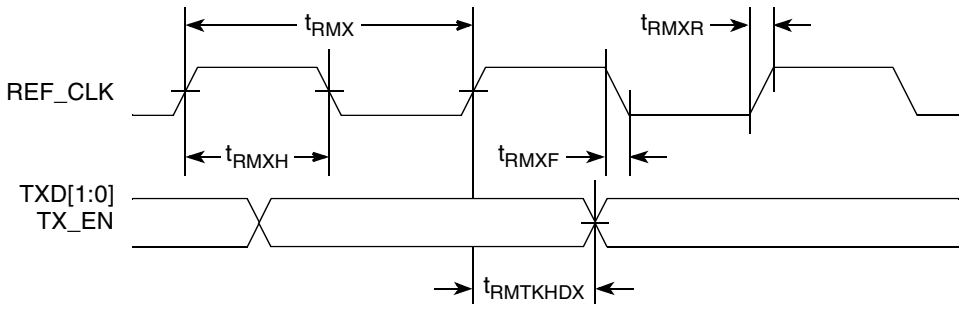


Figure 10. RMII Transmit AC Timing Diagram

8.2.1.4 RMII Receive AC Timing Specifications

Table 27 provides the RMII receive AC timing specifications.

Table 27. RMII Receive AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns

Table 27. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with NV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol [1]	Min	Typical	Max	Unit
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

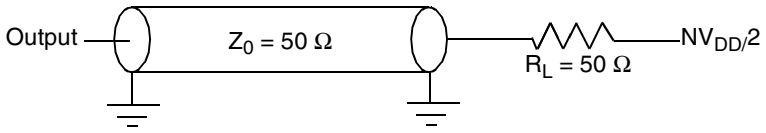


Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

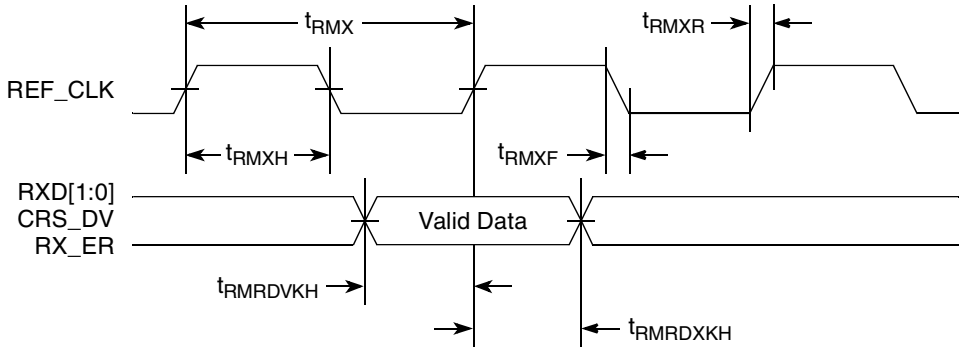


Figure 12. RMII Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

Table 28 presents the RGMII and RTBI AC timing specifications.

Table 28. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns

Table 28. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with LV_{DDA}/LV_{DDB} of 2.5 V ± 5%.

Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $LV_{DDA}/2$ or $LV_{DDB}/2$.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.

Figure 13 shows the RGMII and RTBI AC timing and multiplexing diagrams.

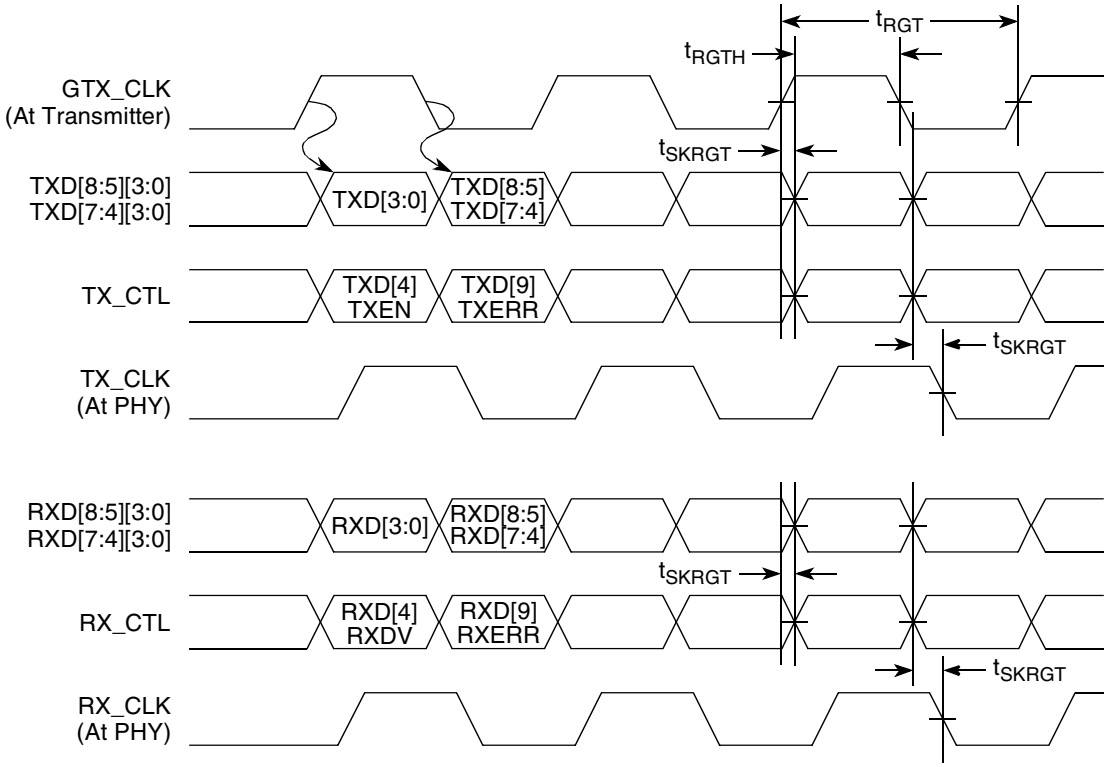


Figure 13. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, RMII, RGMII, SGMII, and RTBI are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5V or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 29 and Table 30.

Table 29. MII Management DC Electrical Characteristics When Powered at 2.5 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (2.5 V)	NV_{DDA}/NV_{DDB}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DDA} or NV_{DDB} = Min	2.00	NV_{DDA} + 0.3 or NV_{DDB} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NV_{DDA} or NV_{DDB} = Min	VSS – 0.3	0.40	V
Input high voltage	V_{IH}	—	NV_{DDA} or NV_{DDB} = Min	1.7	—	V
Input low voltage	V_{IL}	—	NV_{DDA} or NV_{DDB} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} [1] = NV_{DDA} or NV_{DDB}		—	10	µA
Input low current	I_{IL}	V_{IN} = NV_{DDA} or NV_{DDB}		–15	—	µA

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 30. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NV_{DDA}/NV_{DDB}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DDA} or NV_{DDB} = Min	2.10	NV_{DDA} + 0.3 or NV_{DDB} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DDA} or LV_{DDB} = Min	VSS	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	NV_{DDA} or NV_{DDB} = Max	V_{IN} [1] = 2.1 V	—	40	µA
Input low current	I_{IL}	NV_{DDA} or NV_{DDB} = Max	V_{IN} = 0.5 V	–600	—	µA

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 31 provides the MII management AC timing specifications.

Table 31. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} is 3.3 V ± 10% or 2.5 V ± 5%

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 14 shows the MII management AC timing diagram.

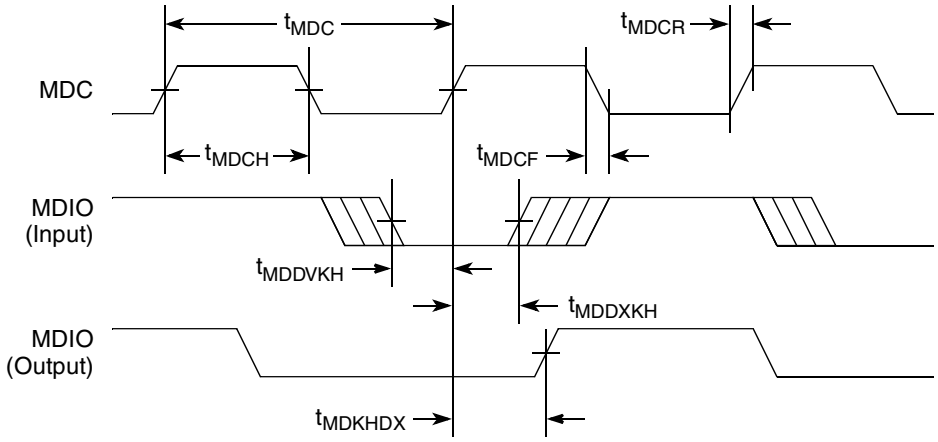


Figure 14. MII Management Interface Timing Diagram

8.3.3 SGMII DC Electrical Characteristics

The SGMII Solution in the MPC8313 is designed to be used in a 4-wire AC-Coupled SGMII link. Table 32 andTable 33describe the SGMII AC-Coupled DC electrical characteristics. Transmitter characteristics are measured at the transmitter outputs, SD_TX and SD_TX_B as depicted in Figure 15.

Table 32. DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage	V_{OH}		0.7*XPADVDD[1]	mV	Will not align to DC-coupled SGMII
Output low voltage	V_{OL}	0.3*XPADVDD		mV	
Output ringing	V_{RING}		10	%	
Output differential voltage	$\|V_{OD}\|$	(XPADVDD/2)/1.7	(XPADVDD/2)/1.3	mV	
Output offset voltage	V_{OS}	(XPADVDD/2) – 50 mV	(XPADVDD/2) + 50 mV	mV	Will not align to DC-coupled SGMII
Output impedance (single ended)	R_O	40	60	Ω	
Mismatch in a pair	ΔR_O		10	%	
Change in V_{OD} between “0” and “1”	$\Delta\|V_{OD}\|$		25	mV	
Change in V_{OS} between “0” and “1”	ΔV_{OS}		25	mV	
Output current on short to GND	I_{SA}, I_{SB}		40	mA	

[1] XPADVDDrefers to the SGMII transmitter output supply voltage.

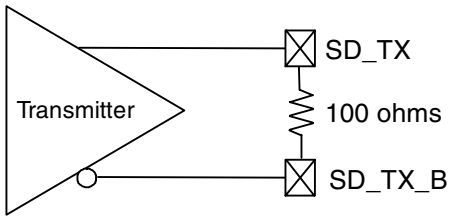


Figure 15. Transmitter Reference Circuit

Table 33. DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
DC input voltage range					Input must be externally ac-coupled.
Input differential voltage	Vrx_diffpp	100	1200	mV	Peak to peak input differential voltage.
Loss of signal threshold	VI_{os}	30	100	mV	
Input AC common mode voltage	Vcm_acpp		100	mV	Peak to peak ac common mode voltage.
Receiver differential input impedance	Zrx_diff	80	120	Ω	
Receiver common mode input impedance	Zrx_cm	20	35	Ω	
Common mode input voltage	Vcm	xcorevss	xcorevss	V	On-chip termination to xcorevss.

8.3.3.1 SGMII Transmit AC Timing Specifications

Table 34 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 34. SGMII Transmit AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Deterministic Jitter	J_D		0.17	UI p-p	
Total Jitter	J_T		0.35	UI p-p	
Unit Interval	U_I	800	800	ps	+/– 100ppm
V_{OD} fall time (80%–20%)	t_{fall}	50	120	ps	
V_{OD} rise time (20%–80%)	t_{rise}	50	120	ps	
Source synchronous clock is not supported					

8.3.3.2 SGMII Receive AC Timing Specifications

Table 35 provides the SGMII transmit AC timing targets. A source synchronous clock is not supported.

Table 35. SGMII Receiver AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Deterministic Jitter Tolerance	J_D	0.37		UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI p-p	Measured at receiver
Sinusoidal Jitter Tolerance	Jsin	0.1		UI p-p	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI p-p	Measured at receiver
Bit Error Ratio	BER		10^{-12}		
Unit Interval	UI	800	800	ps	+/– 100ppm

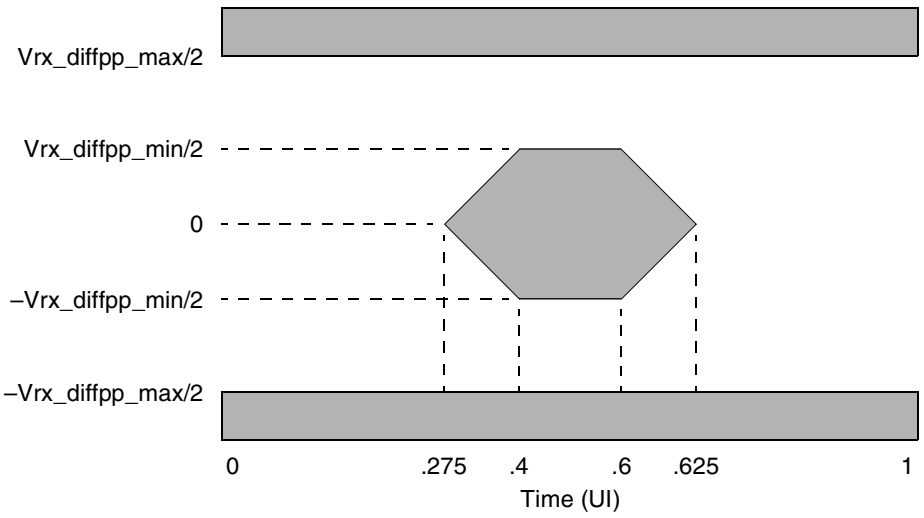


Figure 16. Receive Input Compliance Mask

9 USB

9.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB interface.

9.1.1 USB DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the USB interface.

Table 36. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	LV_{DDB}+ 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	LV_{DDB} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

9.1.2 USB AC Electrical Specifications

Table 37 describes the general timing parameters of the USB interface.

Table 37. USB General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	
Input setup to USB clock - all inputs	t_{USIVKH}	4	—	ns	
input hold to USB clock - all inputs	t_{USIXKH}	0	—	ns	
USB clock to output valid - all outputs	t_{USKHOV}	—	7	ns	
Output hold from USB clock - all outputs	t_{USKHOX}	2	—	ns	

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (USB) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes us timing (USB) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

Figure 17 and Figure 18 provide the AC test load and signals for the USB, respectively.

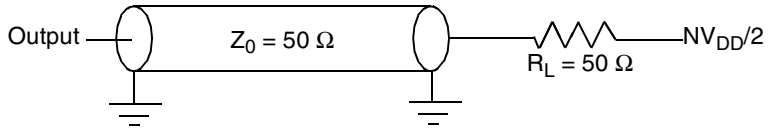


Figure 17. USB AC Test Load

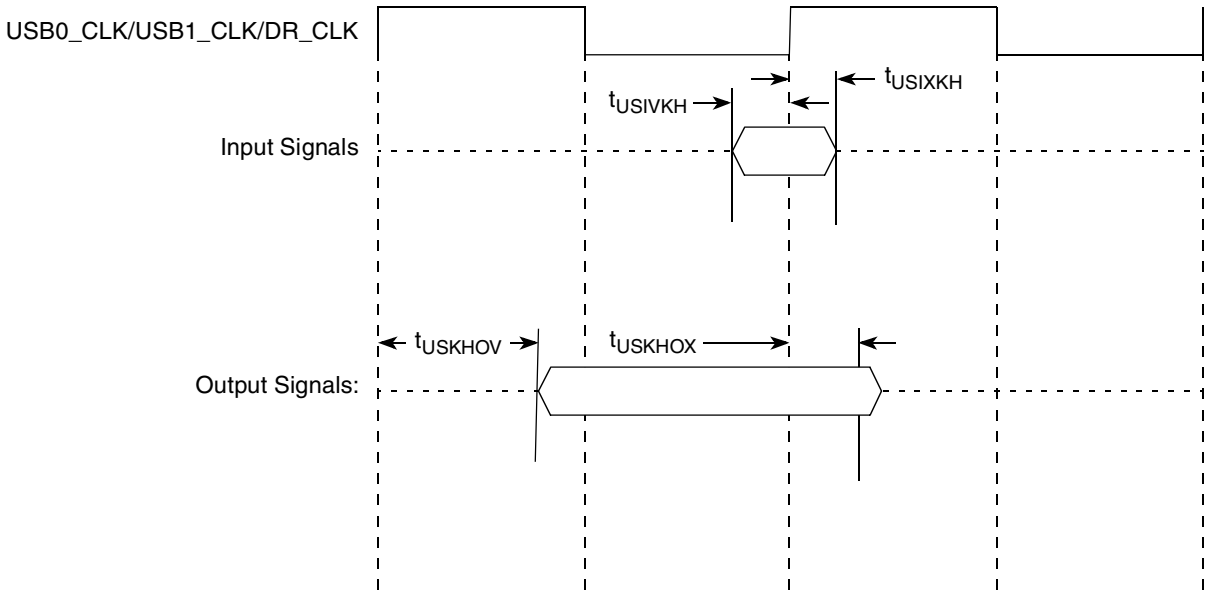


Figure 18. USB Signals

9.2 On-Chip USB PHY

See chapter 7 in the USB Specifications Rev 2.0

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface.

10.1 Local Bus DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the local bus interface.

Table 38. Local Bus DC Electrical Characteristics at 3.3 V

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	LV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±5	μA
High-level output voltage, (LV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	LV_{DD} – 0.2	—	V
Low-level output voltage, (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.2	V

10.2 Local Bus AC Electrical Specifications

Table 39 describes the general timing parameters of the local bus interface.

Table 39. Local Bus General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7

Table 39. Local Bus General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $NV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times NV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 19 provides the AC test load for the local bus.

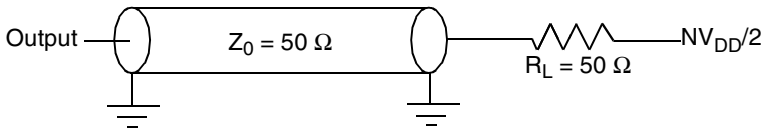


Figure 19. Local Bus AC Test Load

Figure 20 through Figure 22 show the local bus signals.

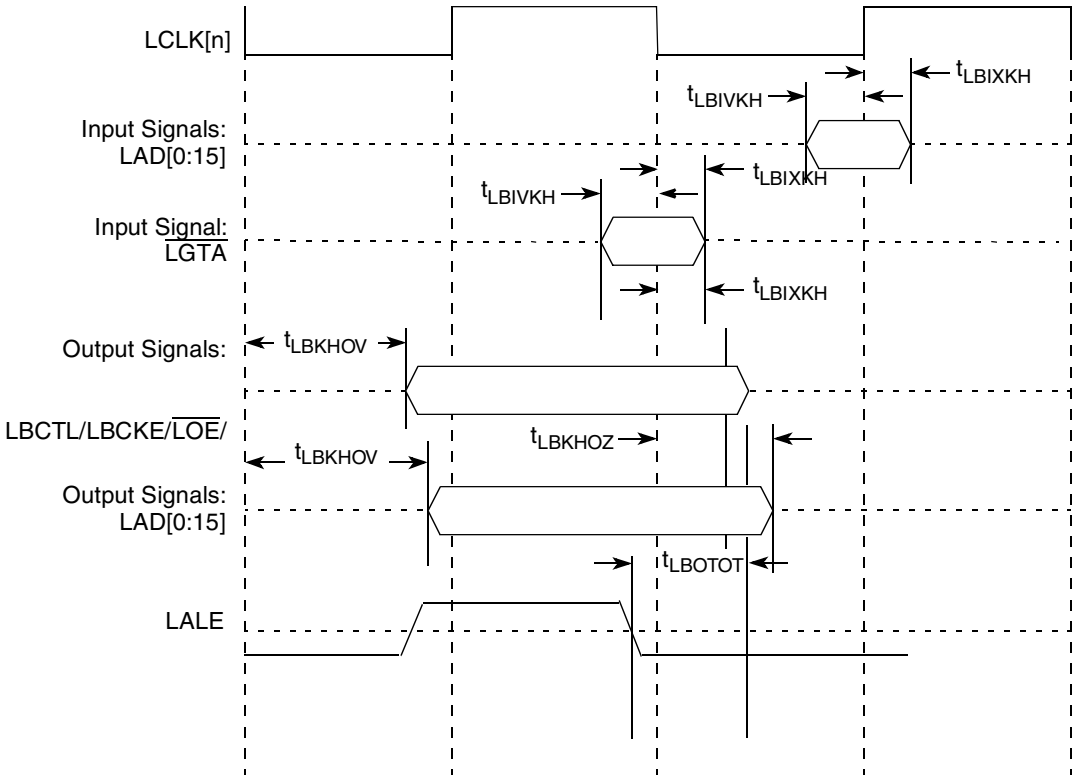


Figure 20. Local Bus Signals, Non-Special Signals Only

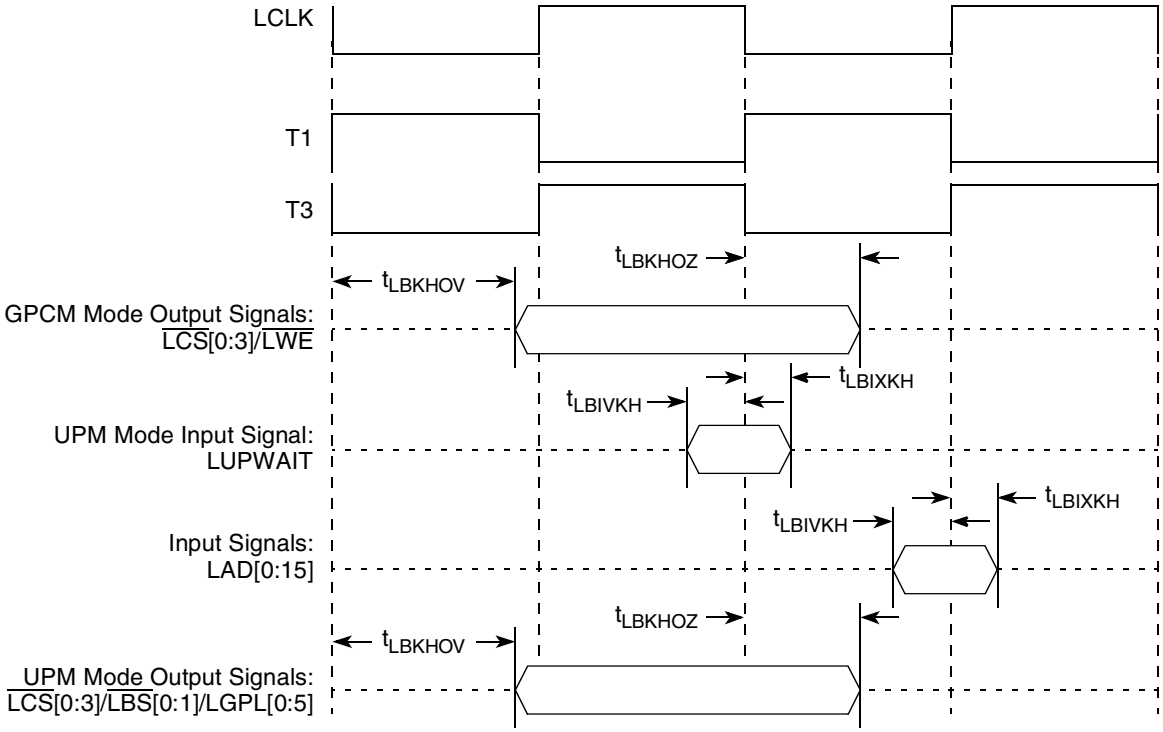


Figure 21. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2

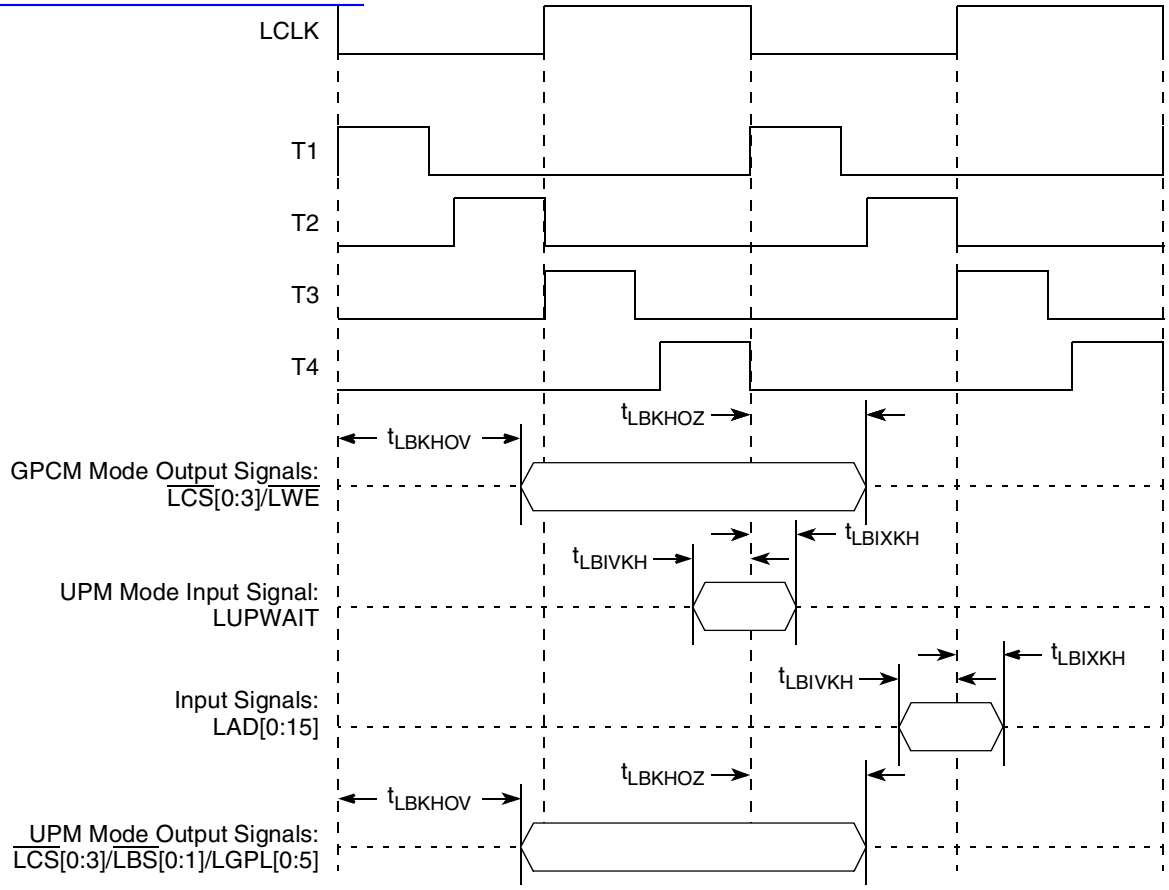


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface.

11.1 JTAG DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface.

Table 40. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface.

Table 41 provides the JTAG AC timing specifications as defined in Figure 24 through Figure 27.

Table 41. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5

Table 41. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 17). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 23 provides the AC test load for TDO and the boundary-scan outputs.

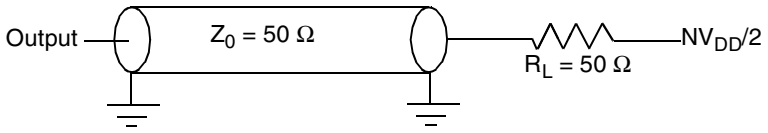


Figure 23. AC Test Load for the JTAG Interface

Figure 24 provides the JTAG clock input timing diagram.

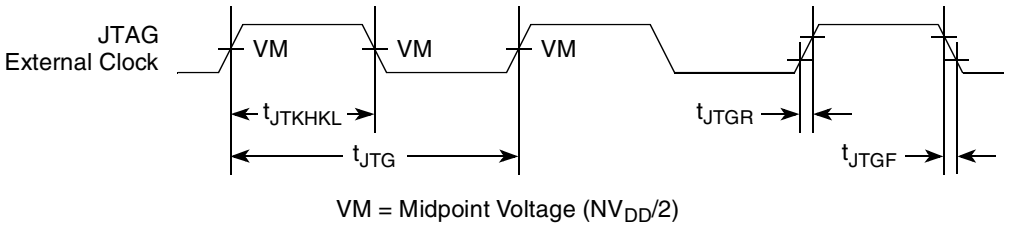


Figure 24. JTAG Clock Input Timing Diagram

Figure 25 provides the $\overline{\text{TRST}}$ timing diagram.

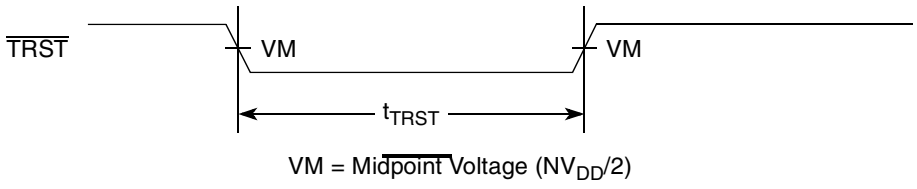


Figure 25. TRST Timing Diagram

Figure 26 provides the boundary-scan timing diagram.

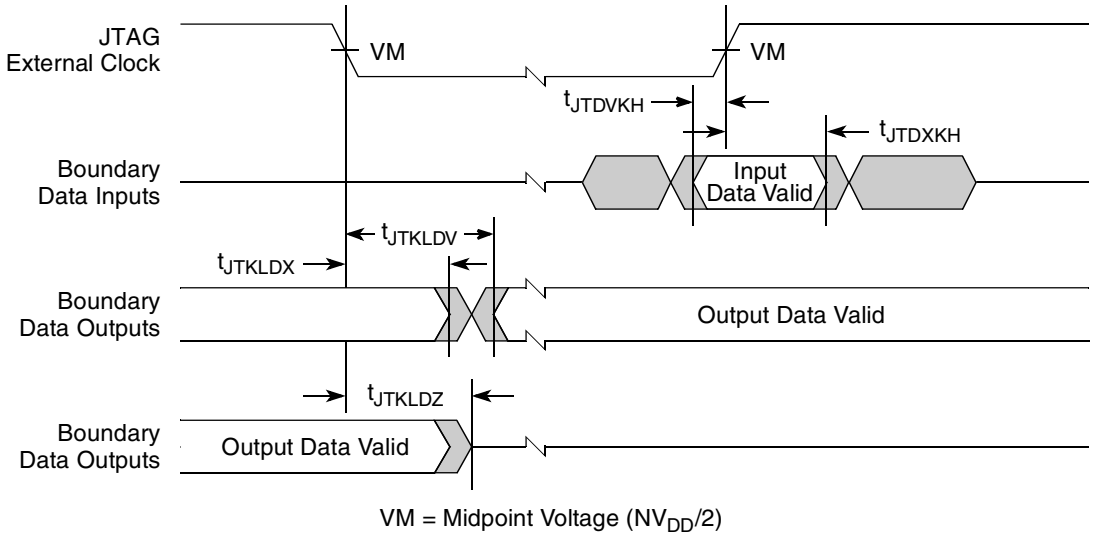


Figure 26. Boundary-Scan Timing Diagram

Figure 27 provides the test access port timing diagram.

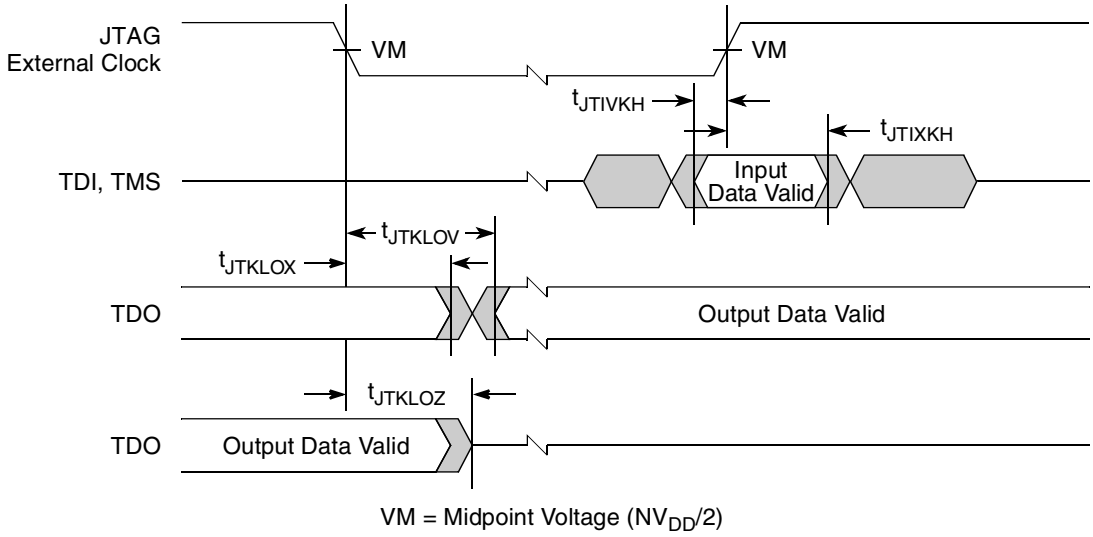


Figure 27. Test Access Port Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

12.1 I²C DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the I²C interface.

Table 42. I²C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times NV_{DD}$	$NV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times NV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times NV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	
Input current ($0 V \le V_{IN} \le NV_{DD}$)	I_{IN}	—	± 5	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8313E PowerQUICC II Pro Integrated Host Processor Reference Manual* for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if NV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 43 provides the AC timing parameters for the I²C interface.

Table 43. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 42).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns

Table 43. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 42).

Parameter	Symbol [1]	Min	Max	Unit
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0 [2]	— 0.9 [3]	µs
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_B [4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_B [4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × NV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × NV_{DD}	—	V

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 28 provides the AC test load for the I²C.

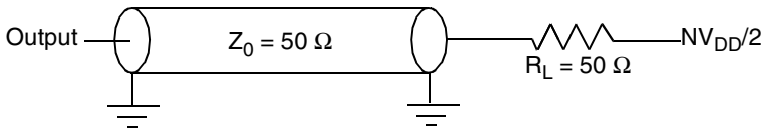


Figure 28. I²C AC Test Load

Figure 29 shows the AC timing diagram for the I^2C bus.

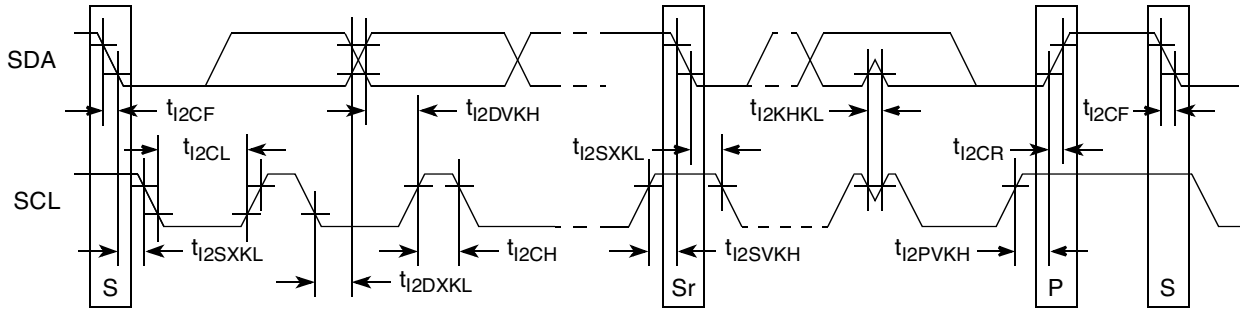


Figure 29. I^2C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus.

13.1 PCI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the PCI interface.

Table 44. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	0.5 x NV_{DD}	NV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.5	0.3 x NV_{DD}	V
High-level output voltage	V_{OH}	NV_{DD} = min, I_{OH} = –100 µA	0.9 x NV_{DD}	—	V
Low-level output voltage	V_{OL}	NV_{DD} = min, I_{OL} = 100 µA	—	0.1x NV_{DD}	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NV_{DD}	—	± 5	µA

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8313E is configured as a host or agent device.

Table 45 shows the PCI AC timing specifications at 66 MHz.

Table 45. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from Clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to Clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Table 46 shows the PCI AC Timing Specifications at 33 MHz.

Table 46. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from Clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to Clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from Clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 30 provides the AC test load for PCI.

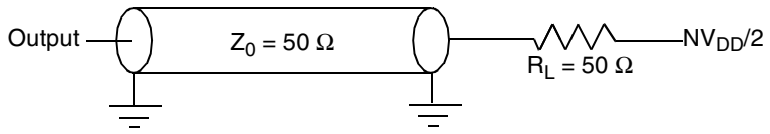


Figure 30. PCI AC Test Load

Figure 31 shows the PCI input AC timing conditions.

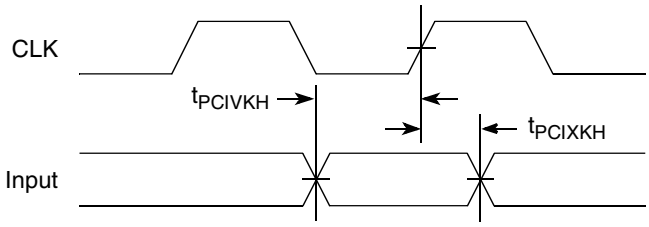


Figure 31. PCI Input AC Timing Measurement Conditions

Figure 32 shows the PCI output AC timing conditions.

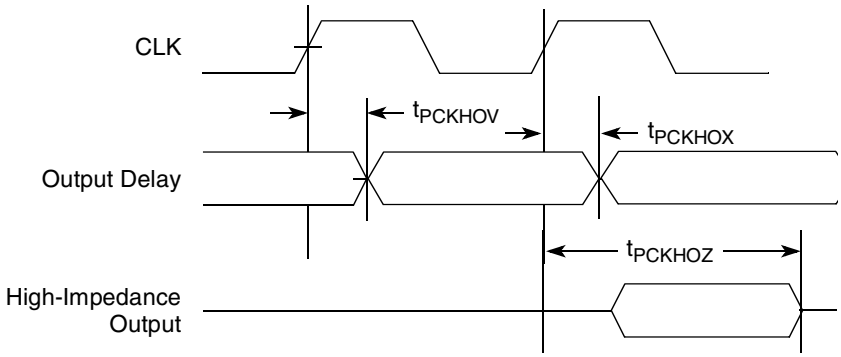


Figure 32. PCI Output AC Timing Measurement Condition

14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timers DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the MPC8313E timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 47. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	± 5	μA

14.2 Timers AC Timing Specifications

Table 48 provides the Timers input and output AC timing specifications.

Table 48. Timers Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

Figure 33 provides the AC test load for the Timers.

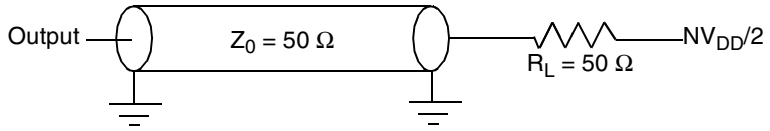


Figure 33. Timers AC Test Load

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the GPIO.

Table 49. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NV_{DD}	—	± 5	μA

15.2 GPIO AC Timing Specifications

Table 50 provides the GPIO input and output AC timing specifications.

Table 50. GPIO Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 34 provides the AC test load for the GPIO.

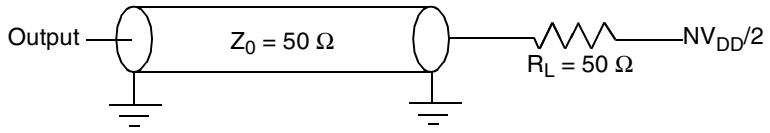


Figure 34. GPIO AC Test Load

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the external interrupt pins.

Table 51. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	μA
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

16.2 IPIC AC Timing Specifications

Table 52 provides the IPIC input and output AC timing specifications.

Table 52. IPIC Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

17 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8313E

17.1 SPI DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the MPC8313E SPI.

Table 53. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	± 5	μA

17.2 SPI AC Timing Specifications

Table 54 and provide the SPI input and output AC timing specifications.

Table 54. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6		ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of SYS_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 35 provides the AC test load for the SPI.

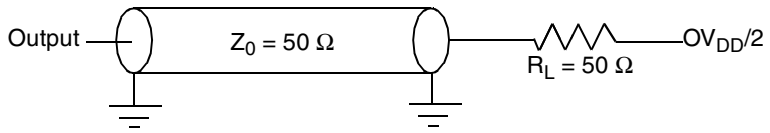
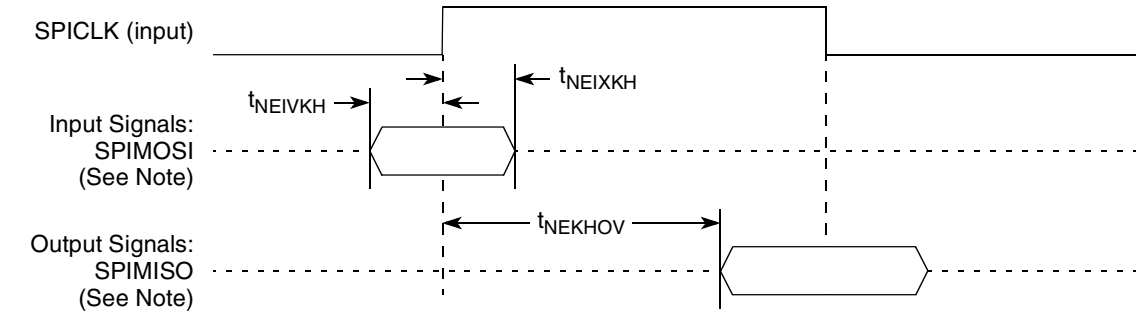


Figure 35. SPI AC Test Load

Figure 36 through Figure 37 represent the AC timing from Table 54. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

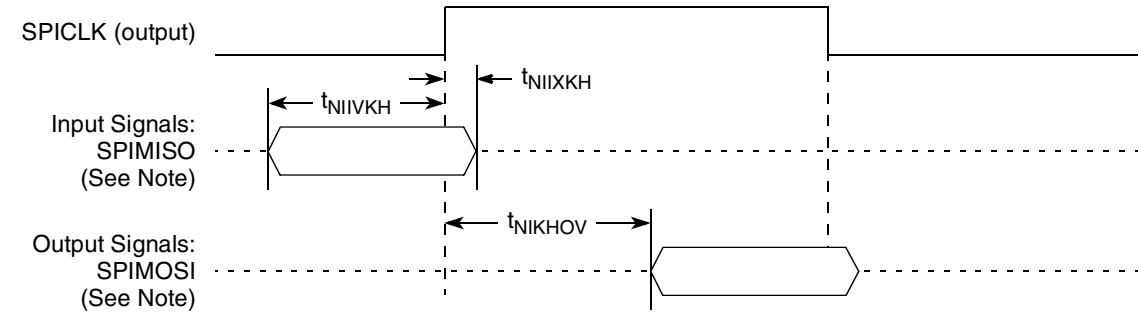
Figure 36 shows the SPI timing in Slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 36. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 37 shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 37. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8313E is available in a thermally enhanced plastic ball grid array (TEPBGAII), see Section 18.1, "Package Parameters for the MPC8313E TEPBGAII," and Section 18.2, "Mechanical Dimensions of the MPC8313E TEPBGAII," for information on the TEPBGAII.

18.1 Package Parameters for the MPC8313E TEPBGAII

The package parameters are as provided in the following list. The package type is 27 mm × 27 mm, 516 TEPBGAII.

Package outline	27 mm × 27 mm
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	95.5 Sn/0.5 Cu/4Ag (VR *package)*
Ball diameter (typical)	0.6 mm

18.2 Mechanical Dimensions of the MPC8313E TEPBGAII

Figure 38 shows the mechanical dimensions and bottom surface nomenclature of the 516-TEPBGAII package.

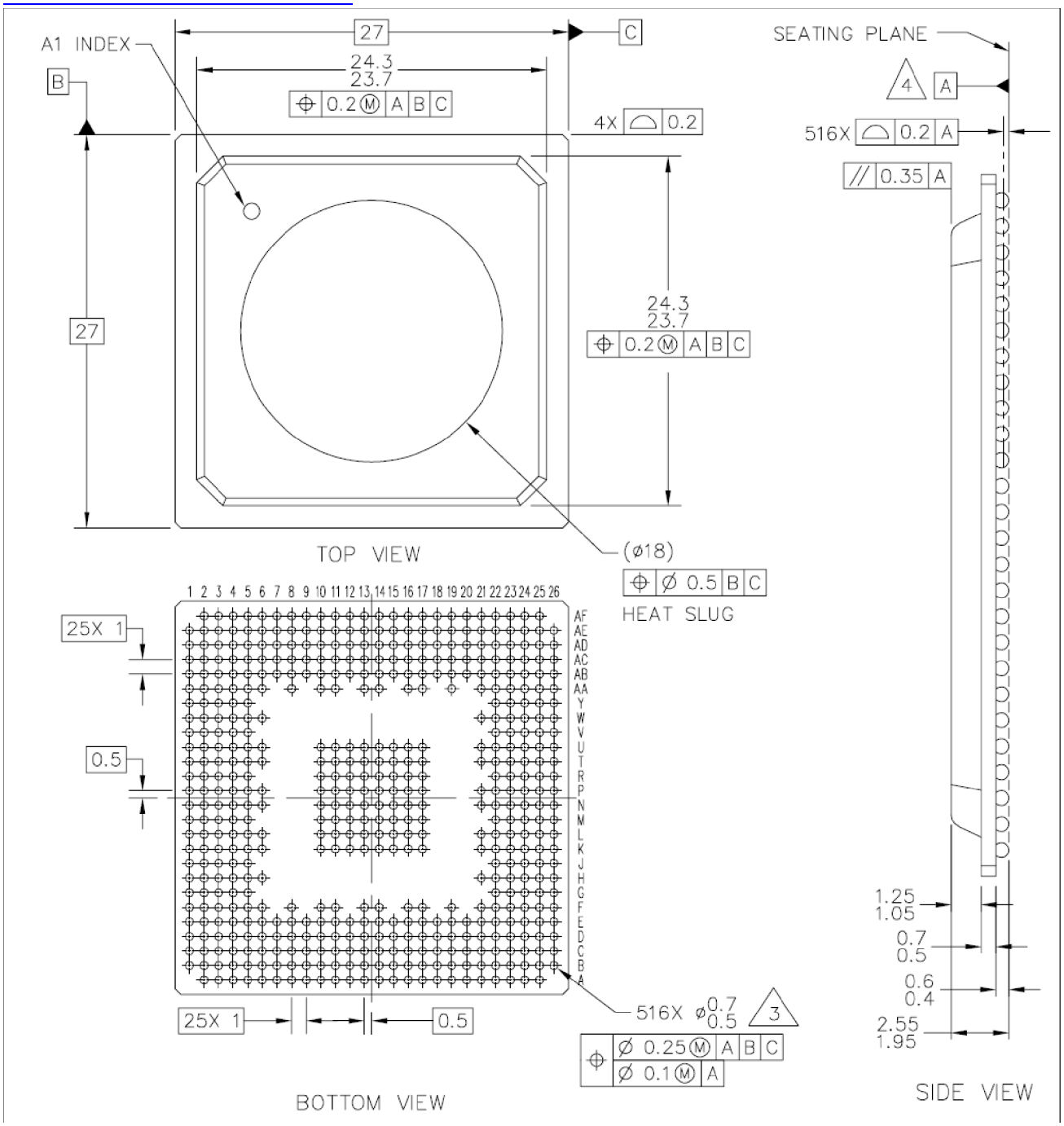


Figure 38. Mechanical Dimension and Bottom Surface Nomenclature of the MPC8313E TEPBGAII

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Package code 5368 is to account for PGE and the built–in heat spreader.

18.3 Pinout Listings

Table 55 provides the pin-out listing for the MPC8313E, TEPBGAII package.

Table 55. MPC8313E TEPBGAII Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ[0]	A8	IO	GV_{DD}	
MEMC_MDQ[1]	A9	IO	GV_{DD}	
MEMC_MDQ[2]	C10	IO	GV_{DD}	
MEMC_MDQ[3]	C9	IO	GV_{DD}	
MEMC_MDQ[4]	E9	IO	GV_{DD}	
MEMC_MDQ[5]	E11	IO	GV_{DD}	
MEMC_MDQ[6]	E10	IO	GV_{DD}	
MEMC_MDQ[7]	C8	IO	GV_{DD}	
MEMC_MDQ[8]	E8	IO	GV_{DD}	
MEMC_MDQ[9]	A6	IO	GV_{DD}	
MEMC_MDQ[10]	B6	IO	GV_{DD}	
MEMC_MDQ[11]	C6	IO	GV_{DD}	
MEMC_MDQ[12]	C7	IO	GV_{DD}	
MEMC_MDQ[13]	D7	IO	GV_{DD}	
MEMC_MDQ[14]	D6	IO	GV_{DD}	
MEMC_MDQ[15]	A5	IO	GV_{DD}	
MEMC_MDQ[16]	A19	IO	GV_{DD}	
MEMC_MDQ[17]	D18	IO	GV_{DD}	
MEMC_MDQ[18]	A17	IO	GV_{DD}	
MEMC_MDQ[19]	E17	IO	GV_{DD}	
MEMC_MDQ[20]	E16	IO	GV_{DD}	
MEMC_MDQ[21]	C18	IO	GV_{DD}	
MEMC_MDQ[22]	D19	IO	GV_{DD}	
MEMC_MDQ[23]	C19	IO	GV_{DD}	
MEMC_MDQ[24]	E19	IO	GV_{DD}	
MEMC_MDQ[25]	A22	IO	GV_{DD}	
MEMC_MDQ[26]	C21	IO	GV_{DD}	
MEMC_MDQ[27]	C20	IO	GV_{DD}	
MEMC_MDQ[28]	A21	IO	GV_{DD}	
MEMC_MDQ[29]	A20	IO	GV_{DD}	

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MDQ[30]	C22	IO	GV_{DD}	
MEMC_MDQ[31]	B22	IO	GV_{DD}	
MEMC_MDM0	B7	O	GV_{DD}	
MEMC_MDM1	E6	O	GV_{DD}	
MEMC_MDM2	E18	O	GV_{DD}	
MEMC_MDM3	E20	O	GV_{DD}	
MEMC_MDQS[0]	A7	IO	GV_{DD}	
MEMC_MDQS[1]	E7	IO	GV_{DD}	
MEMC_MDQS[2]	B19	IO	GV_{DD}	
MEMC_MDQS[3]	A23	IO	GV_{DD}	
MEMC_MBA[0]	D15	O	GV_{DD}	
MEMC_MBA[1]	A18	O	GV_{DD}	
MEMC_MBA[2]	A15	O	GV_{DD}	
MEMC_MA0	E12	O	GV_{DD}	
MEMC_MA1	D11	O	GV_{DD}	
MEMC_MA2	B11	O	GV_{DD}	
MEMC_MA3	A11	O	GV_{DD}	
MEMC_MA4	A12	O	GV_{DD}	
MEMC_MA5	E13	O	GV_{DD}	
MEMC_MA6	C12	O	GV_{DD}	
MEMC_MA7	E14	O	GV_{DD}	
MEMC_MA8	B15	O	GV_{DD}	
MEMC_MA9	C17	O	GV_{DD}	
MEMC_MA10	C13	O	GV_{DD}	
MEMC_MA11	A16	O	GV_{DD}	
MEMC_MA12	C15	O	GV_{DD}	
MEMC_MA13	C16	O	GV_{DD}	
MEMC_MA14	E15	O	GV_{DD}	
$\overline{\text{MEMC\_MWE}}$	B18	O	GV_{DD}	
$\overline{\text{MEMC\_MRAS}}$	C11	O	GV_{DD}	
$\overline{\text{MEMC\_MCAS}}$	B10	O	GV_{DD}	
$\overline{\text{MEMC\_MCS}}$[0]	D10	O	GV_{DD}	
$\overline{\text{MEMC\_MCS}}$[1]	A10	O	GV_{DD}	
MEMC_MCKE	B14	O	GV_{DD}	3

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCK	A13	O	GV_{DD}	
$\overline{\text{MEMC\_MCK}}$	A14	O	GV_{DD}	
MEMC_MODT[0]	B23	O	GV_{DD}	
MEMC_MODT[1]	C23	O	GV_{DD}	
Local Bus Controller Interface				
LAD0	K25	IO	LV_{DD}	
LAD1	K24	IO	LV_{DD}	
LAD2	K23	IO	LV_{DD}	
LAD3	K22	IO	LV_{DD}	
LAD4	J25	IO	LV_{DD}	
LAD5	J24	IO	LV_{DD}	
LAD6	J23	IO	LV_{DD}	
LAD7	J22	IO	LV_{DD}	
LAD8	H24	IO	LV_{DD}	
LAD9	F26	IO	LV_{DD}	
LAD10	G24	IO	LV_{DD}	
LAD11	F25	IO	LV_{DD}	
LAD12	E25	IO	LV_{DD}	
LAD13	F24	IO	LV_{DD}	
LAD14	G22	IO	LV_{DD}	
LAD15	F23	IO	LV_{DD}	
LA16	AC25	O	LV_{DD}	
LA17	AC26	O	LV_{DD}	
LA18	AB22	O	LV_{DD}	
LA19	AB23	O	LV_{DD}	
LA20	AB24	O	LV_{DD}	
LA21	AB25	O	LV_{DD}	
LA22	AB26	O	LV_{DD}	
LA23	E22	O	LV_{DD}	
LA24	E23	O	LV_{DD}	
LA25	D22	O	LV_{DD}	
$\overline{\text{LCS}}$[0]	D23	O	LV_{DD}	
$\overline{\text{LCS}}$[1]	J26	O	LV_{DD}	
$\overline{\text{LCS}}$[2]	F22	O	LV_{DD}	

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS}}$[3]	D26	O	LV_{DD}	
$\overline{\text{LWE}}$[0]	E24	O	LV_{DD}	
$\overline{\text{LWE}}$[1]	H26	O	LV_{DD}	
LBCTL	L22	O	LV_{DD}	
LALE/M1LALE/M2LALE	E26	O	LV_{DD}	
LGPL0	AA23	O	LV_{DD}	
LGPL1	AA24	O	LV_{DD}	
LGPL2	AA25	O	LV_{DD}	
LGPL3	AA26	O	LV_{DD}	
LGPL4	Y22	IO	LV_{DD}	
LGPL5	E21	O	LV_{DD}	
LCLK0	H22	O	LV_{DD}	
LCLK1	G26	O	LV_{DD}	
LA0/GPIO[0]	AC24	IO	LV_{DD}	
LA1/GPIO[1]	Y24	IO	LV_{DD}	
LA2/GPIO[2]	Y26	IO	LV_{DD}	
LA3/GPIO[3]	W22	IO	LV_{DD}	
LA4/GPIO[4]	W24	IO	LV_{DD}	
LA5/GPIO[5]	W26	IO	LV_{DD}	
LA6/GPIO[6]	V22	IO	LV_{DD}	
LA7/GPIO[7]	V23	IO	LV_{DD}	
LA8/GPIO[13]	V24	IO	LV_{DD}	
LA9/GPIO[14]	V25	IO	LV_{DD}	
LA10	V26	O	LV_{DD}	
LA11	U22	O	LV_{DD}	
LA12	AD24	O	LV_{DD}	
LA13	L25	O	LV_{DD}	
LA14	L24	O	LV_{DD}	
LA15	K26	O	LV_{DD}	
DUART				
UART_SOUT1/MSRCID0	N2	O	NV_{DD}	
UART_SIN1/MSRCID1	M5	IO	NV_{DD}	
$\overline{\text{UART\_CTS}}$[1]/GPIO[8]/MSRCID2	M1	IO	NV_{DD}	
$\overline{\text{UART\_RTS}}$[1]/GPIO[9]/MSRCID3	K1	IO	NV_{DD}	

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
UART_SOUT2/MSRCID4	M3	O	NV_{DD}	
UART_SIN2/MDVAL	L1	IO	NV_{DD}	
$\overline{\text{UART\_CTS}}$[2]	L5	IO	NV_{DD}	
$\overline{\text{UART\_RTS}}$[2]	L3	IO	NV_{DD}	
I^2C interface				
IIC1_SDA/$\overline{\text{CKSTOP\_OUT}}$	J4	IO	NV_{DD}	2
IIC1_SCL/$\overline{\text{CKSTOP\_IN}}$	J2	IO	NV_{DD}	2
IIC2_SDA/PMC_PWR_OK/GPIO[10]	J3	IO	NV_{DD}	2
IIC2_SCL/GPIO[11]	H5	IO	NV_{DD}	2
Interrupts				
$\overline{\text{MCP\_OUT}}$	G5	O	NV_{DD}	2
$\overline{\text{IRQ}}$[0]/$\overline{\text{MCP\_IN}}$	K5	I	NV_{DD}	
$\overline{\text{IRQ}}$[1]	K4	I	NV_{DD}	
$\overline{\text{IRQ}}$[2]	K2	I	NV_{DD}	
$\overline{\text{IRQ}}$[3] /$\overline{\text{CKSTOP\_OUT}}$	K3	IO	NV_{DD}	
$\overline{\text{IRQ}}$[4]/ $\overline{\text{CKSTOP\_IN}}$/GPIO[12]	J1	IO	NV_{DD}	
Configuration				
$\overline{\text{CFG\_CLKIN\_DIV}}$	D5	I	NV_{DD}	
EXT_PWR_CTRL	J5	O	NV_{DD}	
CFG_LBIU_MUX_EN	R24	I	NV_{DD}	
JTAG				
TCK	E1	I	NV_{DD}	
TDI	E2	I	NV_{DD}	4
TDO	E3	O	NV_{DD}	3
TMS	E4	I	NV_{DD}	4
$\overline{\text{TRST}}$	E5	I	NV_{DD}	4
TEST				
TEST_MODE	F4	I	NV_{DD}	6
DEBUG				
$\overline{\text{QUIESCE}}$	F5	O	NV_{DD}	
System Control				
$\overline{\text{HRESET}}$	F2	IO	NV_{DD}	1

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{PORESET}}$	F3	I	NV_{DD}	
$\overline{\text{SRESET}}$	F1	I	NV_{DD}	
Clocks				
SYS_CR_CLK_IN	U26	I	NV_{DD}	
SYS_CR_CLK_OUT	U25	O	NV_{DD}	
SYS_CLK_IN	U23	I	NV_{DD}	
USB_CR_CLK_IN	T26	I	NV_{DD}	
USB_CR_CLK_OUT	R26	O	NV_{DD}	
USB_CLK_IN	T22	I	NV_{DD}	
PCI_SYNC_OUT	U24	O	NV_{DD}	3
RTC_PIT_CLOCK	R22	I	NV_{DD}	
PCI_SYNC_IN	T24	I	NV_{DD}	
MISC				
AV_{DD1}	F14	I	Double with Pad	
AV_{DD2}	P21	I	Double with Pad	
PCI				
$\overline{\text{PCI\_INTA}}$	AF7	O	NV_{DD}	
$\overline{\text{PCI\_RESET\_OUT}}$	AB11	O	NV_{DD}	
PCI_AD[0]	AB20	IO	NV_{DD}	
PCI_AD[1]	AF23	IO	NV_{DD}	
PCI_AD[2]	AF22	IO	NV_{DD}	
PCI_AD[3]	AB19	IO	NV_{DD}	
PCI_AD[4]	AE22	IO	NV_{DD}	
PCI_AD[5]	AF21	IO	NV_{DD}	
PCI_AD[6]	AD19	IO	NV_{DD}	
PCI_AD[7]	AD20	IO	NV_{DD}	
PCI_AD[8]	AC18	IO	NV_{DD}	
PCI_AD[9]	AD18	IO	NV_{DD}	
PCI_AD[10]	AB18	IO	NV_{DD}	
PCI_AD[11]	AE19	IO	NV_{DD}	
PCI_AD[12]	AB17	IO	NV_{DD}	
PCI_AD[13]	AE18	IO	NV_{DD}	

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_AD[14]	AD17	IO	NV_{DD}	
PCI_AD[15]	AF19	IO	NV_{DD}	
PCI_AD[16]	AB14	IO	NV_{DD}	
PCI_AD[17]	AF15	IO	NV_{DD}	
PCI_AD[18]	AD14	IO	NV_{DD}	
PCI_AD[19]	AE14	IO	NV_{DD}	
PCI_AD[20]	AF12	IO	NV_{DD}	
PCI_AD[21]	AE11	IO	NV_{DD}	
PCI_AD[22]	AD12	IO	NV_{DD}	
PCI_AD[23]	AB13	IO	NV_{DD}	
PCI_AD[24]	AF9	IO	NV_{DD}	
PCI_AD[25]	AD11	IO	NV_{DD}	
PCI_AD[26]	AE10	IO	NV_{DD}	
PCI_AD[27]	AB12	IO	NV_{DD}	
PCI_AD[28]	AD10	IO	NV_{DD}	
PCI_AD[29]	AC10	IO	NV_{DD}	
PCI_AD[30]	AF10	IO	NV_{DD}	
PCI_AD[31]	AF8	IO	NV_{DD}	
PCI_C/$\overline{BE}$[0]	AC19	IO	NV_{DD}	
PCI_C/$\overline{BE}$[1]	AB15	IO	NV_{DD}	
PCI_C/$\overline{BE}$[2]	AF14	IO	NV_{DD}	
PCI_C/$\overline{BE}$[3]	AF11	IO	NV_{DD}	
PCI_PAR	AD16	IO	NV_{DD}	
$\overline{PCI\_FRAME}$	AF16	IO	NV_{DD}	5
$\overline{PCI\_TRDY}$	AD13	IO	NV_{DD}	5
$\overline{PCI\_IRDY}$	AC15	IO	NV_{DD}	5
$\overline{PCI\_STOP}$	AF13	IO	NV_{DD}	5
$\overline{PCI\_DEVSEL}$	AC14	IO	NV_{DD}	5
PCI_IDSEL	AF20	I	NV_{DD}	
$\overline{PCI\_SERR}$	AE15	IO	NV_{DD}	5
$\overline{PCI\_PERR}$	AD15	IO	NV_{DD}	5
$\overline{PCI\_REQ0}$	AB10	IO	NV_{DD}	
$\overline{PCI\_REQ1}$/CPCI_HS_ES	AD9	I	NV_{DD}	
$\overline{PCI\_REQ2}$	AD8	I	NV_{DD}	

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{PCI\_GNT0}}$	AC11	IO	NV_{DD}	
$\overline{\text{PCI\_GNT1}}$/CPCI_HS_LED	AE7	O	NV_{DD}	
$\overline{\text{PCI\_GNT2}}$/CPCI_HS_ENUM	AD7	O	NV_{DD}	
M66EN	AD21	I	NV_{DD}	
PCI_CLK0	AF17	O	NV_{DD}	
PCI_CLK1	AB16	O	NV_{DD}	
PCI_CLK2	AF18	O	NV_{DD}	
$\overline{\text{PCI\_PME}}$	AD22	IO	NV_{DD}	
ETSEC1/_USBULPI				
TSEC1_COL/USBDR_TXDRXD0	AD2	IO	LV_{DDB}	
TSEC1_CRS/USBDR_TXDRXD1	AC3	IO	LV_{DDB}	
TSEC1_GTX_CLK/USBDR_TXDRXD2	AF3	IO	LV_{DDB}	3
TSEC1_RX_CLK/USBDR_TXDRXD3	AE3	IO	LV_{DDB}	
TSCE1_RX_DV/USBDR_TXDRXD4	AD3	IO	LV_{DDB}	
TSEC1_RXD[3]/USBDR_TXDRXD5	AC6	IO	LV_{DDB}	
TSEC1_RXD[2]/USBDR_TXDRXD6	AF4	IO	LV_{DDB}	
TSEC1_RXD[1]/USBDR_TXDRXD7	AB6	IO	LV_{DDB}	
TSEC1_RXD[0]/USBDR_NXT/TSEC_1588_TRIG1	AB5	I	LV_{DDB}	
TSEC1_RX_ER/USBDR_DIR/TESC_1588_TRIG2	AD4	I	LV_{DDB}	
TSEC1_TX_CLK/USBDR_CLK/TSEC_1588_CLK	AF5	I	LV_{DDB}	
TSEC1_TXD[3]/TSEC_1588_GCLK	AE6	O	LV_{DDB}	
TSEC1_TXD[2]/TSEC_1588_PP1	AC7	O	LV_{DDB}	
TSEC1_TXD[1]/TSEC_1588_PP2	AD6	O	LV_{DDB}	
TSEC1_TXD[0]/USBDR_STP/TSEC_1588_PP3	AD5	O	LV_{DDB}	
TSEC1_TX_EN/TSEC_1588_ALARM1	AB7	O	LV_{DDB}	
TSEC1_TX_ER/TSEC_1588_ALARM2	AB8	O	LV_{DDB}	
TSEC1_GTX_CLK125	AE1	I	LV_{DDB}	
TSEC1_MDC	AF6	O	NV_{DD}	
TSEC1_MDIO	AB9	IO	NV_{DD}	2
ETSEC2				
TSEC2_COL/GTM1_TIN4/GTM2_TIN3/GPIO[15]	AB4	IO	LV_{DDA}	
TSEC2_CRS/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$/GPIO[16]	AB3	IO	LV_{DDA}	
TSEC2_GTX_CLK/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$/GPIO[17]	AC1	IO	LV_{DDA}	
TSEC2_RX_CLK/GTM1_TIN2/GTM2_TIN1/GPIO[18]	AC2	IO	LV_{DDA}	

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSCE2_RX_DV/GTM1_TGATE2/GTM2_TGATE1/GPIO[19]	AA3	IO	LV_{DDA}	
TSEC2_RXD[3]/GPIO[20]	Y5	IO	LV_{DDA}	
TSEC2_RXD[2]/GPIO[21]	AA4	IO	LV_{DDA}	
TSEC2_RXD[1]/GPIO[22]	AB2	IO	LV_{DDA}	
TSEC2_RXD[0]/GPIO[23]	AA5	IO	LV_{DDA}	
TSEC2_RX_ER/GTM1_TOUT2/GTM2_TOUT1/GPIO[24]	AA2	IO	LV_{DDA}	
TSEC2_TX_CLK/GPIO[25]	AB1	IO	LV_{DDA}	
TSEC2_TXD[3]/CFG_RESET_SOURCE[0]	W3	IO	LV_{DDA}	
TSEC2_TXD[2]/CFG_RESET_SOURCE[1]	Y1	IO	LV_{DDA}	
TSEC2_TXD[1]/CFG_RESET_SOURCE[2]	W5	IO	LV_{DDA}	
TSEC2_TXD[0]/CFG_RESET_SOURCE[3]	Y3	IO	LV_{DDA}	
TSEC2_TX_EN/GPIO[26]	AA1	IO	LV_{DDA}	
TSEC2_TX_ER/GPIO[27]	W1	IO	LV_{DDA}	
SGMII PHY				
TXA	U3	O		
$\overline{\text{TXA}}$	V3	O		
RXA	U1	I		
$\overline{\text{RXA}}$	V1	I		
TXB	P4	O		
$\overline{\text{TXB}}$	N4	O		
RXB	R1	I		
$\overline{\text{RXB}}$	P1	I		
SD_IMP_CAL_RX	V5	I		
$\overline{\text{SD\_REF\_CLK}}$	T5	I		
SD_REF_CLK	T4	I		
SD_PLL_TPD	T2	O		
SD_IMP_CAL_TX	N5	I		
SDAVDD	R5	IO		
SD_PLL_TPA_ANA	R4	O		
SDAVSS	R3	IO		
USB PHY				
USB_DP	P26	IO		
USB_DM	N26	IO		
USB_VBUS	P24	IO		

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
USB_TPA	L26	IO		
USB_RBIAS	M24	IO		
USB_PLL_PWR3	M26	IO		
USB_PLL_GND	N24	IO		
USB_PLL_PWR1	N25	IO		
USB_VSSA_BIAS	M25	IO		
USB_VDDA_BIAS	M22	IO		
USB_VSSA	N22	IO		
USB_VDDA	P22	IO		
GTM/USB				
USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2	AD23	IO	NV_{DD}	
USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	AE23	IO	NV_{DD}	
USBDR_PCTL0/$\overline{\text{GTM1\_TOUT1}}$	AC22	O	NV_{DD}	
USBDR_PCTL1	AB21	O	NV_{DD}	
SPI				
SPIMOSI/GTM1_TIN3/GTM2_TIN4/GPIO[28]	H1	IO	NV_{DD}	
SPIMISO/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$/GPIO[29]/LDVAL	H3	IO	NV_{DD}	
SPICLK/$\overline{\text{GTM1\_TOUT3}}$/GPIO[30]	G1	IO	NV_{DD}	
SPISEL/GPIO[31]	G3	IO	NV_{DD}	
Power and Ground Supplies				
GV_{DD}	A2,A3,A4,A24,A25,B3, B4,B5,B12,B13,B20, B21,B24,B25,B26,D1, D2,D8,D9,D16,D17			
LV_{DD}	D24,D25,G23,H23,R23, T23,W25,Y25, AA22,AC23			
LV_{DDA}	W2,Y2			
LV_{DDB}	AC8,AC9,AE4,AE5			
MV_{REF}	C14,D14			
NV_{DD}	G4,H4,L2,M2,AC16, AC17,AD25,AD26,AE12, AE13,AE20,AE21,AE24, AE25,AE26,AF24, AF25			

Table 55. MPC8313E TEPBGAII Pinout Listing (continued)

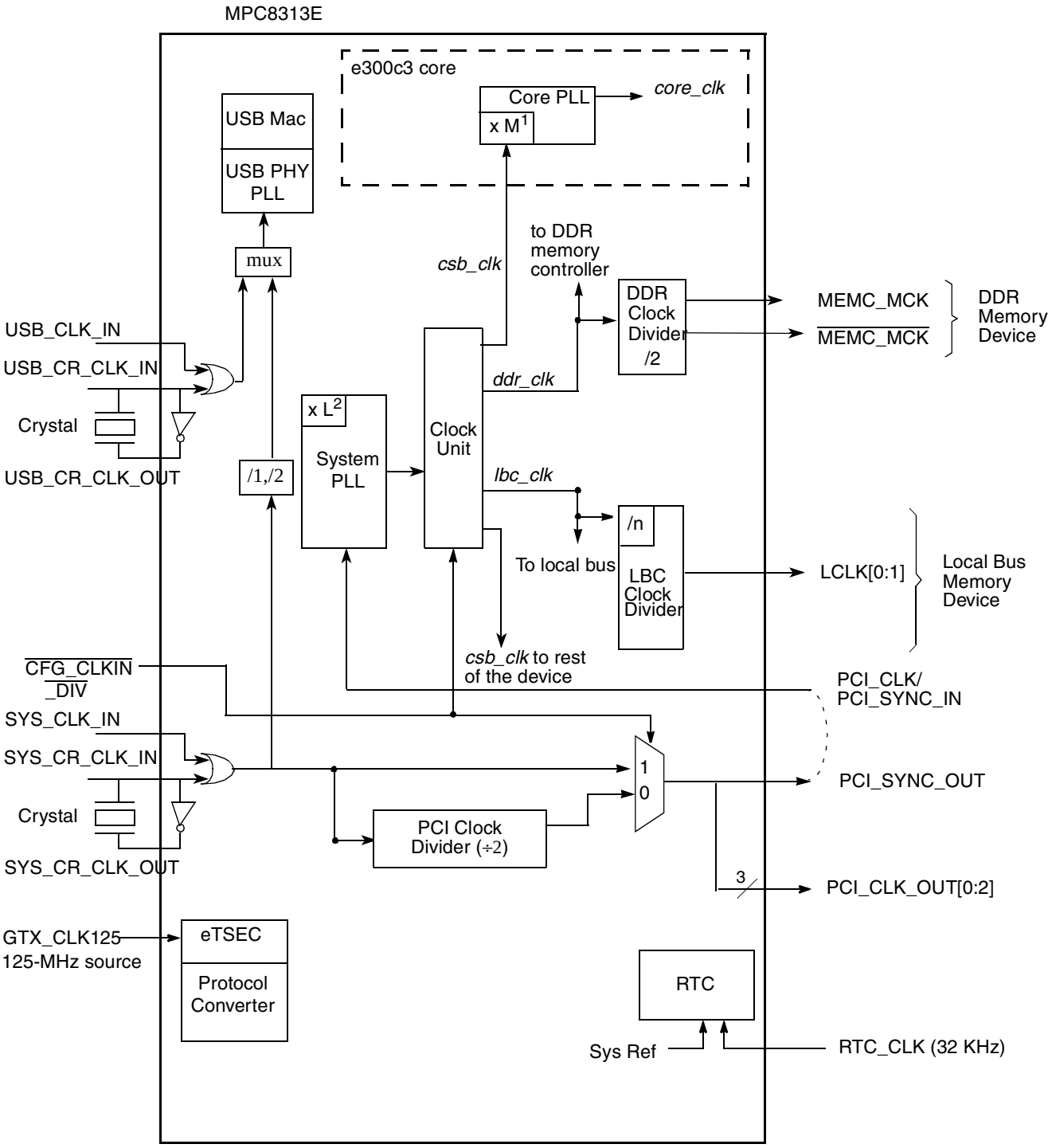
Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	K11,K12,K13,K14,K15,K16,L10,L17,M10,M17,N10,N17,U12,U13,T1,U2,V2,P5,U4			
V_{DDC}	F6,F10,F19,K6,K10,K17,K21,P6,P10,P17,R10,R17,T10,T17,U10,U11,U14,U15,U16,U17,W6,W21,AA6,AA10,AA14,AA19			
VSS	B1,B2,B8,B9,B16,B17,C1,C2,C3,C4,C5,C24,C25,C26,D3,D4,D12,D13,D20,D21,F8,F11,F13,F16,F17,F21,G2,G25,H2,H6,H21,H25,L4,L6,L11,L12,L13,L14,L15,L16,L21,L23,M4,M11,M12,M13,M14,M15,M16,M23,N1,N3,N6,N11,N12,N13,N14,N15,N16,N21,N23,P11,P12,P13,P14,P15,P16,P23,P25,R11,R12,R13,R14,R15,R16,R25,T6,T11,T12,T13,T14,T15,T16,T21,T25,U5,U6,U21,W4,W23,Y4,Y23,AA8,AA11,AA13,AA16,AA17,AA21,AC4,AC5,AC12,AC13,AC20,AC21,AD1,AE2,AE8,AE9,AE16,AE17,AF2,P2, R2,T3,P3,V4			

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to VSS.

19 Clocking

Figure 39 shows the internal distribution of clocks within the MPC8313E.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3.

2 Multiplication factor L = 2, 3, 4, 5 and 6. Value is decided by RCWLR[SPMF].

Figure 39. MPC8313E Clock Subsystem

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOE*n*] parameters select whether the PCI_SYNC_OUT is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to VSS.

As shown in Figure 39, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbc_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8313E PowerQUICC II Pro Integrated Host Processor Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbc_clk* frequency is determined by the following equation:

$$lbc\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the a LBC clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBC clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 56 specifies which units have a configurable clock frequency.

Table 56. Configurable Clock Units

Unit	Default Frequency	Options
TSEC1	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
TSEC2	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
Security Core, I2C, SAP, TPR	*csb_clk*	Off, *csb_clk*, csb_clk/2, *csb_clk*/3
USB DR	*csb_clk*	Off, csb_clk, csb_clk/2, *csb_clk*/3
PCI and DMA complex	*csb_clk*	Off, *csb_clk*

Table 57 provides the operating frequencies for the MPC8313E TEPBGA II under recommended operating conditions (see Table 2).

Table 57. Operating Frequencies for TEPBGA I I

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	333	MHz
Coherent system bus frequency (*csb_clk*)	167	MHz
DDR1/2 memory bus frequency (MCK)[2]	167	MHz
Local bus frequency (LCLK*n*)[3]	33–66	MHz
PCI input frequency (SYS_CLK_IN or PCI_CLK)	24–66	MHz

Notes:

1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM] and SCCR[USBDRCM] must be programmed such that the maximum internal operating frequency of the Security core and USB modules will not exceed their respective value listed in this table.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

Table 58. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

As described in Section 19, "Clocking," The LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_SYNC_IN) and the internal coherent system bus clock (*csb_clk*). Table 59 shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 59. CSB Frequency Options

CFG_CLKIN_DIV at reset [1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock Frequency(MHz)[2]			
			24	25	33.33	66.67
				csb_clk	Frequency(MHz)	
High	0010	2 : 1				133
High	0011	3 : 1			100	
High	0100	4 : 1		100	133	
High	0101	5 : 1	120	125	167	
High	0110	6 : 1	144	150		
Low	0010	2 : 1				133
Low	0011	3 : 1			100	
Low	0100	4 : 1		100	133	

Table 59. CSB Frequency Options (continued)

CFG_CLKIN_DIV at reset [1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock Frequency(MHz)[2]			
			24	25	33.33	66.67
				csb_clk	Frequency(MHz)	
Low	0101	5 : 1	120	125	167	
Low	0110	6 : 1	144	150		

1 CFG_CLKIN_DIV select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.

2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 60 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 60 should be considered as reserved.

NOTE

Core VCO frequency = Core frequency × VCO divider
VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 60. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO divider [1]
0–1	2–5	6		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	***nnnn***	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4

Table 60. e300 Core PLL Configuration (continued)

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO divider [1]
0–1	2–5	6		
10	0010	1	2.5:1	8
00	0011	0	3:1	2
01	0011	0	3:1	4
10	0011	0	3:1	8

1 Core VCO frequency = Core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400-800MHz.

19.3 Example Clock Frequency Combinations

Table 61 shows several possible frequency combinations that can be selected based on the indicated input reference frequencies, with RCWLR[LBCM] = 0 and RCWLR[DDRCM] =1, such that the LBC operates with a frequency equal to the frequency of csb_clk and the DDR controller operates at twice the frequency of csb_clk.

Table 61. System Clock Frequencies

						LBC(lbc_clk)				e300 Core(core_clk)				
SYS_CLK_IN/ PCI_CLK	SPMF [1]	vcod [2]	vco	CSB(csb_clk)	DDR (ddr_clk)	/2	/4	/8	USB ref [3]	×1	×1.5	×2	×2.5	×3
24.0	6	2	576.0	144.0	288.0		36	18.0	12.0	144.0	216	288	360	
24.0	5	2	480.0	120.0	240.0	60	30	15.0	12.0	120.0	180	240	300	360
25.0	6	2	600.0	150.0	300.0		37.5	18.8	Note 1	150.0	225	300	375	
25.0	5	2	500.0	125.0	250.0	62.5	31.25	15.6	Note1	125.0	188	250	313	375
32.0	5	2	640.0	160.0	320.0		40	20.0	16.0	160.0	240	320		
32.0	4	2	512.0	128.0	256.0	64	32	16.0	16.0	128.0	192	256	320	384
33.3	5	2	666.0	166.5	333.0		41.63	20.8	Note 1	166.5	250	333		
33.3	4	2	532.8	133.2	266.4	66.6	33.3	16.7	Note 1	133.2	200	266	333	400
48.0	3	2	576.0	144.0	288.0		36	18.0	48.0	144.0	216	288	360	

Table 61. System Clock Frequencies (continued)

66.7	2	2	533.4	133.3	266.7	66.7	33.34	16.7	Note 1	133.3	200	267	333	400

Note:

Note 1: USB reference clock must be supplied from a separate source as it must be 12, 16 or 48 MHz, the USB reference must be supplied from a separate external source using USB_CLK_IN. Note 2: When considering operating frequencies, the valid system APLL VCO operating range of 400-800 MHz must not be violated.

Note 3: csb_clk frequencies of less than 133MHz will not support Gigabit Ethernet data rates.

1 System PLL Multiplication Factor

2 System PLL VCO Divider

3 Frequency of USB PLL Input reference

20 Thermal

This section describes the thermal specifications of the MPC8313E.

20.1 Thermal Characteristics

Table 62 provides the package thermal characteristics for the 516 27 × 27 mm TEPBGAII.

Table 62. Package Thermal Characteristics for TEPBGAII

Characteristic	Board type	Symbol	TEPBGAII	Unit	Notes
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	25	°C/W	1,2
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	18	°C/W	1,2,3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	20	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1,3
Junction to Board		$R_{\theta JB}$	10	°C/W	4
Junction to Case		$R_{\theta JC}$	8	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	7	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package will be approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51–8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink will be required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 63. Heat Sinks and Junction-to-Case Thermal Resistance of MPC8313E (TEPBGAII)

Heat Sink Assuming Thermal Grease	Air Flow	35x35 mm TBGA
		Junction-to-Ambient Thermal Resistance
AAVID 30x30x9.4 mm Pin Fin	Natural Convection	10.7
AAVID 30x30x9.4 mm Pin Fin	1 m/s	6.2
AAVID 30x30x9.4 mm Pin Fin	2 m/s	5.3
AAVID 31x35x23 mm Pin Fin	Natural Convection	8.1
AAVID 31x35x23 mm Pin Fin	1 m/s	4.4
AAVID 31x35x23 mm Pin Fin	2 m/s	3.7
Wakefield, 53x53x25 mm Pin Fin	Natural Convection	5.4
Wakefield, 53x53x25 mm Pin Fin	1 m/s	3.2
Wakefield, 53x53x25 mm Pin Fin	2 m/s	2.4
MEI, 75x85x12 no adjacent board, extrusion	Natural Convection	6.4
MEI, 75x85x12 no adjacent board, extrusion	1 m/s	3.8
MEI, 75x85x12 no adjacent board, extrusion	2 m/s	2.5
MEI, 75x85x12 mm, adjacent board, 40 mm Side bypass	1 m/s	2.8

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink Vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO BOX 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

Where:

T_J = junction temperature (°C)

T_C = case temperature of the package

$R_{\theta JC}$ = junction-to-case thermal resistance

P_D = power dissipation

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8313E SYS_CLK_IN

21.1 System Clocking

The MPC8313E includes two PLLs.

1. The platform PLL (AV_{DD2}) generates the platform clock from the externally supplied SYS_CLK_IN input in PCI host mode or SYS_CLK_IN/PCI_SYNC_IN in PCI agent mode. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 19.1, “System PLL Configuration.”
2. The e300 Core PLL (AV_{DD1}) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, “Core PLL Configuration.”

21.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1}, AV_{DD2} respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 40, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 40 shows the PLL power supply filter circuit.

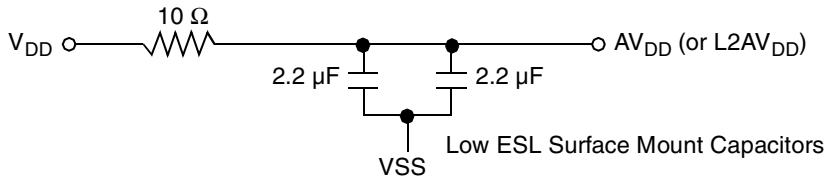


Figure 40. PLL Power Supply Filter Circuit

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8313E system, and the MPC8313E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, and LV_{DDB} pins of the device. These decoupling capacitors should receive their power from separate V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, LV_{DDB} and VSS power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, and LV_{DDB} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA} or LV_{DDB} as required. Unused active high inputs should be connected to VSS. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, LV_{DDB}, and VSS pins of the device.

21.5 Output Buffer DC Impedance

The MPC8313E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or VSS. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (see Figure 41). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

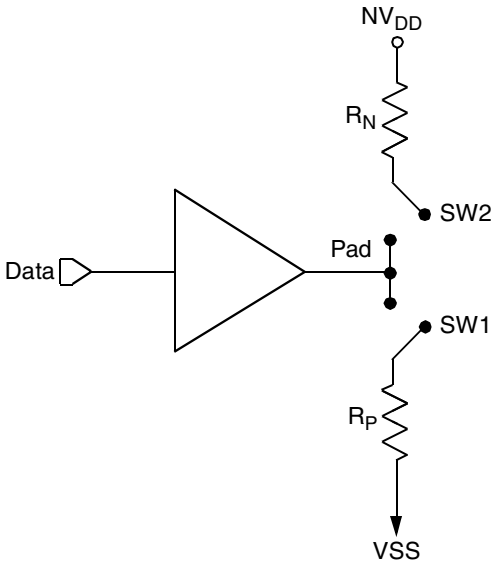


Figure 41. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 64 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal NV_{DD}, 105°C.

Table 64. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (not including PCI output clocks)	PCI Output Clocks (including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

21.6 Configuration Pin Muxing

The MPC8313E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

21.7 Pull-Up Resistor Requirements

The MPC8313E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins, Ethernet Management MDIO pin and EPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 42. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

21.8 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in IEEE Std. 1149.1, but is provided on all processors that implement the PowerPC architecture. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical.

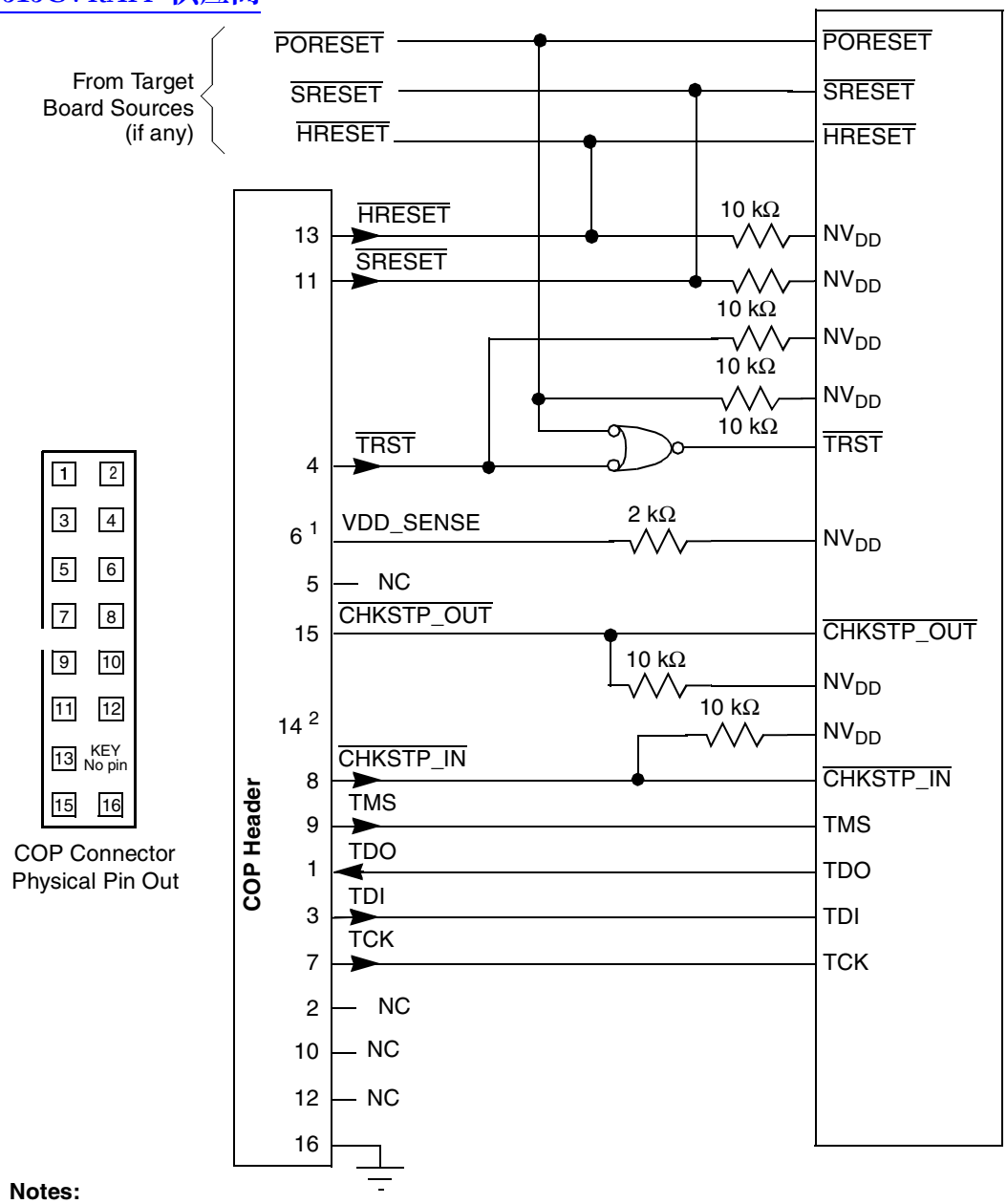
The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{TRST}}$ without causing $\overline{\text{PORESET}}$. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 42 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$ so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted.

The COP header shown in Figure 42 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 42; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 42 is common to all known emulators.



Notes:

1. Some systems require power to be fed from the application board into the debugger repeater card via the COP header. In this case the resistor value for VDD_SENSE should be around 20Ω.
2. Key location; pin 14 is not physically present on the COP header.

Figure 42. JTAG Interface Connection

22 Document Revision History

Table 22-61 provides a revision history for this hardware specification.

Table 65. Document Revision History

Revision	Date	Substantive Change(s)
0	06/2007	Initial release.

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 23.1, "Part Numbers Fully Addressed by This Document."

23.1 Part Numbers Fully Addressed by This Document

Table 66 provides the Freescale part numbering nomenclature for the MPC8313E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 66. Part Numbering Nomenclature

MPC	*nnnn*	*e*	*t*	*pp*	*aa*	*a*	*x*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [3]**	**Package [1]**	**e300 core Frequency [2]**	**DDR Frequency**	**Revision Level**
MPC	8313	Blank = Not included E = included	Blank = 0 to 105°C C= –40 to 105°C	VR= PB free TEPBGAII	AF = 333MHz	F = 333 MHz	Contact local Freescale sales office

Notes:

1. See Section 18, "Package and Pin Listings," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
3. Contact local Freescale office on availability of parts with C temperature range

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