



November 1988  
Revised November 1999

## 74AC245 • 74ACT245

### Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs

#### General Description

The AC/ACT245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

#### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Noninverting buffers
- Bidirectional data path
- A and B outputs source/sink 24 mA
- ACT245 has TTL-compatible inputs

#### Ordering Code:

Order Number	Package Number	Package Description
74AC245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74AC245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACT245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ACT245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

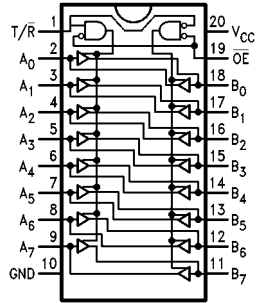
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

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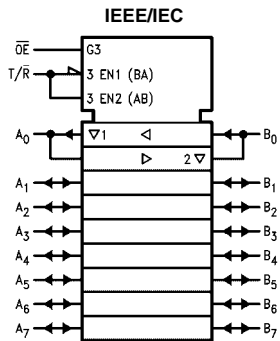
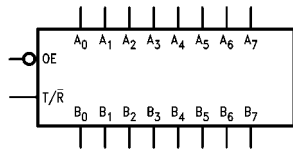
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### Connection Diagram



### Logic Symbols



### Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
$A_0-A_7$	Side A 3-STATE Inputs or 3-STATE Outputs
$B_0-B_7$	Side B 3-STATE Inputs or 3-STATE Outputs

### Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions	
Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V	Supply Voltage ( $V_{CC}$ )	AC 2.0V to 6.0V
DC Input Diode Current ( $I_{IK}$ )		ACT 4.5V to 5.5V	
$V_I = -0.5V$	-20 mA	Input Voltage ( $V_I$ )	0V to $V_{CC}$
$V_I = V_{CC} + 0.5V$	+20 mA	Output Voltage ( $V_O$ )	0V to $V_{CC}$
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$	Operating Temperature ( $T_A$ )	-40°C to +85°C
DC Output Diode Current ( $I_{OK}$ )		Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
$V_O = -0.5V$	-20 mA	AC Devices	
$V_O = V_{CC} + 0.5V$	+20 mA	$V_{IN}$ from 30% to 70% of $V_{CC}$	
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$	$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA	Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA	ACT Devices	
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C	$V_{IN}$ from 0.8V to 2.0V	
Junction Temperature ( $T_J$ )		$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns
PDIP	140°C	<b>Note 1:</b> Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.	

DC Electrical Characteristics for AC								
Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9		V	$I_{OUT} = -50 \mu A$
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46		V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2)
		4.5		3.86	3.76			
		5.5		4.86	4.76			
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1		V	$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44		V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2)
		4.5		0.36	0.44			
		5.5		0.36	0.44			
$I_{IN}$ (Note 4)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$		$\mu A$	$V_I = V_{CC}, GND$
$I_{OLD}$	Dynamic Output	5.5			75		mA	$V_{OLD} = 1.65V$ Max
$I_{OHD}$	Current Minimum (Note 3)	5.5			-75		mA	$V_{OHD} = 3.85V$ Min
$I_{CC}$ (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0		$\mu A$	$V_{IN} = V_{CC}$ or GND
$I_{OZT}$	Maximum I/O Leakage Current	5.5		$\pm 0.3$	$\pm 3.0$		$\mu A$	$V_I$ (OE) = $V_{IL}, V_{IH}$ $V_I = V_{CC}, GND$ $V_O = V_{CC}, GND$

**Note 2:** All outputs loaded; thresholds on input associated with output under test.  
**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.  
**Note 4:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

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DC Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4		V	I <sub>OUT</sub> = -50 μA
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 5)
		5.5		4.86	4.76			
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1		V	I <sub>OUT</sub> = 50 μA
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44		V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 5)
		5.5		0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	Dynamic Output Current Minimum (Note 6)	5.5			75		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Current Minimum (Note 6)	5.5			-75		mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5		±0.3	±3.0		μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND

**Note 5:** All outputs loaded; thresholds on input associated with output under test.  
**Note 6:** Maximum test duration 2.0 ms, one output loaded at a time.

### AC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V) (Note 7)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	3.3	1.5	5.0	8.5	1.0	9.0	ns
		5.0	1.5	3.5	6.5	1.0	7.0	
t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	3.3	1.5	5.0	8.5	1.0	9.0	ns
		5.0	1.5	3.5	6.0	1.0	7.0	
t <sub>PZH</sub>	Output Enable Time	3.3	2.5	7.0	11.5	2.0	12.5	ns
		5.0	1.5	5.0	8.5	1.0	9.0	
t <sub>PZL</sub>	Output Enable Time	3.3	2.5	7.5	12.0	2.0	13.5	ns
		5.0	1.5	5.5	9.0	1.0	9.5	
t <sub>PHZ</sub>	Output Disable Time	3.3	2.0	6.5	12.0	1.0	12.5	ns
		5.0	1.5	5.5	9.0	1.0	10.0	
t <sub>PLZ</sub>	Output Disable Time	3.3	2.0	7.0	11.5	1.5	13.0	ns
		5.0	1.5	5.5	9.0	1.0	10.0	

**Note 7:** Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	5.0	1.5	4.0	7.5	1.5	8.0	ns
t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	5.0	1.5	4.0	8.0	1.0	9.0	ns
t <sub>PZH</sub>	Output Enable Time	5.0	1.5	5.0	10.0	1.5	11.0	ns
t <sub>PZL</sub>	Output Enable Time	5.0	1.5	5.5	10.0	1.5	12.0	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	1.5	5.5	10.0	1.0	11.0	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	2.0	5.0	10.0	1.5	11.0	ns

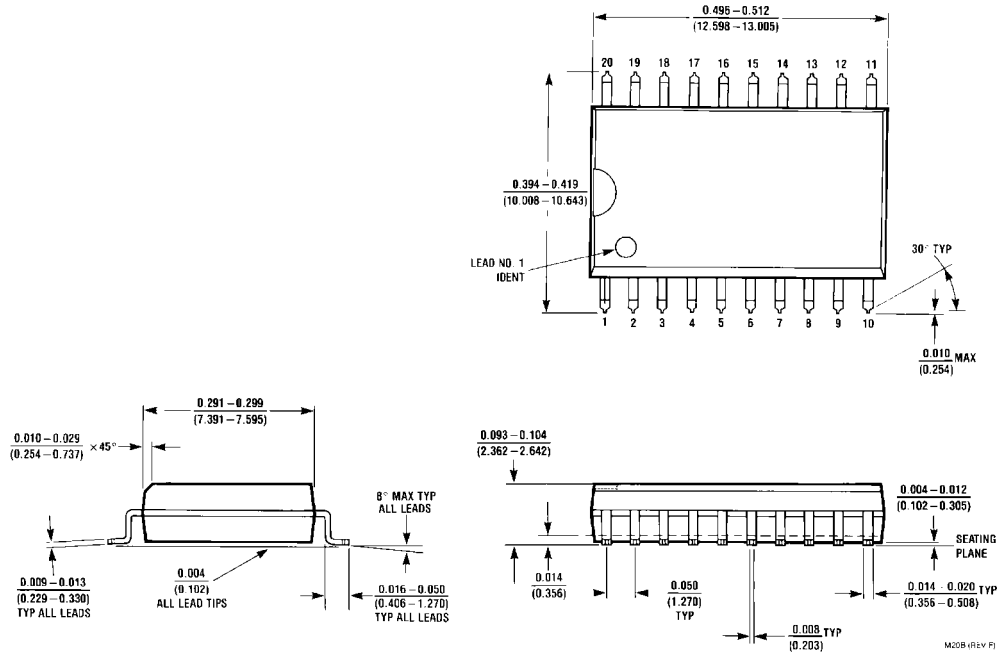
**Note 8:** Voltage Range 5.0 is 5.0V ± 0.5V

### Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>I/O</sub>	Input/Output Capacitance	15.0	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	45.0	pF	V <sub>CC</sub> = 5.0V

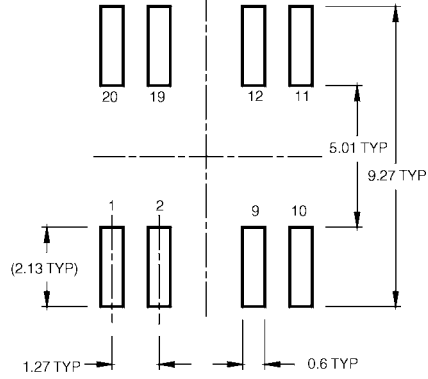
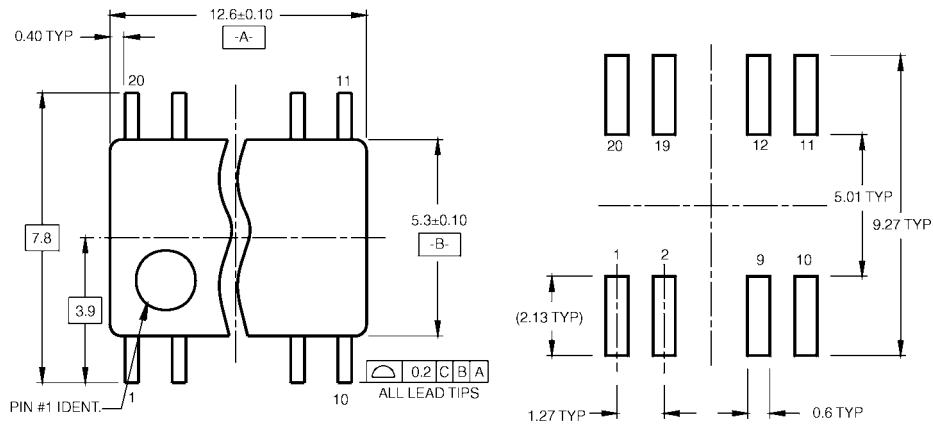
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**Physical Dimensions** inches (millimeters) unless otherwise noted

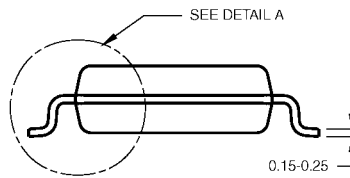
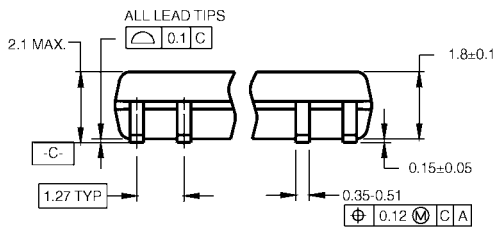


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



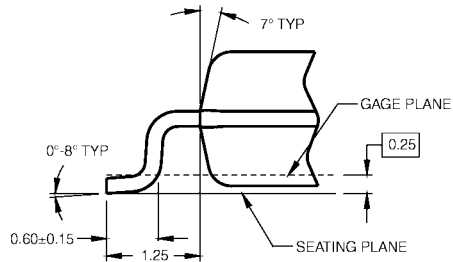
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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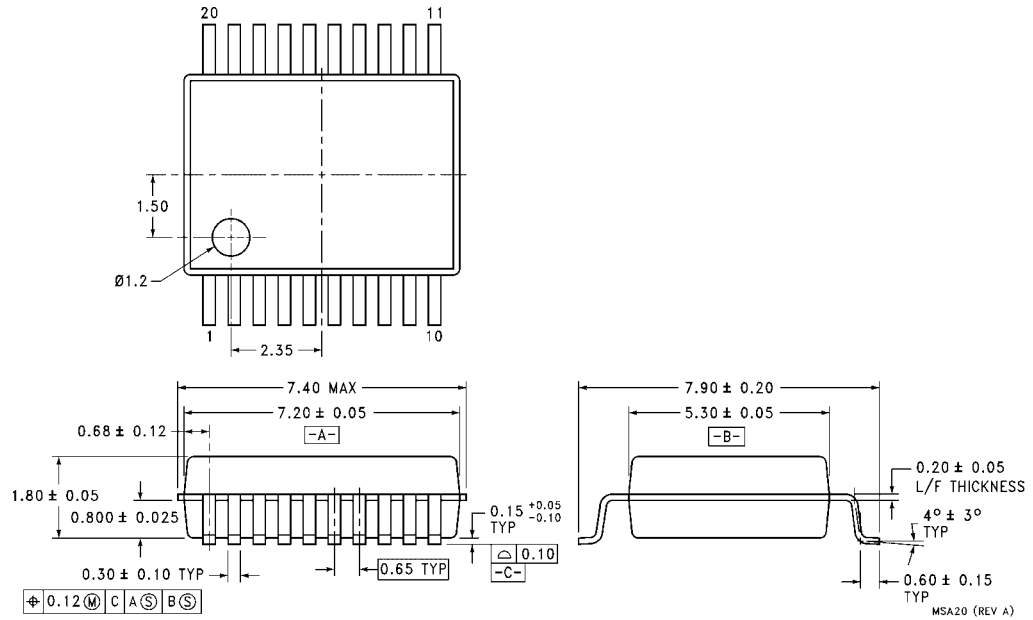


DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

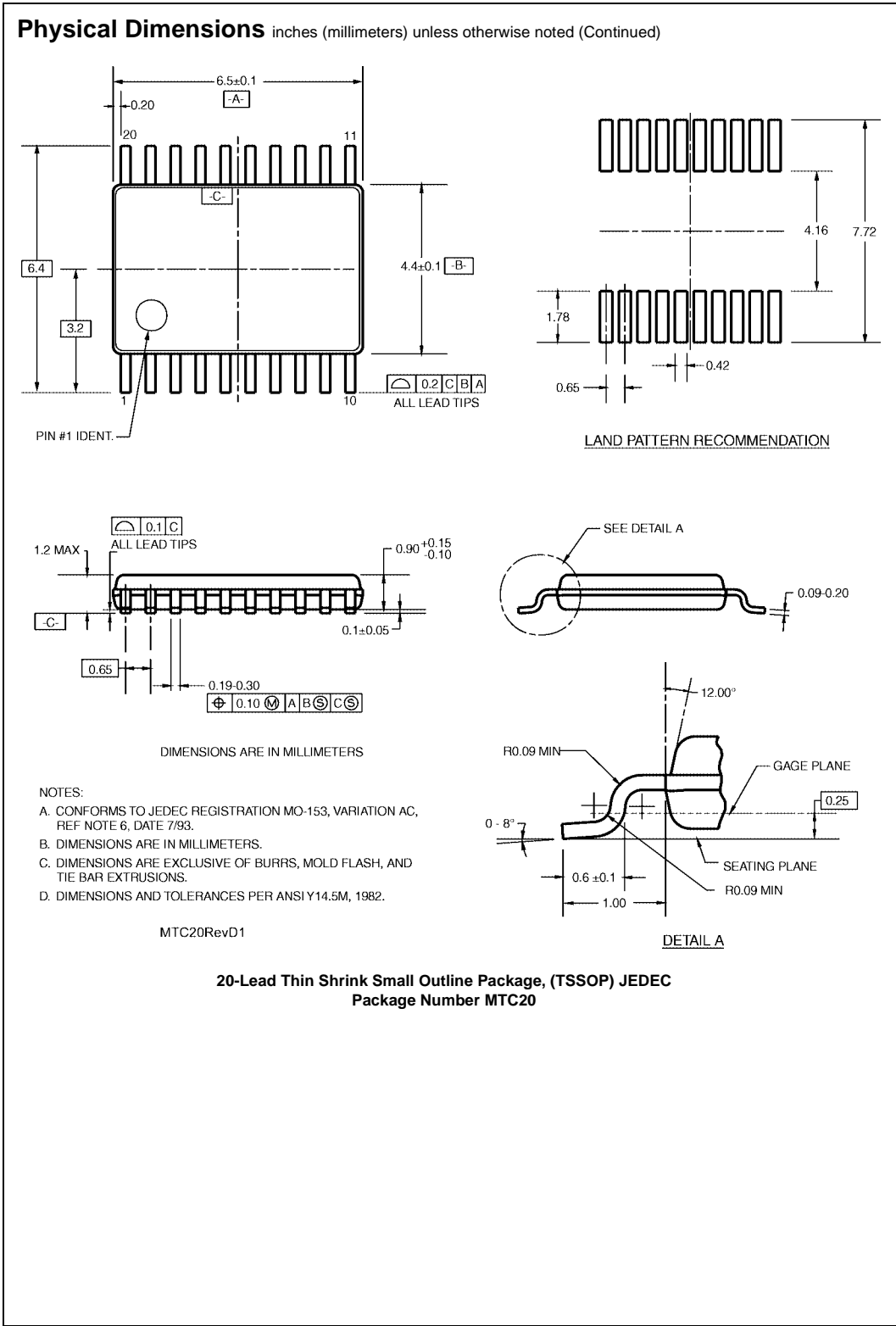
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**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

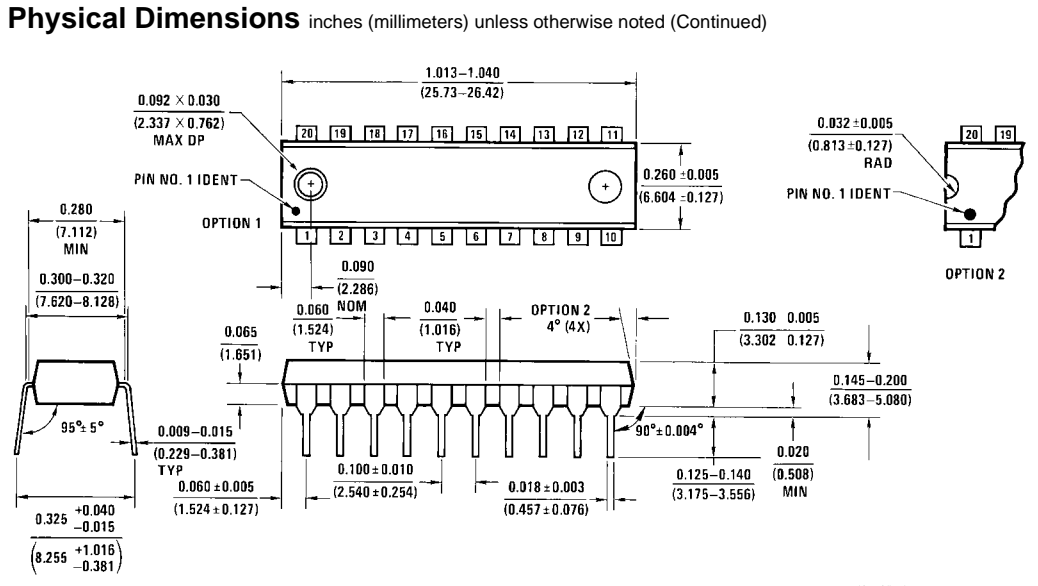


**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA20**





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20-Lead Plastic Dual-In-Line (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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