

## LP3996

# Dual Linear Regulator with 300mA and 150mA Outputs and Power-On-Reset

## General Description

The LP3996 is a dual low dropout regulator with power-on-reset circuit. The first regulator can source 150mA, while the second is capable of sourcing 300mA and has a power-on-reset function included.

The LP3996 provides 1.5% accuracy requiring an ultra low quiescent current of 35µA. Separate enable pins allow each output of the LP3996 to be shut down, drawing virtually zero current.

The LP3996 is designed to be stable with small footprint ceramic capacitors down to 1µF. An external capacitor may be used to set the POR delay time as required.

The LP3996 is available in fixed output voltages and comes in a 10 pin, 3mm x 3mm, LLP package. .

## Features

- 2 LDO Outputs with Independent Enable
- 1.5% Accuracy at Room Temperature, 3% over Temperature
- Power-On-Reset Function with Adjustable Delay
- Thermal Shutdown Protection
- Stable with Ceramic Capacitors

## Key Specifications

- |                                   |                |
|-----------------------------------|----------------|
| ■ Input Voltage Range             | 2.0V to 6.0V   |
| ■ Low Dropout Voltage             | 210mV at 300mA |
| ■ Ultra-Low $I_Q$ (enabled)       | 35µA           |
| ■ Virtually Zero $I_Q$ (disabled) | <10nA          |

## Package

All available in Lead Free option.

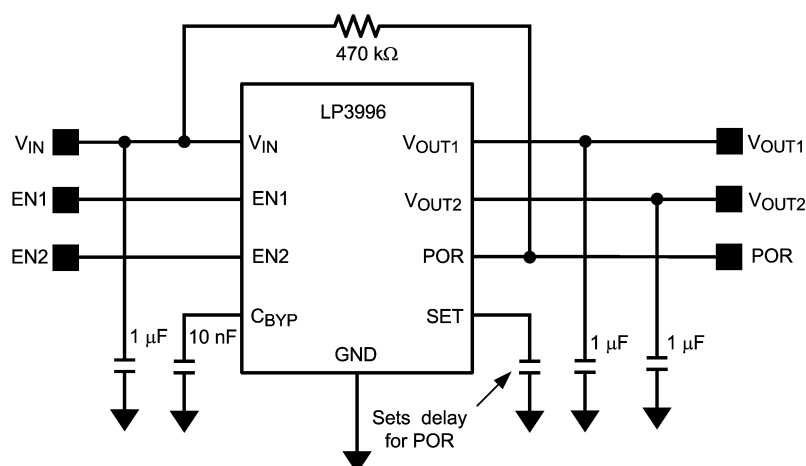
10 pin LLP 3mm x 3mm

For other package options contact your NSC sales office.

## Applications

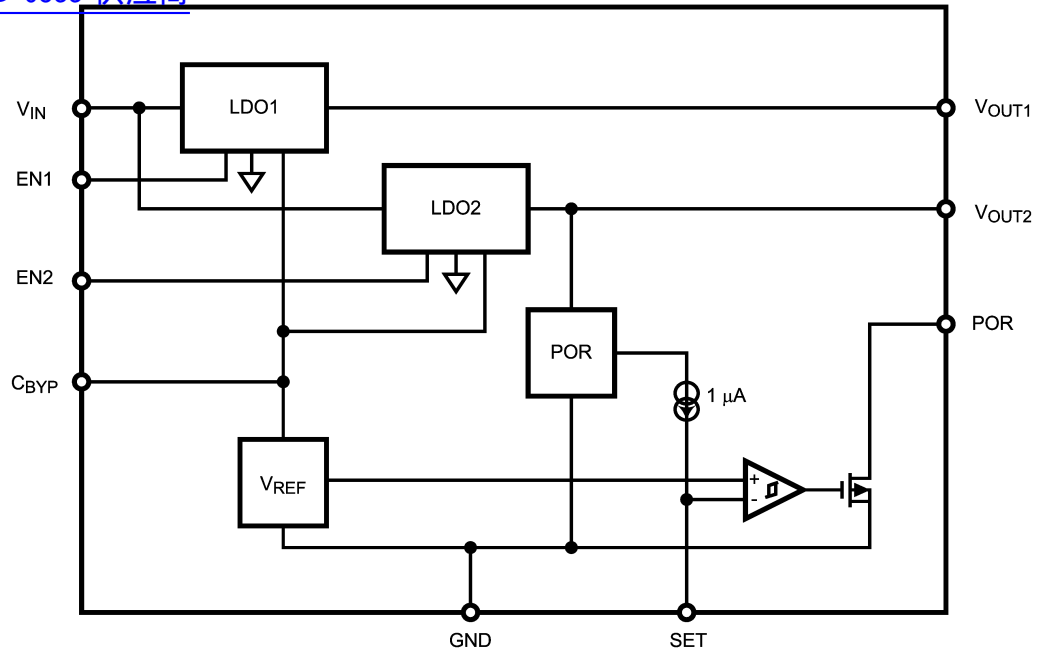
- Cellular Handsets
- PDA's
- Wireless Network Adaptors

## Typical Application Circuit



20145801

## Functional Block Diagram



20145806

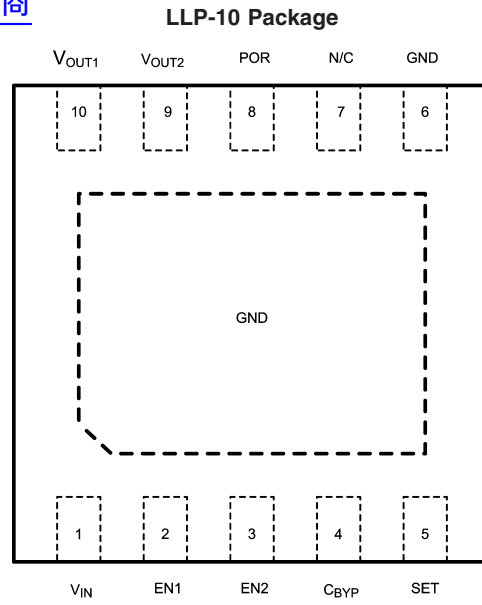
## Pin Descriptions

### LLP-10 Package

Pin No	Symbol	Name and Function
1	$V_{IN}$	Voltage Supply Input. Connect a $1\mu F$ capacitor between this pin and GND.
2	EN1	Enable Input to Regulator 1. Active high input. High = On. Low = OFF.
3	EN2	Enable Input to Regulator 2. Active high input. High = On. Low = OFF.
4	$C_{BYP}$	Internal Voltage Reference Bypass. Connect a $10nF$ capacitor from this pin to GND to reduce output noise and improve line transient and PSRR. This pin may be left open.
5	SET	Set Delay Input. Connect a capacitor between this pin and GND to set the POR delay time. If left open, there will be no delay.
6	GND	Common Ground pin. Connect externally to exposed pad.
7	N/C	No Connection. Do not connect to any other pin.
8	POR	Power-On Reset Output. Open drain output. Active low indicates under-voltage output on Regulator 2. A pull-up resistor is required for correct operation.
9	$V_{OUT2}$	Output of Regulator 2. 300mA maximum current output. Connect a $1\mu F$ capacitor between this pin and GND.
10	$V_{OUT1}$	Output of Regulator 1. 150mA maximum current output. Connect a $1\mu F$ capacitor between this pin and GND.
Pad	GND	Common Ground. Connect to Pin 6.

# Connection Diagram

[查询"LP3996SD-0833"供应商](#)



**Top View**

20145803

See NS package number **SDA10A**

## Ordering Information (LLP-10)

请向"LP3996SD-0833"供应商

For other voltage options, please contact your local NSC sales office

Output Voltage (V)	Order Number	Spec	Package Marking	Supplied As
0.8 / 3.3	LP3996SD-0833	NOPB	L167B	1000 Units, Tape-and-Reel
	LP3996SDX-0833	NOPB		4500 Units, Tape-and-Reel
	LP3996SD-0833			1000 Units, Tape-and-Reel
	LP3996SDX-0833			4500 Units, Tape-and-Reel
1.5 / 2.5	LP3996SD-1525	NOPB	L168B	1000 Units, Tape-and-Reel
	LP3996SDX-1525	NOPB		4500 Units, Tape-and-Reel
	LP3996SD-1525			1000 Units, Tape-and-Reel
	LP3996SDX-1525			4500 Units, Tape-and-Reel
2.8 / 2.8	LP3996SD-2828	NOPB	L171B	1000 Units, Tape-and-Reel
	LP3996SDX-2828	NOPB		4500 Units, Tape-and-Reel
	LP3996SD-2828			1000 Units, Tape-and-Reel
	LP3996SDX-2828			4500 Units, Tape-and-Reel
3.0 / 3.0	LP3996SD-3030	NOPB	L172B	1000 Units, Tape-and-Reel
	LP3996SDX-3030	NOPB		4500 Units, Tape-and-Reel
	LP3996SD-3030			1000 Units, Tape-and-Reel
	LP3996SDX-3030			4500 Units, Tape-and-Reel
3.0 / 3.3	LP3996SD-3033	NOPB	L170B	1000 Units, Tape-and-Reel
	LP3996SDX-3033	NOPB		4500 Units, Tape-and-Reel
	LP3996SD-3033			1000 Units, Tape-and-Reel
	LP3996SDX-3033			4500 Units, Tape-and-Reel
3.3 / 0.8	LP3996SD-3308	NOPB	L188B	1000 Units, Tape-and-Reel
	LP3996SDX-3308	NOPB		4500 Units, Tape-and-Reel
	LP3996SD-3308			1000 Units, Tape-and-Reel
	LP3996SDX-3308			4500 Units, Tape-and-Reel
3.3 / 3.3	LP3996SD-3333	NOPB	L173B	1000 Units, Tape-and-Reel
	LP3996SDX-3333	NOPB		4500 Units, Tape-and-Reel
	LP3996SD-3333			1000 Units, Tape-and-Reel
	LP3996SDX-3333			4500 Units, Tape-and-Reel

## Absolute Maximum Ratings

(Notes 1, 2)  
[查询"LP3996SD-0833"供应商](#)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage to GND	-0.3V to 6.5V
$V_{OUT1}$ , $V_{OUT2}$ EN1 and EN2 Voltage to GND	-0.3V to ( $V_{IN} + 0.3V$ ) with 6.5V (max)
POR to GND	-0.3V to 6.5V
Junction Temperature ( $T_{J-MAX}$ )	150°C
Lead/Pad Temp. (Note 3)	235°C
Storage Temperature	-65°C to 150°C
Continuous Power Dissipation Internally Limited (Note 4)	
ESD Rating (Note 5)	
Human Body Model	2.0kV
Machine Model	200V

## Operating Ratings

(Notes 1, 2)

Input Voltage	2.0V to 6.0V
EN1, EN2, POR Voltage	0 to ( $V_{IN} + 0.3V$ ) to 6.0V (max)
Junction Temperature	-40°C to 125°C
Ambient Temperature $T_A$ Range (Note 6)	-40°C to 85°C

## Thermal Properties

(Note 1)

Junction To Ambient Thermal Resistance (Note 7)	
$\theta_{JA}$ LLP-10 Package	55°C/W

## Electrical Characteristics

(Notes 2, 8)

Unless otherwise noted,  $V_{EN} = 950mV$ ,  $V_{IN} = V_{OUT} + 1.0V$ , or 2.0V, whichever is higher, where  $V_{OUT}$  is the higher of  $V_{OUT1}$  and  $V_{OUT2}$ .  $C_{IN} = 1 \mu F$ ,  $I_{OUT} = 1 mA$ ,  $C_{OUT1} = C_{OUT2} = 1.0 \mu F$ . Typical values and limits appearing in normal type apply for  $T_A = 25^\circ C$ . Limits appearing in **boldface** type apply over the full junction temperature range for operation, -40 to +125°C.

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$V_{IN}$	Input Voltage	(Note 9)		2	6	V
$\Delta V_{OUT}$	Output Voltage Tolerance	$I_{OUT} = 1mA$		-2.5	+2.5	%
		$1.5V < V_{OUT} \leq 3.3V$		<b>-3.75</b>	<b>+3.75</b>	
		$V_{OUT} \leq 1.5V$		-2.75	+2.75	
	Line Regulation Error	$V_{IN} = (V_{OUT(NOM)} + 1.0V)$ to 6.0V	0.03		<b>0.3</b>	%/V
	Load Regulation Error	$I_{OUT} = 1mA$ to 150mA (LDO 1)	85		<b>155</b>	$\mu V/mA$
		$I_{OUT} = 1mA$ to 300mA (LDO 2)	26		<b>85</b>	
$V_{DO}$	Dropout Voltage (Note 10)	$I_{OUT} = 1mA$ to 150mA (LDO 1)	110		<b>220</b>	mV
		$I_{OUT} = 1mA$ to 300mA (LDO 2)	210		<b>550</b>	
$I_Q$	Quiescent Current	LDO 1 ON, LDO 2 ON $I_{OUT1} = I_{OUT2} = 0mA$	35		<b>100</b>	$\mu A$
		LDO 1 ON, LDO 2 OFF $I_{OUT1} = 150mA$	45		<b>110</b>	
		LDO 1 OFF, LDO 2 ON $I_{OUT2} = 300mA$	45		<b>110</b>	
		LDO 1 ON, LDO 2 ON $I_{OUT1} = 150mA$ , $I_{OUT2} = 300mA$	70		<b>170</b>	
		$V_{EN1} = V_{EN2} = 0.4V$	0.5		<b>10</b>	nA
$I_{SC}$	Short Circuit Current Limit	LDO 1	420		<b>750</b>	mA
		LDO 2	550		<b>840</b>	
$I_{OUT}$	Maximum Output Current	LDO 1		<b>150</b>		mA
		LDO 2		<b>300</b>		

## Electrical Characteristics (Notes 2, 8) (Continued)

LP33960B-0830,  $V_{REG} = 950\text{mV}$ ,  $V_{IN} = V_{OUT} + 1.0\text{V}$ , or  $2.0\text{V}$ , whichever is higher, where  $V_{OUT}$  is the higher of  $V_{OUT1}$  and  $V_{OUT2}$ .  $C_{IN} = 1\mu\text{F}$ ,  $I_{OUT} = 1\text{mA}$ ,  $C_{OUT1} = C_{OUT2} = 1.0\mu\text{F}$ . Typical values and limits appearing in normal type apply for  $T_A = 25^\circ\text{C}$ . Limits appearing in **boldface** type apply over the full junction temperature range for operation,  $-40$  to  $+125^\circ\text{C}$ .

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
PSRR	Power Supply Rejection Ratio (Note 11)	f = 1kHz, I <sub>OUT</sub> = 1mA to 150mA	LDO1	58			dB
		C <sub>BYP</sub> = 10nF	LDO2	70			
		f = 20kHz, I <sub>OUT</sub> = 1mA to 150mA	LDO1	45			
		C <sub>BYP</sub> = 10nF	LDO2	60			
e <sub>n</sub>	Output noise Voltage (Note 11)	BW = 10Hz to 100kHz C <sub>BYP</sub> = 10nF	V <sub>OUT</sub> = 0.8V	36			μV <sub>RMS</sub>
			V <sub>OUT</sub> = 3.3V	75			
T <sub>SHUTDOWN</sub>	Thermal Shutdown	Temperature		160			°C
		Hysteresis		20			
Enable Control Characteristics							
I <sub>EN</sub>	Input Current at V <sub>EN1</sub> or V <sub>EN2</sub>	V <sub>EN</sub> = 0.0V		0.005		0.1	μA
		V <sub>EN</sub> = 6V		2		5	
V <sub>IL</sub>	Low Input Threshold at V <sub>EN1</sub> or V <sub>EN2</sub>					0.4	V
V <sub>IH</sub>	High Input Threshold at V <sub>EN1</sub> or V <sub>EN2</sub>				0.95		V
POR Output Characteristics							
V <sub>TH</sub>	Low Threshold % Of V <sub>OUT2 (NOM)</sub>	Flag ON			88		%
	High Threshold % Of V <sub>OUT2 (NOM)</sub>	Flag OFF				96	
I <sub>POR</sub>	Leakage Current	Flag OFF, V <sub>POR</sub> = 6.5V		30			nA
V <sub>OL</sub>	Flag Output Low Voltage	I <sub>SINK</sub> = 250μA		20			mV
Timing Characteristics							
T <sub>ON</sub>	Turn On Time (Note 11)	To 95% Level C <sub>BYP</sub> = 10nF		300			μs
Transient Response	Line Transient Response  δV <sub>OUT</sub>   (Note 11)	T <sub>rise</sub> = T <sub>fall</sub> = 10μs δV <sub>IN</sub> = 1VC <sub>BYP</sub> = 10nF		20			mV (pk - pk)
	Load Transient Response  δV <sub>OUT</sub>   (Note 11)	T <sub>rise</sub> = T <sub>fall</sub> = 1μs	LDO 1 I <sub>OUT</sub> = 1mA to 150mA	175			
			LDO 2 I <sub>OUT</sub> = 1mA to 300mA	150			
SET Input Characteristics							
I <sub>SET</sub>	SET Pin Current Source	V <sub>SET</sub> = 0V		1.3			μA
V <sub>TH(SET)</sub>	SET Pin Threshold Voltage	POR = High		1.25			V

## Electrical Characteristics (Notes 2, 8) (Continued)

**Note 1:** Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

**Note 2:** All Voltages are with respect to the potential at the GND pin.

**Note 3:** For detailed soldering specifications and information, please refer to National Semiconductor Application Note AN-1187, Leadless Leadframe Package.

**Note 4:** Internal thermal shutdown circuitry protects the device from permanent damage.

**Note 5:** The human body model is 100pF discharged through a 1.5k $\Omega$  resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

**Note 6:** The maximum ambient temperature ( $T_{A(max)}$ ) is dependant on the maximum operating junction temperature ( $T_{J(max-op)} = 125^{\circ}C$ ), the maximum power dissipation of the device in the application ( $P_{D(max)}$ ), and the junction to ambient thermal resistance of the part/package in the application ( $\theta_{JA}$ ), as given by the following equation:  $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$ .

**Note 7:** Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

**Note 8:** Min Max limits are guaranteed by design, test or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

**Note 9:**  $V_{IN(MIN)} = V_{OUT(NOM)} + 0.5V$ , or 2.0V, whichever is higher.

**Note 10:** Dropout voltage is voltage difference between input and output at which the output voltage drops to 100mV below its nominal value. This parameter only for output voltages above 2.0V

**Note 11:** This electrical specification is guaranteed by design.

## Output Capacitor, Recommended Specifications

Symbol	Parameter	Conditions	Nom	Limit		Units
				Min	Max	
$C_{OUT}$	Output Capacitance	Capacitance (Note 12)	1.0	0.7		$\mu F$
		ESR		5	500	m $\Omega$

**Note 12:** The Capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor is X7R. However, depending on the application, X5R, Y5V and Z5U can also be used. (See capacitor section in Applications Hints).

## Transient Test Conditions

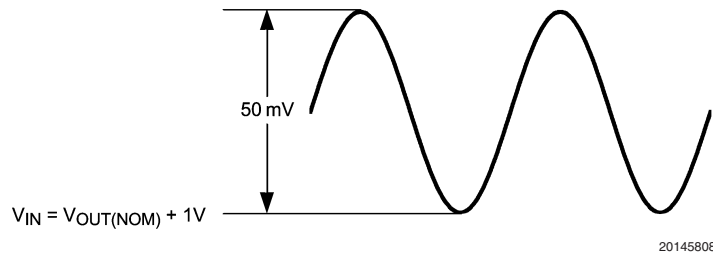


FIGURE 1. PSRR Input Signal

## Transient Test Conditions (Continued)

请向"LP3996SD-0833"供应商

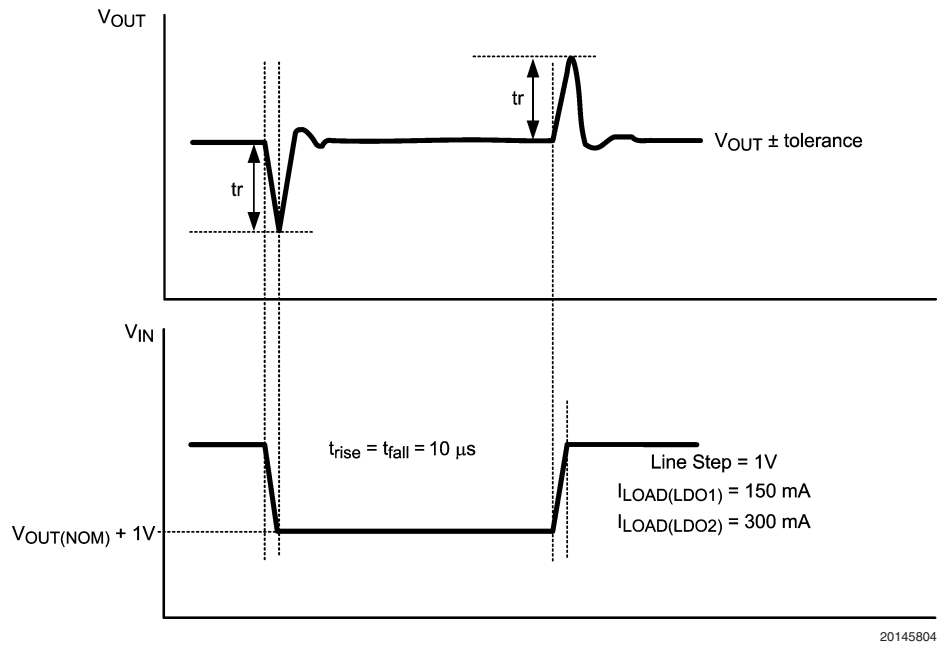


FIGURE 2. Line Transient Input Test Signal

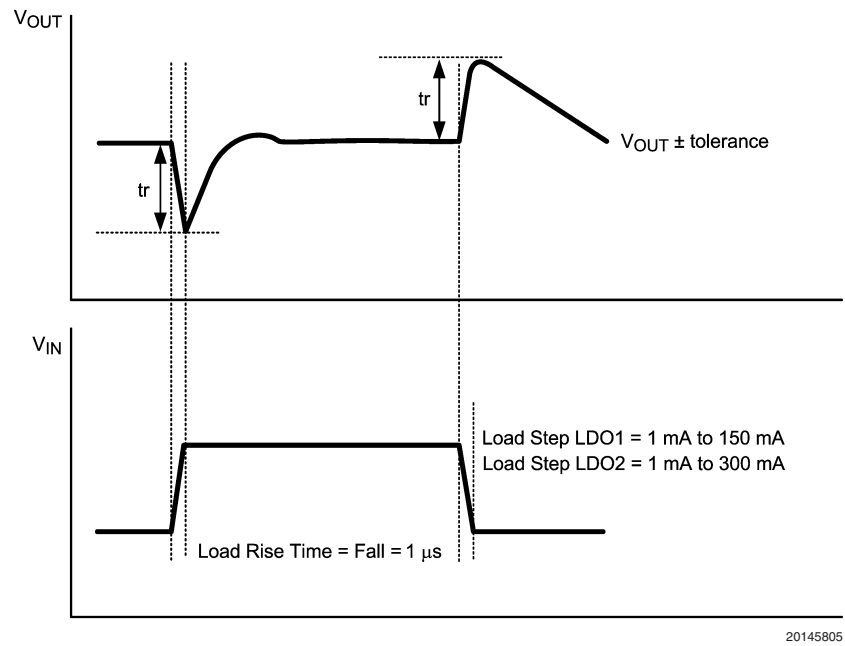


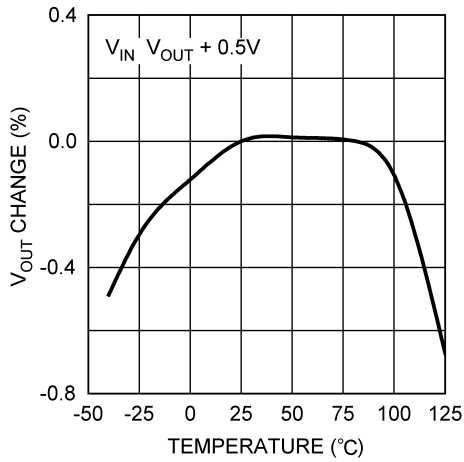
FIGURE 3. Load Transient Input Signal



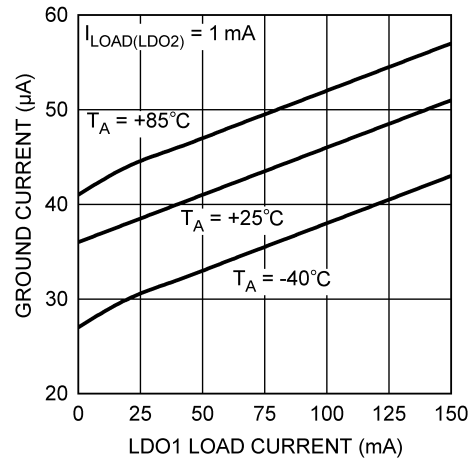
# Typical Performance Characteristics.

Unless otherwise specified,  $C_{IN} = 1.0\mu F$  Ceramic,  $C_{OUT1} = C_{OUT2} = 10\mu F$  Ceramic,  $V_{IN} = V_{OUT2(NOM)} + 1.0V$ ,  $T_A = 25^\circ C$ ,  $V_{OUT1(NOM)} = 3.3V$ ,  $V_{OUT2(NOM)} = 3.3V$ , Enable pins are tied to  $V_{IN}$ .

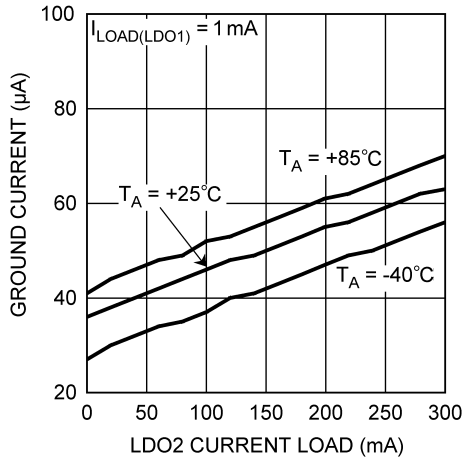
Output Voltage Change vs Temperature



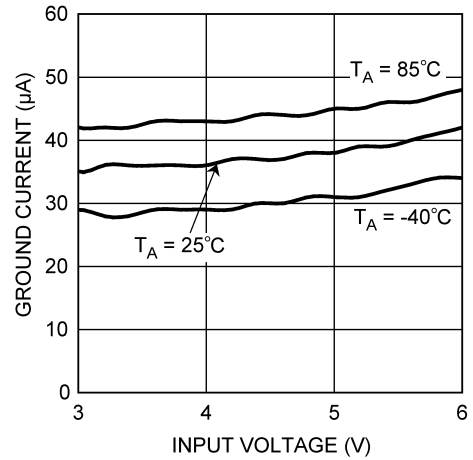
Ground Current vs Load Current, LDO1



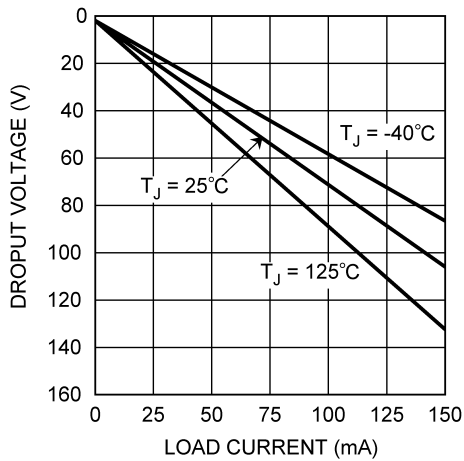
Ground Current vs Load Current, LDO2



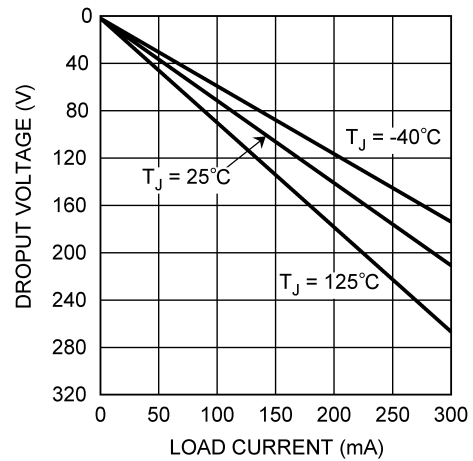
Ground Current vs  $V_{IN}$ ,  $I_{LOAD} = 1mA$



Dropout Voltage vs  $I_{LOAD}$ , LDO1



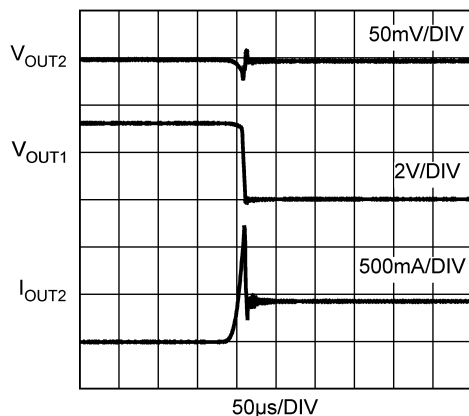
Dropout Voltage vs  $I_{LOAD}$ , LDO2



## Typical Performance Characteristics.

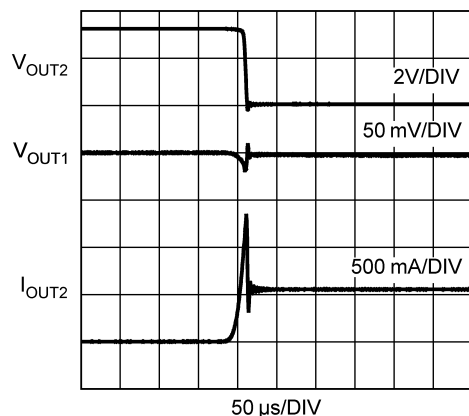
Unless otherwise specified,  $C_{IN} = 1.0\mu\text{F}$  Ceramic,  $C_{OUT1} = C_{OUT2} = 10\mu\text{F}$  Ceramic,  $C_{BYP} = 10\text{nF}$ ,  $V_{IN} = V_{OUT2(NOM)} + 1.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT1(NOM)} = 3.3\text{V}$ ,  $V_{OUT2(NOM)} = 3.3\text{V}$ , Enable pins are tied to  $V_{IN}$ . (Continued)

### Short Circuit Current, LDO1



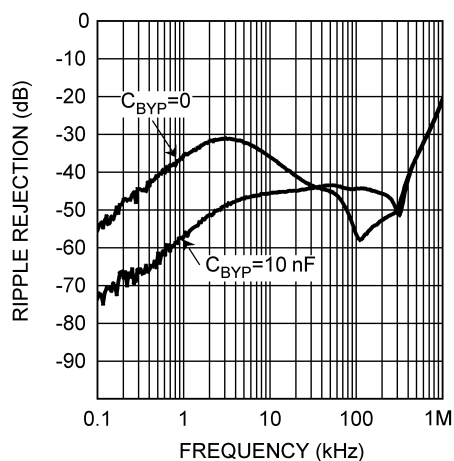
20145852

### Short Circuit Current, LDO2



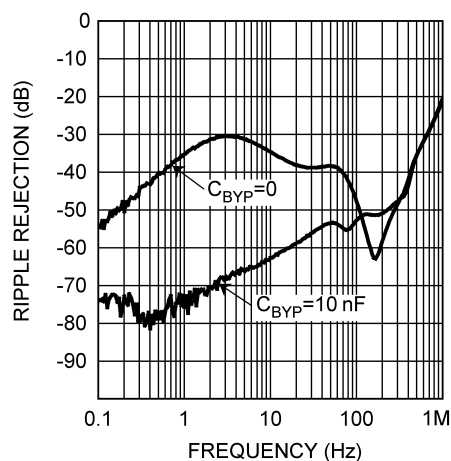
20145853

### Power Supply Rejection Ratio, LDO1



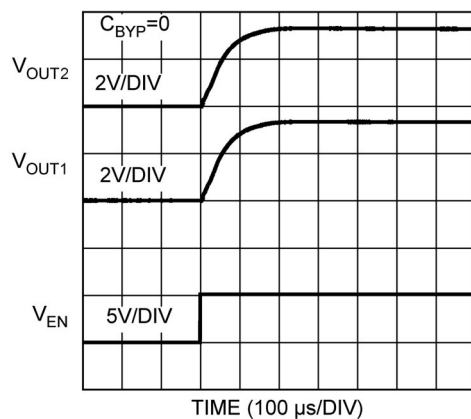
20145855

### Power Supply Rejection Ratio, LDO2



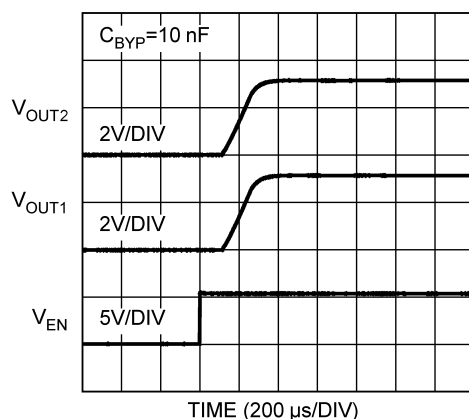
20145854

### Enable Start-up Time, $C_{BYP}=0$



20145860

### Enable Start-up Time, $C_{BYP}=10\text{nF}$



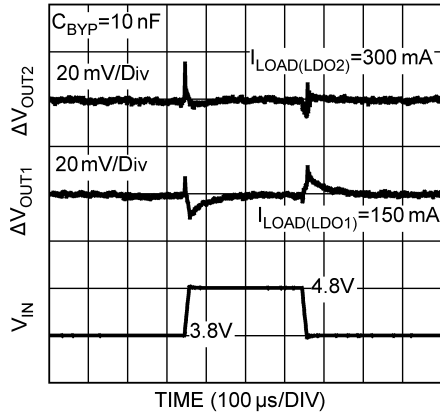
20145861

# Typical Performance Characteristics.

Unless otherwise specified,  $C_{IN} = 1.0\mu F$  Ceramic,  $C_{OUT1} = C_{OUT2} = 0.1\mu F$  Ceramic,  $V_{IN} = V_{OUT2(NOM)} + 1.0V$ ,  $T_A = 25^\circ C$ ,  $V_{OUT1(NOM)} = 3.3V$ ,  $V_{OUT2(NOM)} = 3.3V$ , Enable pins are tied to  $V_{IN}$ . (Continued)

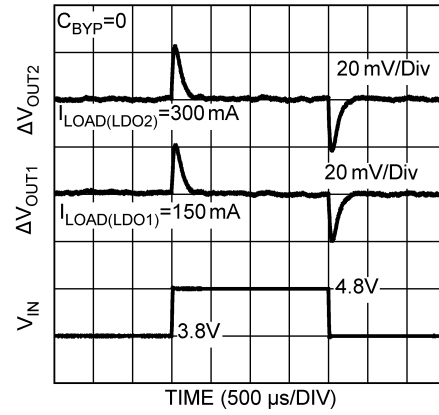
查询"LP3996D-0833"供应商

Line Transient,  $C_{BYP}=10nF$



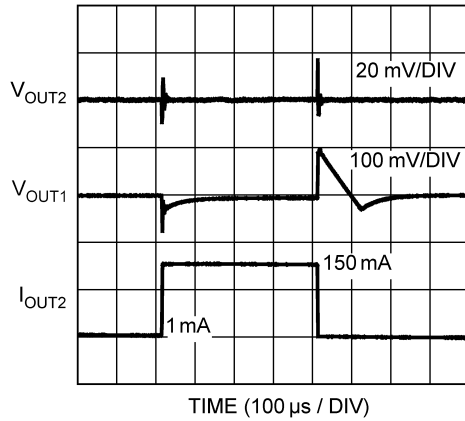
20145819

Line Transient,  $C_{BYP}=0$



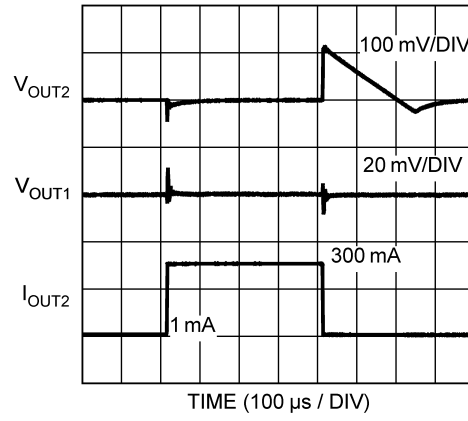
20145820

Load Transient, LDO1



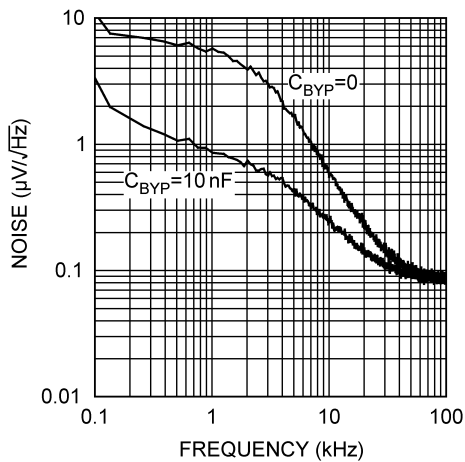
20145850

Load Transient, LDO2



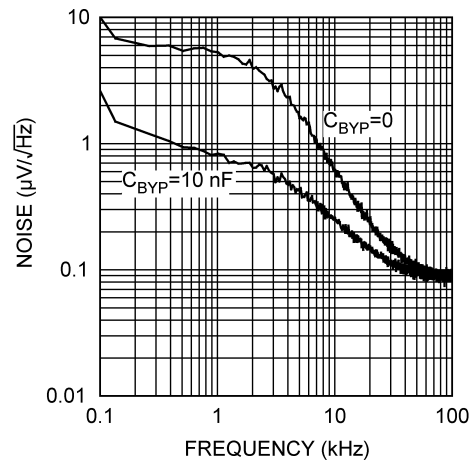
20145851

Noise Density LDO1



20145856

Noise Density, LDO2

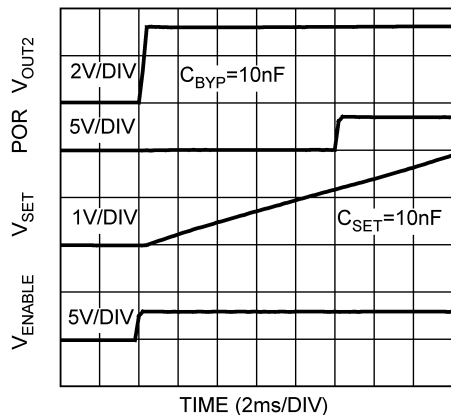


20145857

## Typical Performance Characteristics.

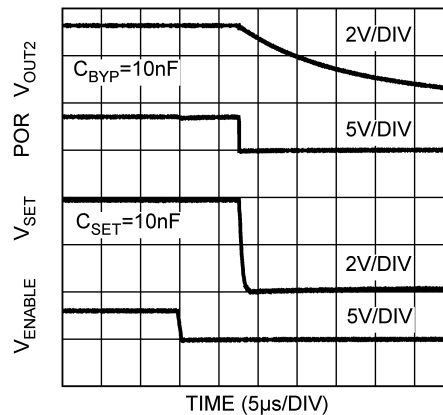
Unless otherwise specified,  $C_{IN} = 1.0\mu\text{F}$  Ceramic,  $C_{OUT1} = 1.0\mu\text{F}$  Ceramic,  $C_{BYP} = 10\text{nF}$ ,  $V_{IN} = V_{OUT2(NOM)} + 1.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT1(NOM)} = 3.3\text{V}$ ,  $V_{OUT2(NOM)} = 3.3\text{V}$ , Enable pins are tied to  $V_{IN}$ . (Continued)

Power-on-Reset Start-up Operation



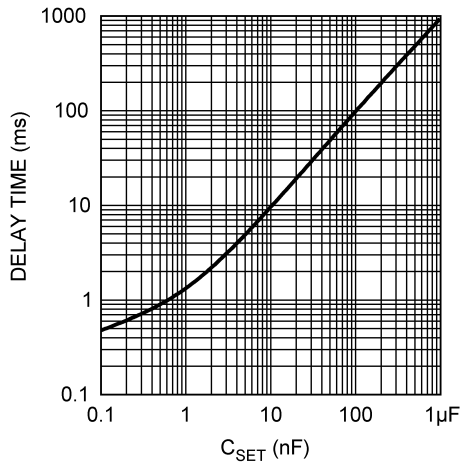
20145816

Power-on-Reset Shutdown Operation



20145817

POR Delay Time



20145818

## Application Hints

[查询"LP3996SD-0833"供应商](#)

### OPERATION DESCRIPTION

The LP3996 is a low quiescent current, power management IC, designed specifically for portable applications requiring minimum board space and smallest components. The LP3996 contains two independently selectable LDOs. The first is capable of sourcing 150mA at outputs between 0.8V and 3.3V. The second can source 300mA at an output voltage of 0.8V to 3.3V. In addition, LDO2 contains power good flag circuit, which monitors the output voltage and indicates when it is within 8% of its nominal value. The flag will also act as a power-on-reset signal and, by adding an external capacitor, a delay may be programmed for the POR output.

### INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0 $\mu$ F capacitor be connected between the LP3996 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

**Important:** Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0 $\mu$ F over the entire operating temperature range.

### OUTPUT CAPACITOR

The LP3996 is designed specifically to work with very small ceramic output capacitors. A 1.0 $\mu$ F ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5m $\Omega$  to 500m $\Omega$ , is suitable in the LP3996 application circuit.

For this device the output capacitor should be connected between the  $V_{OUT}$  pin and ground.

It is also possible to use tantalum or film capacitors at the device output,  $C_{OUT}$  (or  $V_{OUT}$ ), but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5m $\Omega$  to 500m $\Omega$  for stability.

### NO-LOAD STABILITY

The LP3996 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

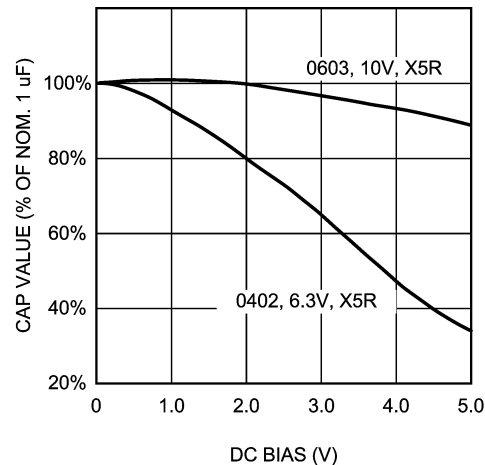
### CAPACITOR CHARACTERISTICS

The LP3996 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 $\mu$ F to 4.7 $\mu$ F, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating

high frequency noise. The ESR of a typical 1.0 $\mu$ F ceramic capacitor is in the range of 20m $\Omega$  to 40m $\Omega$ , which easily meets the ESR requirement for stability for the LP3996.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, *Figure 4* shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7 $\mu$ F in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.



**FIGURE 4. Graph Showing a Typical Variation in Capacitance vs DC Bias**

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within  $\pm 15\%$ . The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C. Many large value ceramic capacitors, larger than 1 $\mu$ F are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 $\mu$ F to 4.7 $\mu$ F range.

## Application Hints (Continued)

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

### ENABLE CONTROL

The LP3996 features active high enable pins for each regulator, EN1 and EN2, which turns the corresponding LDO off when pulled low. The device outputs are enabled when the enable lines are set to high. When not enabled the regulator output is off and the device typically consumes 2nA.

If the application does not require the Enable switching feature, one or both enable pins should be tied to  $V_{IN}$  to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the enable inputs must be able to swing above and below the specified turn-on / off voltage thresholds listed in the Electrical Characteristics section under  $V_{IL}$  and  $V_{IH}$ .

### POWER-ON-RESET

The POR pin is an open-drain output which will be set to Low whenever the output of LDO2 falls out of regulation to approximately 90% of its nominal value. An external pull-up resistor, connected to  $V_{OUT}$  or  $V_{IN}$ , is required on this pin. During start-up, or whenever a fault condition is removed, the POR flag will return to the High state after the output reaches approximately 96% of its nominal value. By connecting a capacitor from the SET pin to GND, a delay to the rising condition of the POR flag may be introduced. The delayed signal may then be used as a Power-on -Reset for a microprocessor within the user's application.

The duration of the delay is determined by the time to charge the delay capacitor to a threshold voltage of 1.25V at 1.2μA from the SET pin as in the formula below.

$$t_{\text{DELAY}} = \frac{V_{\text{TH(SET)}} \times C_{\text{SET}}}{I_{\text{SET}}}$$

20145841

A 0.1μF capacitor will introduce a delay of approximately 100ms.

### BYPASS CAPACITOR

The internal voltage reference circuit of the LP3996 is connected to the  $C_{\text{BYP}}$  pin via a high value internal resistor. An external capacitor, connected to this pin, forms a low-pass filter which reduces the noise level on both outputs of the device. There is also some improvement in PSSR and line transient performance. Internal circuitry ensures rapid charging of the  $C_{\text{BYP}}$  capacitor during start-up. A 10nF, high quality ceramic capacitor with either NPO or COG dielectric is recommended due to their low leakage characteristics and low noise performance.

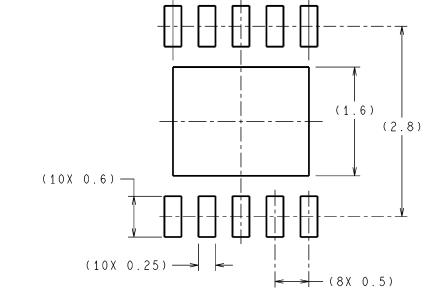
### SAFE AREA OF OPERATION

Due consideration should be given to operating conditions to avoid excessive thermal dissipation of the LP3996 or triggering its thermal shutdown circuit. When both outputs are enabled, the total power dissipation will be  $P_{\text{D(LDO1)}} + P_{\text{D(LDO2)}}$  Where  $P_{\text{D}} = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}}$  for each LDO.

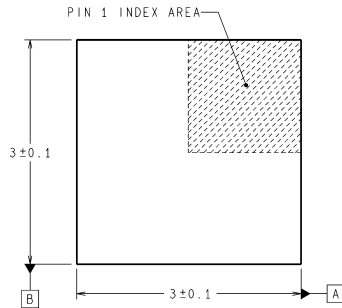
In general, device options which have a large difference in output voltage will dissipate more power when both outputs are enabled, due to the input voltage required for the higher output voltage LDO. In such cases, especially at elevated ambient temperature, it may not be possible to operate both outputs at maximum current at the same time.

# Physical Dimensions inches (millimeters) unless otherwise noted

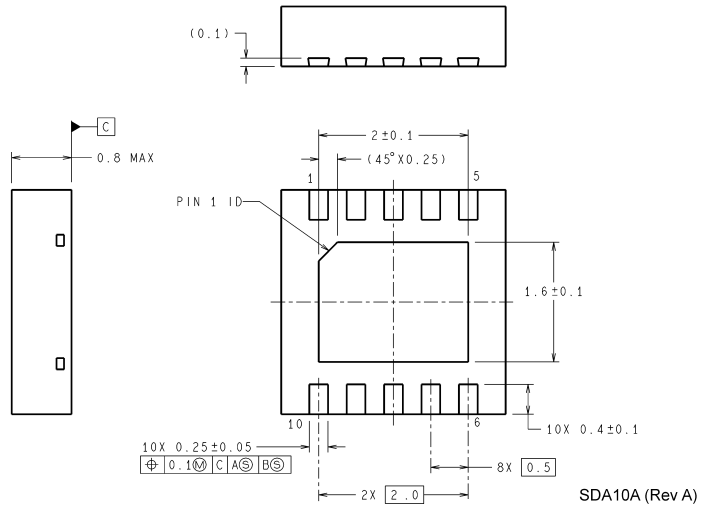
[查询"LP3996SD-0833"供应商](#)



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



LLP, 10 Lead, Package  
NS Package Number SDA10A

SDA10A (Rev A)

[查询"LP3996SD-0833"供应商](#)

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

#### LIFE SUPPORT POLICY

**NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION.** As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are trademarks or registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright © 2006 National Semiconductor Corporation.

For the most current product information visit us at [www.national.com](http://www.national.com).



**National Semiconductor**  
Americas Customer  
Support Center  
Email: [new.feedback@nsc.com](mailto:new.feedback@nsc.com)  
Tel: 1-800-272-9959

[www.national.com](http://www.national.com)

**National Semiconductor**  
Europe Customer Support Center  
Fax: +49 (0) 180-530 85 86  
Email: [europa.support@nsc.com](mailto:europa.support@nsc.com)  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor**  
Asia Pacific Customer  
Support Center  
Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

**National Semiconductor**  
Japan Customer Support Center  
Fax: 81-3-5639-7507  
Email: [jpn.feedback@nsc.com](mailto:jpn.feedback@nsc.com)  
Tel: 81-3-5639-7560