

REVISIONS

查询"5962-9071901MXA"供应商

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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REV STATUS OF SHEETS	REV																			
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	PREPARED BY Dan Wonnell	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444																	
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Sandra Rooney	MICROCIRCUIT, LINEAR, ARINC 429 BUFFER/RECEIVER, MULTI-CHANNEL, MONOLITHIC SILICON																	
	APPROVED BY Michael A. Frye																		
	DRAWING APPROVAL DATE 92-12-11	SIZE A	CAGE CODE 67268	5962-90719															
	REVISION LEVEL	SHEET	1	OF	18														

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5962-E568-92

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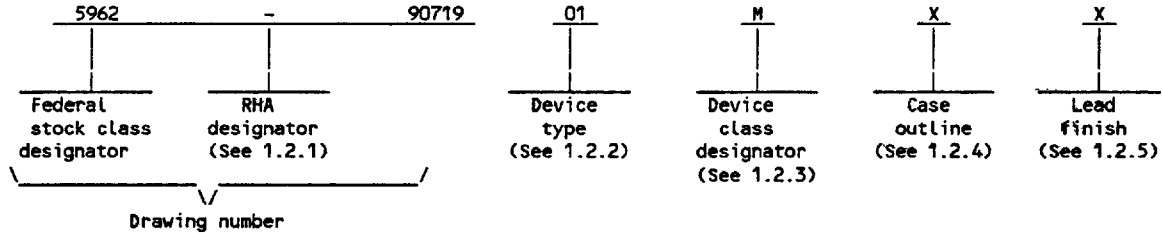
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1. SCOPE

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1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	EF4442	ARINC 429 multi-channel buffer/receiver 1/

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP2-T28 or GDIP1-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ This circuit was designed to be compatible with Aeronautical Radio, Inc., (ARINC), 429 of Mark 33 Digital Information Transfer System, (DITS), which defines the air transport industry's standards for the transfer of digital data between avionics systems elements.

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Supply voltage range (V_{CC}) -0.3 V dc to +7.0 V dc
 Storage temperature range -65°C to +150°C
 Power dissipation (P_D) 600 mW
 Lead temperature (soldering, 5 seconds) +270°C
 Thermal resistance, junction-to-case (θ_{JC}) See MIL-STD-1835
 Thermal resistance, junction-to-ambient (θ_{JA}) 50°C/W
 Junction temperature (T_J) +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) 4.5 V dc to 5.5 V dc
 High level input voltage, logic inputs (V_{IH}) 2.0 V dc to V_{CC}
 Low level input voltage, logic inputs (V_{IL}) GND to 0.8 V dc
 Minimum high level output voltage (V_{OH}) $V_{CC} - 0.75$ V dc
 Maximum low level output voltage (V_{OL}) 0.5 V dc
 Frequency of operation (f_{OP}) 2.0 MHz
 Case operating temperature range (T_C) -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

- MIL-M-38510 - Microcircuits, General Specification for.
- MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

- MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

- MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

- MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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3. REQUIREMENTS
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3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 107 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

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Table I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	NO-N1, DO-D7, I _{OH} = -250 μA	1,2,3	ALL	2.4	V _{CC}	V
		IRQ/V, I _{OH} = 10 μA	1,2,3	ALL		V _{CC}	V
Low level output voltage	V _{OL}	I _{OL} = 3.2 mA, V _{CC} = 4.5 V IRQ/V	1,2,3	ALL		0.4	V
		I _{OL} = 1.6 mA, V _{CC} = 4.5 V NO-N1, DO-D7	1,2,3	ALL		0.4	V
High impedance (off-state) output high current	I _{OHZ}	V _O = 2.4 V	1,2,3	ALL		10	μA
High impedance (off-state) output low current	I _{OLZ}	V _O = 0.4 V	1,2,3	ALL	-10		μA
High level input voltage	V _{IH}	ALL inputs except MODE and IRQ/V	1,2,3	ALL	2.2		V
Low level input voltage	V _{IL}	ALL inputs except MODE and IRQ/V	1,2,3	ALL		0.8	V
Supply current	I _{CC}	V _{CC} = 5.5 V	1,2,3	ALL		105	mA
Input state leakage current	I _{IN}	ALL inputs except MODE and IRQ/V V _{IN} = 0.4 V to 5.25 V	1,2,3	ALL	-10		μA
Three-state leakage current	I _{TSI}	NO-N1, DO-D7 V _{IN} = 0.4 V to 2.4 V	1,2,3	ALL	-10	+10	μA
Input capacitance	C _{IN}	V _{IN} = 0 V, f = 1.0 MHz, T _A = +25°C, see 4.4.1b, all inputs except MODE and IRQ/V	4	ALL		10	pF

See footnotes at end of table.

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TABLE Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External high programming impedance (MODE, IRQ/V) 2/	ZH	Scan frequency = f _{CLOCK} + 8, C _L ≤ 20 pF	4	ALL	10		kΩ
External low programming impedance (MODE, IRQ/V) 2/	ZL	Scan frequency = f _{CLOCK} + 8, C _L ≤ 20 pF	4	ALL		10	Ω
Functional tests	FT	See 4.4.1d	7,8A,8B	ALL			

READ A MODE TIMING CHARACTERISTICS

Address input hold time (AO-A1, RW/INH, CS)	t _{AH1}	See figure 3	9,10,11	ALL	10		ns
Data access time (D0-D7)	t _{ACC1}		9,10,11	ALL		300	ns
Data output hold time (D0-D7)	t _{DH1}		9,10,11	ALL	50		ns

WRITE A MODE TIMING CHARACTERISTICS

Address input setup time (AO-A1, RW/INH, CS)	t _{AS1}	See figure 3	9,10,11	ALL	50		ns
Address input hold time (AO-A1, RW/INH, CS)	t _{AH2}		9,10,11	ALL	10		ns
Data input setup time (D0-D7)	t _{DS}		9,10,11	ALL	100		ns
Data input hold time (D0-D7)	t _{DH2}		9,10,11	ALL	30		ns

See footnotes at end of table.

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TABLE I Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ B MODE TIMING CHARACTERISTICS							
Address setup time (AO-A1, CS, RW/INH)	t _{AS2}	See figure 3	9,10,11	ALL	50		ns
Address input hold time (AO-A1, CS, RW/INH)	t _{AH3}		9,10,11	ALL	10		ns
Data output hold time (NO-N1, DO-D7)	t _{DH3}		9,10,11	ALL	10		ns
Data access time (NO-N1, DO-D7)	t _{ACC2}		9,10,11	ALL		300	ns
RW/INH setup time	t _{SI}		9,10,11	ALL	50		ns
CLOCK TIMING CHARACTERISTICS							
A-mode cycle time	t _{CA}	See figure 3	9,10,11	ALL	500	2000	ns
B-mode cycle time	t _{CB}		9,10,11	ALL	1000	2000	ns
Pulse width - high	t _{WH}		9,10,11	ALL	180	2000	ns
Pulse width - low	t _{WL}		9,10,11	ALL	180	2000	ns
IRQ/V OUTPUT TIMING CHARACTERISTICS							
Propagation delay time, low to high	t _{PLH}	See figure 3	9,10,11	ALL		1600	ns
Propagation delay time, high to low	t _{PHL}		9,10,11	ALL		1000	ns
1/ 4.5 V ≤ V _{CC} ≤ 5.5 V and V _{SS} = 0 V, unless otherwise specified. 2/ If not tested, shall be guaranteed to the limits specified in table I.							
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Case outline	X	Case outline	X
Device type	ALL	Device type	ALL
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V _{SS}	15	D3
2	R \bar{W} /INH	16	D2
3	NO	17	D1
4	N1	18	D0
5	\bar{CS}	19	L0
6	A0	20	H0
7	A1	21	L1
8	\bar{RESET}	22	H1
9	e	23	L2
10	D7	24	H2
11	D6	25	L3
12	D5	26	H3
13	D4	27	$\bar{IRQ/V}$
14	V _{CC}	28	MODE

FIGURE 1. Terminal connections.

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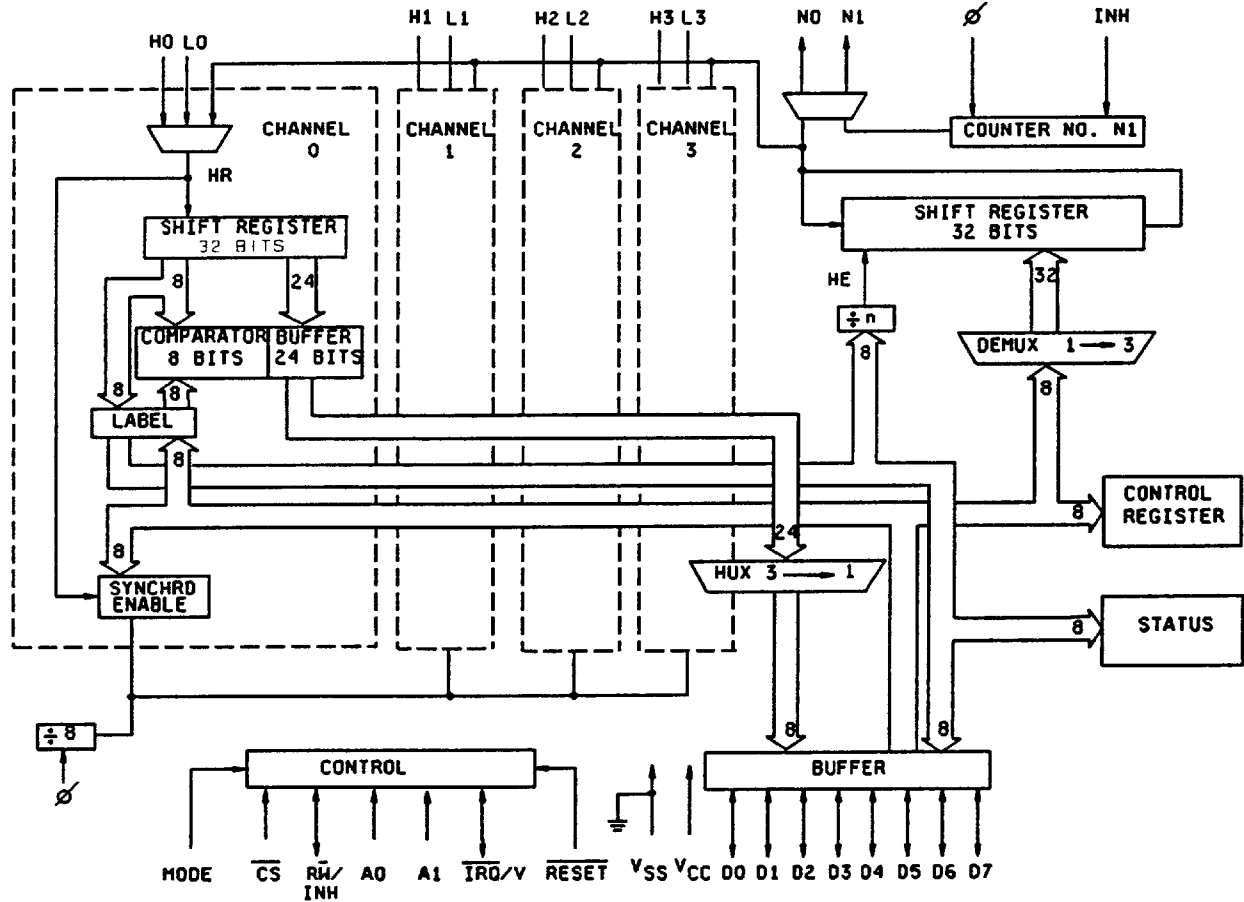


FIGURE 2. Logic diagram.

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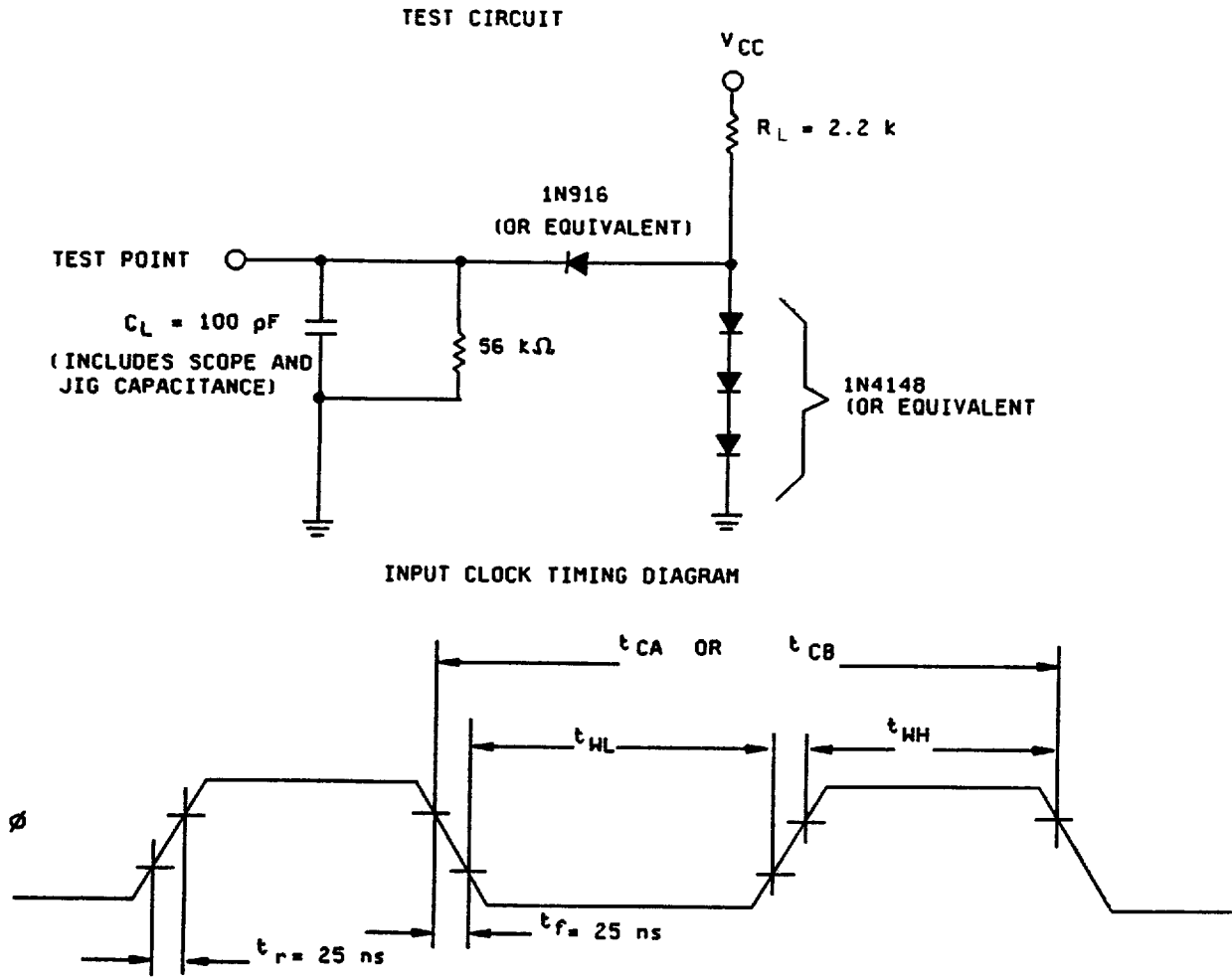
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NOTE: All timing measurement reference levels are 2.3 V and 0.5 V.

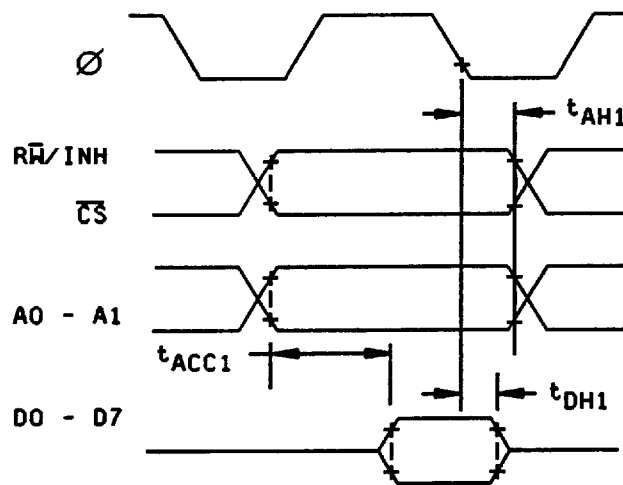
FIGURE 3. Switching times test circuit and waveforms.

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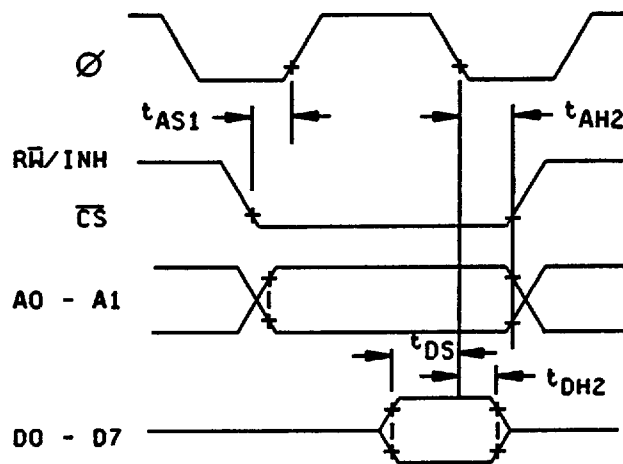
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READ A MODE TIMING DIAGRAM



WRITE A MODE TIMING DIAGRAM



NOTE: All timing measurement reference levels are 2.3 V and 0.5 V.

FIGURE 3. Switching times test circuit and waveforms - Continued.

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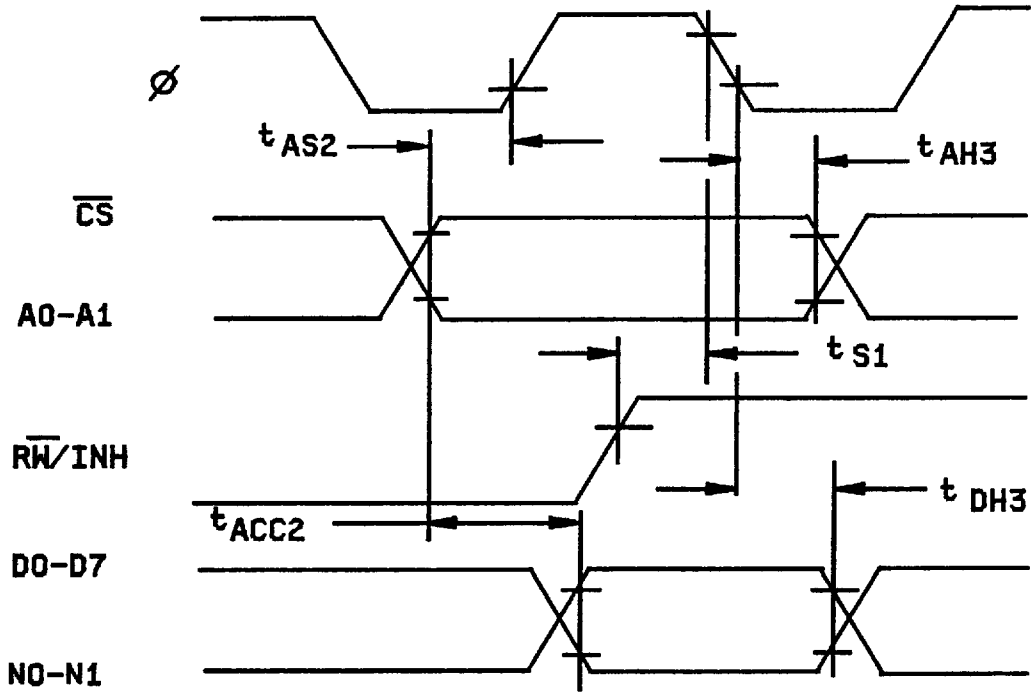
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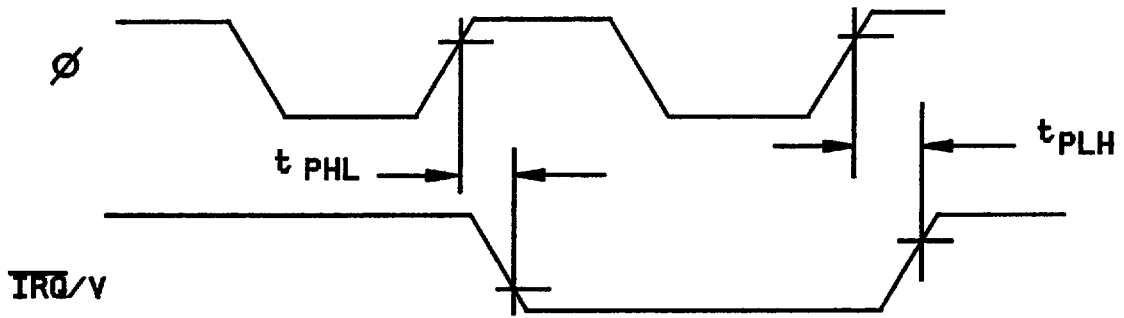
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READ B MODE TIMING DIAGRAM



\overline{IRQ}/V OUTPUT TIMING DIAGRAM



NOTE: All timing measurement reference levels are 2.3 V and 0.5 V.

FIGURE 3. Switching times test circuit and waveforms - Continued.

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4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D, or E. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7	1,7	1,7	1,7	1,7
Final electrical parameters (see 4.2)	1,2,3,7, 8A,8B,9, 10,11 <u>1/</u>	1,2,3,7, 8A,8B,9, 10,11 <u>2/</u>	1,2,3,7, 8A,8B,9, 10,11 <u>2/</u>	1,2,3,7, 8A,8B,9, 10,11 <u>1/</u>	1,2,3,7, 8A,8B,9, 10,11 <u>1/</u>
Group A test requirements (see 4.4)	1,2,3,4, 7,8A,8B, 9,10,11	1,2,3,4, 7,8A,8B, 9,10,11	1,2,3,4, 7,8A,8B, 9,10,11	1,2,3,4, 7,8A,8B, 9,10,11	1,2,3,4, 7,8A,8B, 9,10,11
Group B end-point electrical parameters (see 4.4)	---	---	2,8A,10	---	---
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	---	2,8A,10	2,8A,10
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10	2,8A,10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroup 4 (C_{IN} measurement) shall be measured initially and after process or design changes which may affect input capacitance. Sample size is 15 devices with no failures, and all input terminals tested.
- c. Subgroups 7 and 8 functional testing shall include verification of instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, D, or E. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

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c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

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TABLE III. Pin functions.

Terminal symbol	Terminal number	Function
V _{SS}	1	This pin is connected to the negative side of the power supply (ground).
RW/INH	2	This input selects the direction of transfer (write or read) of data between the circuit and the microprocessor when the circuit is programmed in mode A (pin 28). In mode B, this input is used to disable the channel scanning divide by 4 counter.
NO	3	In A mode, this output has a transmit function. The signal corresponding to the result of ANDing the ARINC transmit clock and the complemented output signal of the transmit shift register (logic "0" clock output) is available on this pin. In B mode, the value of the least significant bit of the address of the scanned channel is available on this pin.
N1	4	In A mode, this output has a transmit function. The signal corresponding to the result of ANDing the ARINC transmit clock and the output signal of the transmit shift register (logic "1" clock output) is available on this pin. In B mode, the value of the most significant bit of the address of the scanned channel is available on this pin.
CS	5	In A mode, this input (active when low) selects the chip for a microprocessor access.
A0	6	In A mode, this input corresponds to the least significant bit of the circuit function address. In B mode, this input corresponds to the least significant bit of the data byte in the message.
A1	7	In A mode, this input corresponds to the most significant bit of the circuit function address. In B mode, this input corresponds to the most significant bit of the address of the data byte in the message.
RESET	8	This input (active when low) initializes the circuit by resetting certain registers.
ø	9	This input receives the clock signal from the circuit which corresponds to phase ø2 of the microprocessor clock.
D7	10	This three-state input/output is connected to the eighth line of the data bus.

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Terminal symbol	Terminal number	Function
D6	11	This three-state input/output is connected to the seventh line of the data bus.
D5	12	This three-state input/output is connected to the sixth line of the data bus.
D4	13	This three-state input/output is connected to the fifth line of the data bus.
V _{CC}	14	This pin is connected to the positive side of the power supply (+5 V).
D3	15	This three-state input/output is connected to the fourth line of the data bus.
D2	16	This three-state input/output is connected to the third line of the data bus.
D1	17	This three-state input/output is connected to the second line of the data bus.
D0	18	This three-state input/output is connected to the first line of the data bus.
L0	19	This input receives the logic "0" clock from the signal shaping/separation subsystem of the first ARINC channel.
H0	20	This input receives the logic "1" clock from the signal shaping/separation subsystem of the first ARINC channel.
L1	21	This input receives the logic "0" clock from the signal shaping/separation subsystem of the second ARINC channel.
H1	22	This input receives the logic "1" clock from the signal shaping/separation subsystem of the second ARINC channel.
L2	23	This input receives the logic "0" clock from the signal shaping/separation subsystem of the third ARINC channel.
H2	24	This input receives the logic "1" clock from the signal shaping/separation subsystem of the third ARINC channel.
L3	25	This input receives the logic "0" clock from the signal shaping/separation subsystem of the fourth ARINC channel.
H3	26	This input receives the logic "1" clock from the signal shaping/separation subsystem of the fourth ARINC channel.

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TABLE III. Pin functions - Continued.

Terminal symbol	Terminal number	Function
$\overline{\text{IRQ/V}}$	27	In A mode, this pin (active when low) constitutes an open drain output delivering the signal for interrupting the microprocessor. In B mode, this pin is an input used to program the number of high speed channels.
Mode	28	This input is used to program the operating mode (A or B) of the circuit and also to enable or disable the parity check.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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