OKI Semiconductor
This version: Jan. 1998
Previous version: Nov. 1996

MSM6948/6948V

1200 bps Single Chip MSK Modem

GENERAL DESCRIPTION

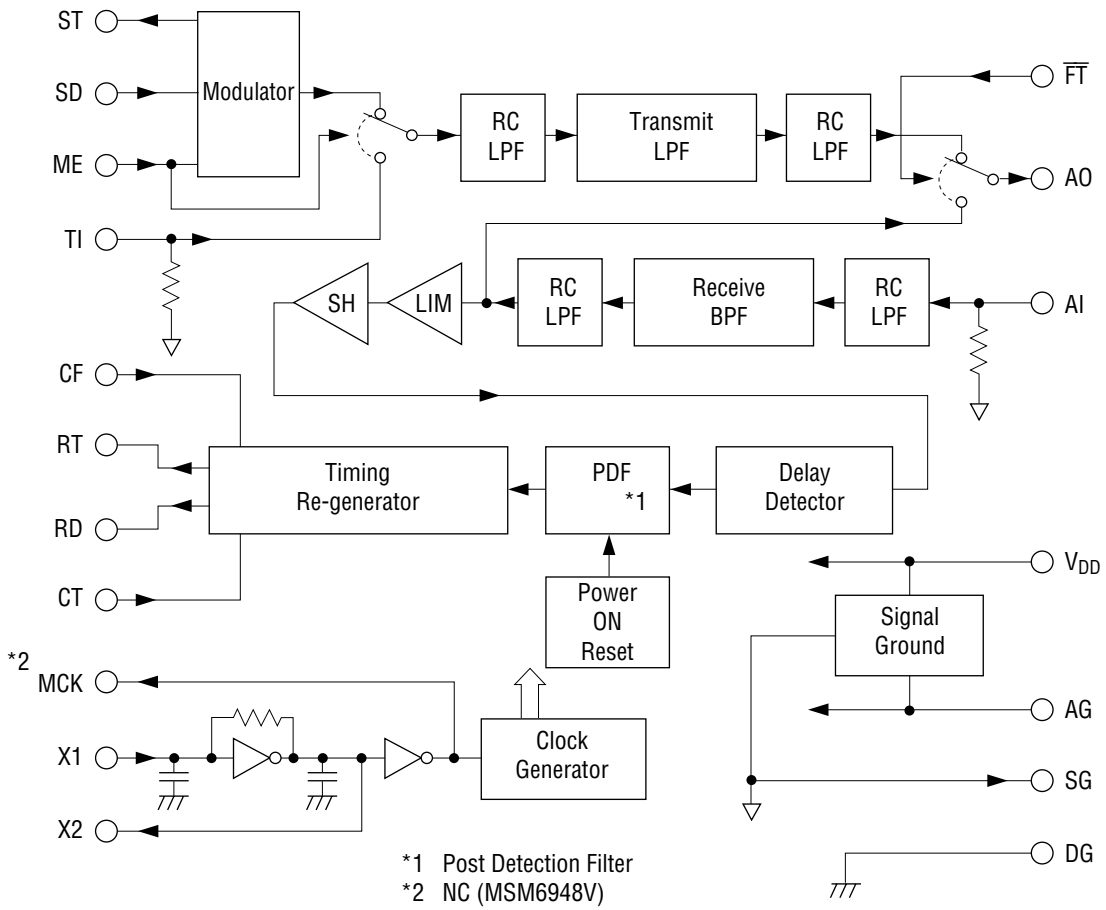
The MSM6948/6948V is a single chip MSK (Minimum Shift Keying) modem which is fabricated by Oki's low power consumption CMOS silicon gate technology.
The demodulator receives the data to be transmitted (SD) synchronized with the transmit timing clock (ST) generated by the on-chip clock generator. The signal, which is modulated by MSK method, is output.
The demodulator converts the received MSK signal to the received data (RD) by means of a delay detection technique after limiting the band of the received MSK signal. This signal is input to the digital PLL and the re-generated timing clock (RT) is output from the demodulator, synchronized with the RD.

FEATURES

- Signal power supply: +5 V
- On-chip SCF (Switched Capacitor Filter)
- The transmit filter can be also used as voice splatter filter.
- The receive timing re-generator has two different lock-in time performance options to be chosen from.
- Built-in crystal oscillation circuit.
- Small number of external components for easy application.
- Wide application-wireless data equipment, MCA system.
- Low power consumption CMOS.
- Package options:

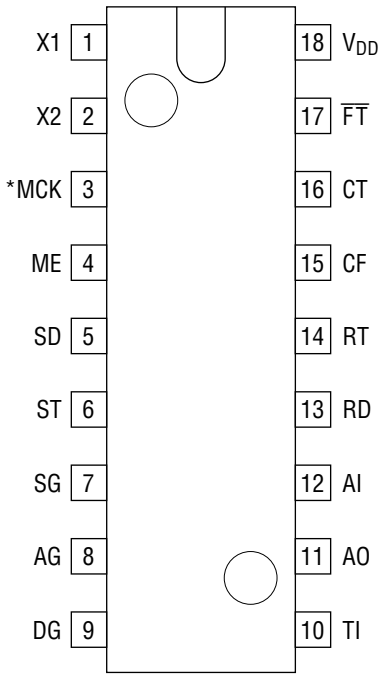
18-pin plastic DIP	(DIP18-P-300-2.54)	(Product name: MSM6948RS)
24-pin plastic SOP	(SOP24-P-430-1.27-K)	(Product name: MSM6948GS-K)

BLOCK DIAGRAM

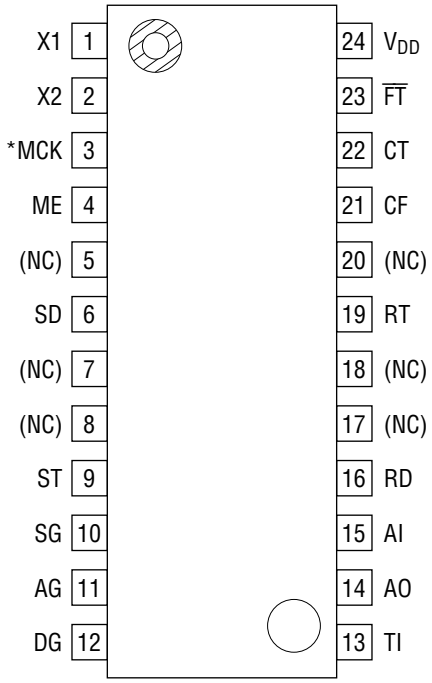


*1 Post Detection Filter
*2 NC (MSM6948V)

PIN CONFIGURATION (TOP VIEW)



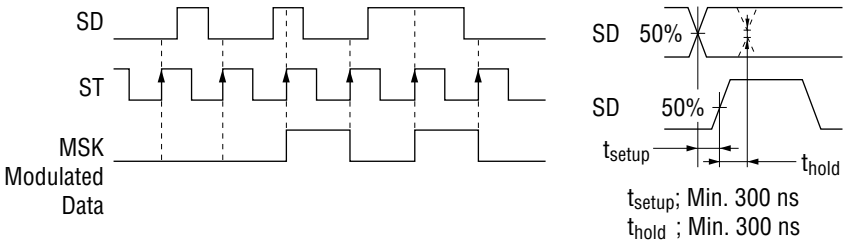
18-Pin Plastic DIP



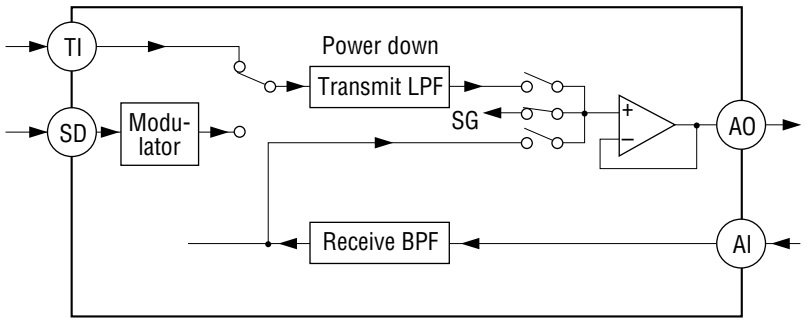
24-Pin Plastic SOP

*NC (MSM6948V)
NC : No connect pin

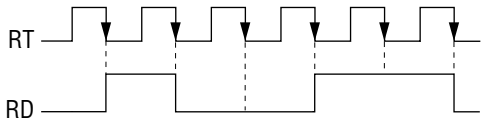
PIN DESCRIPTION

Name	Description
X1	Crystal connection pins. A 3.6864 MHz crystal shall be connected. When an external clock is applied for MSM6948's oscillation source, it has to be input to X2. In this case, X2 has to be AC-coupled by the capacitor of 200 pF. X1 shall be left open.
X2	
*MCK	3.6864 MHz ±0.02% clock output. This can be used for other devices under limited load conditions.
ME	When digital "1" is put on this pin, MSK modulator output is connected to the input of transmit LPF. When digital "0" is put on, the input of transmit LPF is connected to TI that is voice signal input. The data put on ME terminal is synchronized with the rising edge of ST and input to internal logic as a control data. The rising edge of this synchronized data resets MSK modulator.
SD	Transmit data input. The data on this pin is synchronized with the rising edge of ST and input to MSK modulator as an actual transmit data.  t_{setup}; Min. 300 ns t_{hold} ; Min. 300 ns
ST	ST is synchronizing signal used for ME and SD. This is made from master clock and is usually 1200 Hz.
SG	Built-in analog signal ground. The DC voltage is approximately half of V_{DD}, so the analog signals of AI, AO, and TI interfaces with peripheral circuits which must be implemented by AC-coupling. To make this voltage source impedance lower and ensure the device performance, it is necessary to put a bypass capacitor on SG in close physical proximity to the device.
AG	Analog ground. This pin should be common with DG at the system ground point as close as possible.

*NC : MSM6948V

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>DG</td><td>Digital ground.
This pin should be common with AG at the system ground point as close as possible.</td></tr>
<tr><td>TI</td><td>Voice signal input.
The signal input to this pin can be sent out to AO through the transmit LPF, the characteristics of which, gives the splatter filter for voice band signal.
When this function is used, digital "0" must be input to ME.
TI is biased internally to SG with about 100 kΩ.</td></tr>
<tr><td>AO</td><td>Transmit analog signal output.
According to the control data on ME and $\overline{FT}$, AO is set to various state as an output terminal as follows.
<table>
<tr><th>$\overline{FT}$</th><th>ME</th><th>Transmit LPF</th><th colspan="2">State of AO</th></tr>
<tr><td>"1"</td><td>"1"</td><td rowspan="2">Power On</td><td rowspan="2">The output of Transmit LPF</td><td>MSK Signal</td></tr>
<tr><td>"1"</td><td>"0"</td><td>Voice Signal</td></tr>
<tr><td>"0"</td><td>"1"</td><td rowspan="2">Power Down</td><td colspan="2">The Output of Receive BPF
(Used for Device Test Only)</td></tr>
<tr><td>"0"</td><td>"0"</td><td colspan="2">No-signal Output
(DC-biased to SG)</td></tr>
</table>


The state when $\overline{FT}$ and ME = "0" is shown above. When the input digital data on $\overline{FT}$ changes to "1" from "0", AO remains to be connected to SG during about 12 ms and after that, and AO is switched to transmit LPF.
This delay time prevents AO from outputting meaningless signal during transient time from power down to on of LPF.</td></tr>
<tr><td>AI</td><td>Receive analog signal input.
AI is biased internally to SG with about 100 kΩ same as TI. Receive BPF and demodulator extract the information in this signal and convert it into a serial data stream at RD output.</td></tr>
</table>

Name	Description
RD	Demodulated serial data output. This data is synchronized with the re-generated timing clock RT.
RT	Receive data timing clock output. This signal is re-generated by internal digital PLL. Synchronizing to falling edge of RT, RD is output.  Delay time (RT → RD) < 300 ns
CF	Receive data timing clock is re-generated by digital PLL of which phase correcting speed can be selected with CF. When a digital "1" is put on CF and phase difference between receive data timing and RT is more than 22.5 degree, phase correcting speed is high. In this case, as the phase difference enters within 22.5 degrees, that speed changes to low immediately. When digital "0" is input to CF, phase correcting speed of PLL remains low regardless of the phase difference. Usually, CF is connected to digital "1".
CT	PLL's lock-in characteristics can be selected with CT. When digital "1" is put on CT, PLL requires max. 50-bit alternative data pattern. On the other hand, when digital "0" is input to CT, PLL can be locked in below 18-bit data. Equipment / CT: Personal/MCA wireless terminals / "1"; MCA wireless bases / "0"
$\overline{FT}$	Control signal for the internal connection of AO. Refer to column AO. When digital "0" is input to this pin, transmit LPF enters in power down mode, but the output buffer operational amplifier remains active.
V_{DD}	+5 V power supply. This device is sensitive to supply noises as switched capacitor techniques are utilized. Bypass capacitors of more than 2.2 µF between V_{DD} and AG, and between V_{DD} and DG are indispensable to ensure the performance.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C With respect to AG and DG	–0.3 to 7.0	V
Analog Input Voltage *1	V_{IA}		–0.3 to V_{DD} + 0.3	
Digital Input Voltage *2	V_{ID}		–0.3 to V_{DD} + 0.3	
Operating Temperature	T_{op}	—	–25 to 70	°C
Storage Temperature	T_{STG}	—	–55 to 150	

*1 TI, AI
*2 ME, SD, CF, CT, $\overline{FT}$

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage		V_{DD}	With respect to AG and DG	4.75	5	5.25	V
		AG, DG	—	—	0	—	
Operating Temperature		T_{op}	—	–25	25	70	°C
Crystal Resonant Frequency		$f_{X'TAL}$	—	3.6860	3.6864	3.6868	MHz
Data Speed		T_S	—	—	1200	—	bit/sec
C1		—	—	—	2.2	—	µF
C2, C6		—	—	—	0.1	—	
C3		—	—	—	0.047	—	
C4		—	$R_{LX} \geq 100$ kΩ	—	0.01	—	
C5		—	—	—	0.047	—	
Crystal	Frequency Deviation	—	25 ±5°C	–100	—	+100	ppm
	Temperature Characteristics	—	At –40°C to +85°C	–100	—	+100	
	Equivalent Series Resistance	—	—	—	—	100	Ω
	Load Capacitance	—	—	—	16	—	pF

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 5 V ±5%, Ta = –25°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD}	Normal Operating Mode	—	3	6	mA
Oscilating Frequency	f_{MCK}	$f_{X'TAL}$ = 3.6864 MHz ±0.01%	3.6857	3.6864	3.6871	MHz
Input Leakage Current *1	I_{IL}	V_{IN} = 0 V	–10	—	10	µA
	I_{IH}	V_{IN} = V_{DD}	–10	—	10	
Input Voltage *1	V_{IL}	—	0	—	0.8	V
	V_{IH}	—	2.2	—	V_{DD}	
Output Voltage *2	V_{OL1}	I_{OL} = 1.6 mA	0	—	0.4	
	V_{OH1}	I_{OH} = 400 µA	0.8V_{DD}	—	V_{DD}	
Output Voltage *3	V_{OL2}	R_L > 50 kΩ C_L < 20 pF	0	—	0.4	
	V_{OH2}		0.6V_{DD}	—	V_{DD}	

*1 ME, SD, CF, CT, $\overline{FT}$
*2 ST, RD, RT
*3 MCK (NC : MSM6948V)

Analog Interface Characteristics

Transmit signal output (AO)

(V_{DD} = 5.0 V ±5%, Ta = –25°C to 70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Carrier Frequency	f_M	SD = "1"	$\overline{FT}$ = "1" ME = "1"	1199	1200	1201	Hz
	f_S	SD = "0"		1799	1800	1801	
Carrier Level	V_{OX}	$R_L \geq 100$ kΩ $C_L \leq 40$ pF	$\overline{FT}$ = "1" ME = "1"	–2	0	+2	dBm
Output Resistance	R_{OX}	$f_{AO} \leq 4$ kHz		—	—	1	kΩ
Output Load Resistance	R_{LX}	—		100	—	—	
Output Load Capacitance	C_{LX}	—		—	—	40	pF
Output DC Voltage	V_{OSX}	—		$\frac{V_{DD}}{2}$ – 0.1	$\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2}$ + 0.1	V

Note 0 dBm = 0.775 Vrms

Voice signal input (TI)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Voltage Gain	GT	V_{AO}/V_{TI}	$\overline{FT}$ = "1" ME = "0"	–2	0	+2	dB
Input Signal Level	V_{TI}	—		—	—	0	dBm
Input Resistance	R_{TI}	$f_{TI} \leq 4$ kHz		50	—	—	kΩ

Built-in signal ground (SG)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DC Voltage	V_{SG}	Without DC Load	$\frac{V_{DD}}{2} - 0.1$	$\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2} + 0.1$	V

Receive signal input (AI)

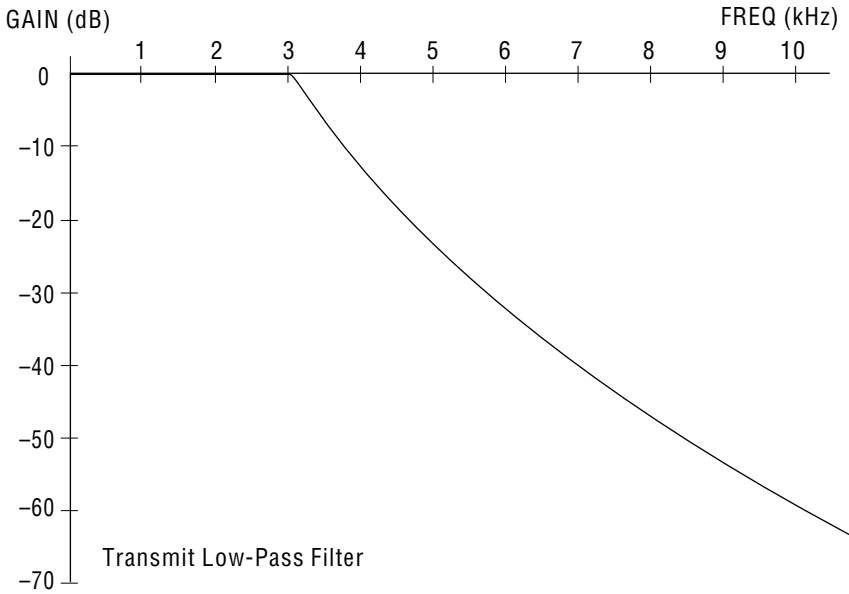
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{IR}	$f_{TI} \leq 4$ kHz		50	—	—	kΩ
Receive Signal Level	V_{IR}	—		–30	—	0	dBm
Bit Error Rate	BER	S/N at AI	8 dB	—	1×10^{-3}	—	N/N
			10 dB	—	5×10^{-5}	—	

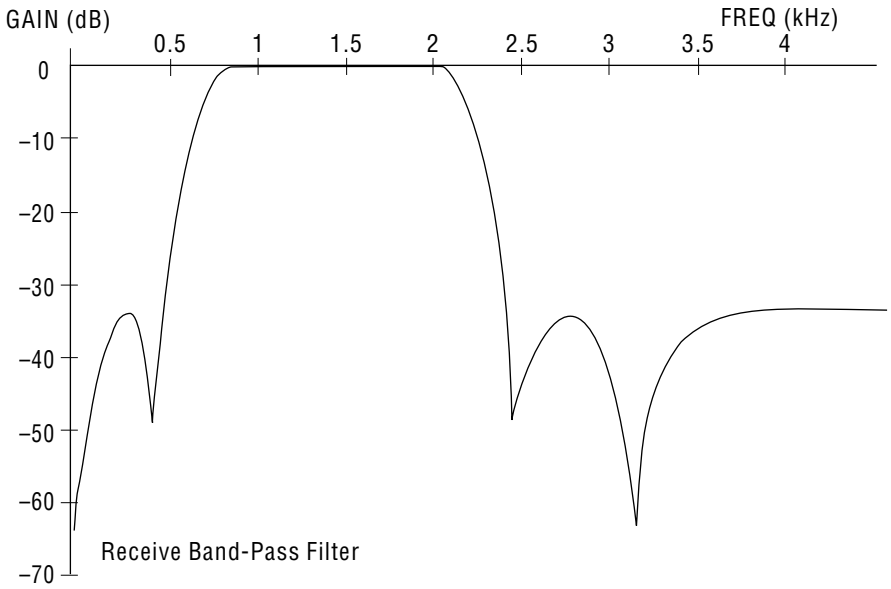
Re-generated receive data timing clock output (RT)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
Data Bit Number for PLL' Lock-in	N_{PLL1}	CF = "1"	CT= "0"	*1	—	—	18	bit
	N_{PLL2}		CT= "1"		—	—	50	

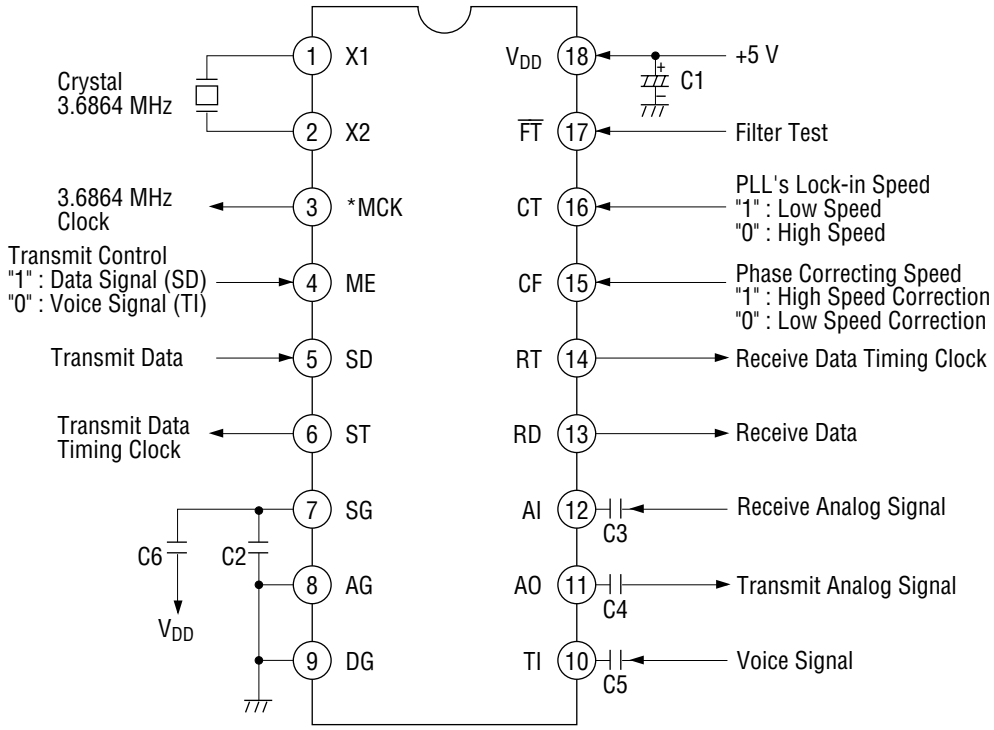
*1 Data bit number to lock-in within 22.5 degree

BUILT-IN FILTER FREQUENCY CHARACTERISTICS





APPLICATION CIRCUIT

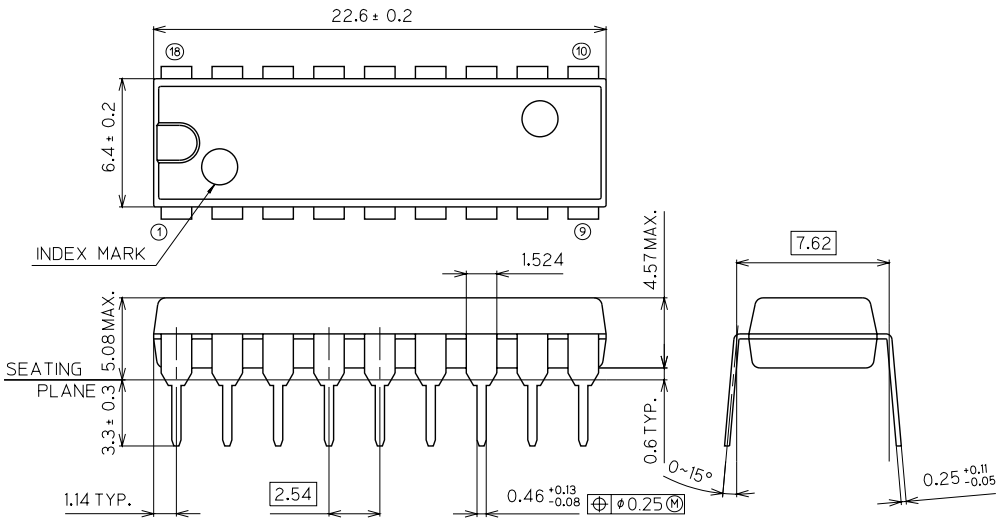


*NC : MSM6948V

PACKAGE DIMENSIONS

(Unit : mm)

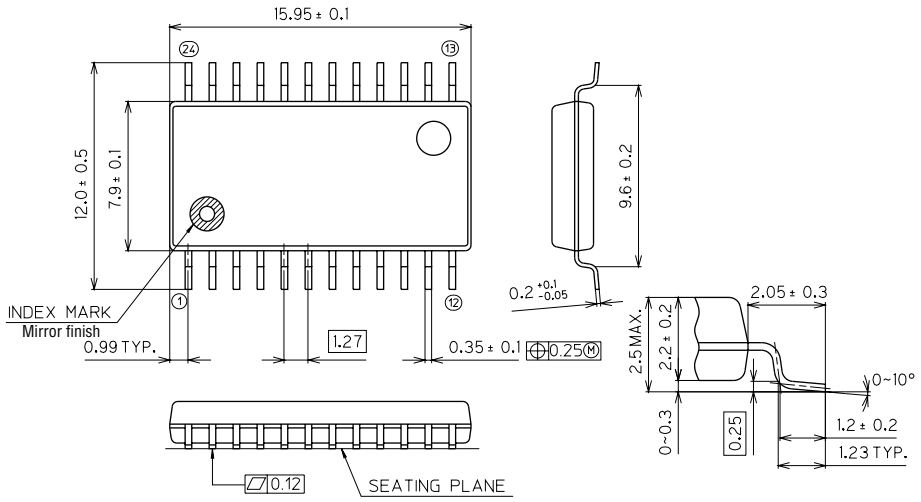
DIP18-P-300-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.30 TYP.

(Unit : mm)

SOP24-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).