YM6063B

CD-I Data Controller(CDC)

■ OUTLINE

The CDC (CD-I Data Controller) is a data processor capable of handling data from both CD-I and CD-ROM sources.
This receives data read out from a CD-I disk and detects the synchronous pattern, then descrambles the data and puts it in a buffer. File and channel selection, and data distribution can be done through use of an 8 bit microcomputer.
It is also possible to create a compact CD-I system configuration by using this together with the YM6064 (ADP) and YM7302 (MPC).

■ FEATURES

- Capacity to handle either CD-I or CD-ROM.
- Real time errors can be detected and corrected by the hardware.
- Interface can be accomplished with any CD audio signal processing format, regardless of the maker--e.g. Yamaha, Sony, Sanyo, NEC, Mitsubishi, Toshiba, Hitachi, or Matsushita.
- CD-I ADPCM data can be transferred directly to the audio processor (ADP).
- When used with the YM7302 (MPC), data can be transferred at a rate of 1170 bytes/msec.
- An optimal system can be set up when connected with a 68000- type bus.
- CMOS, 5V power supply, 80 PIN QFP

YAMAHA CORPORATION

YM6063B CATALOG
CATALOG No.:LSI-2160633
1992. 3

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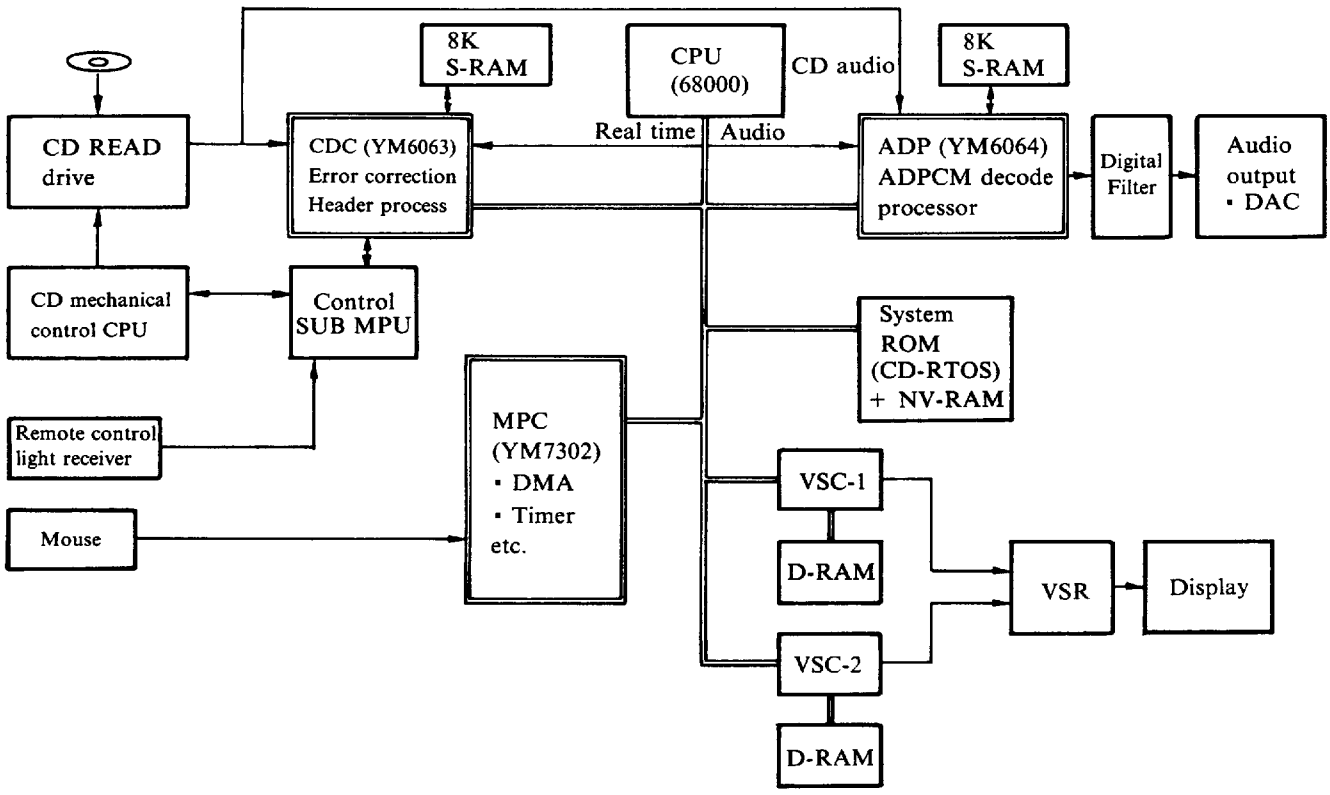
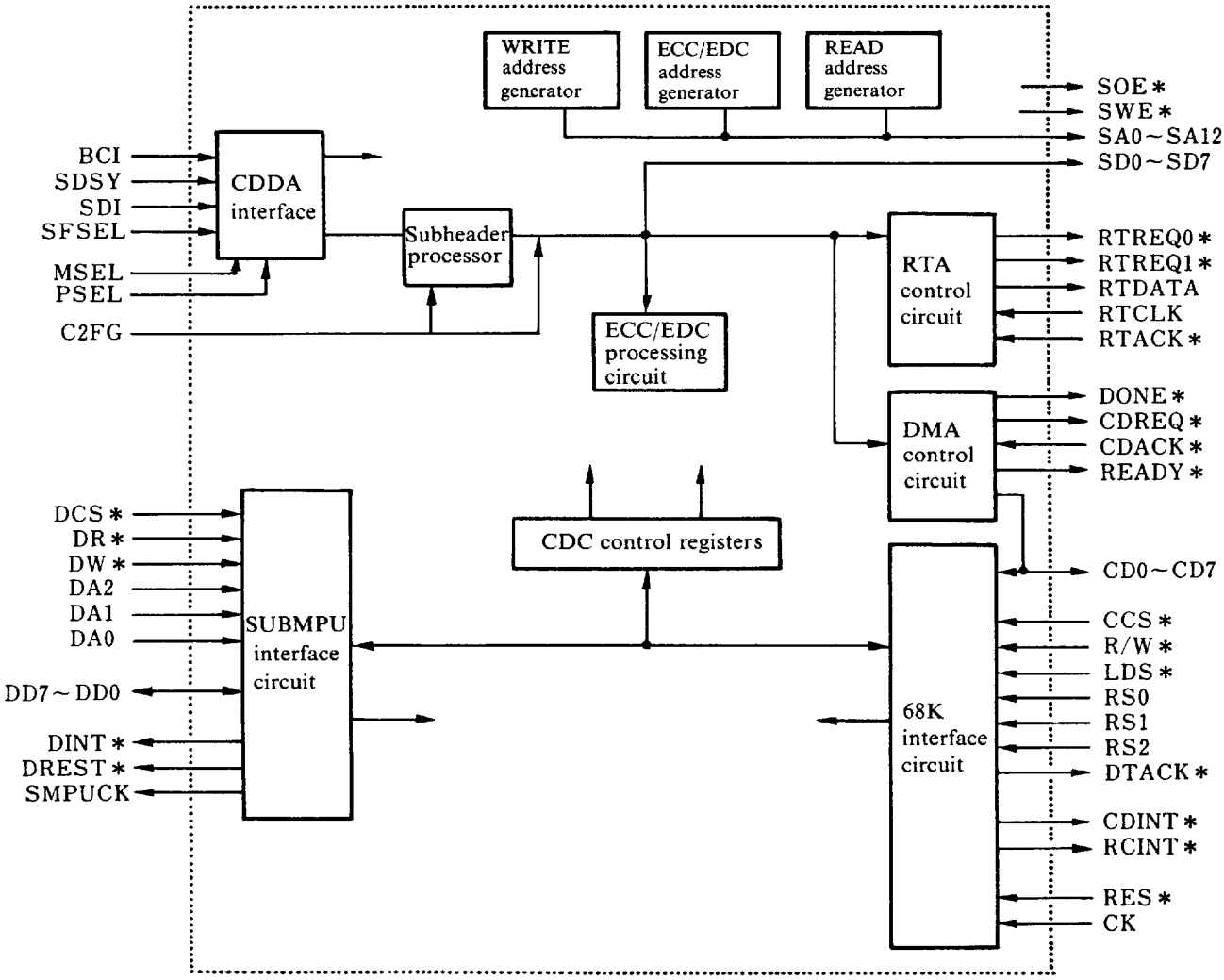
■ SAMPLE CD-I CONFIGURATION

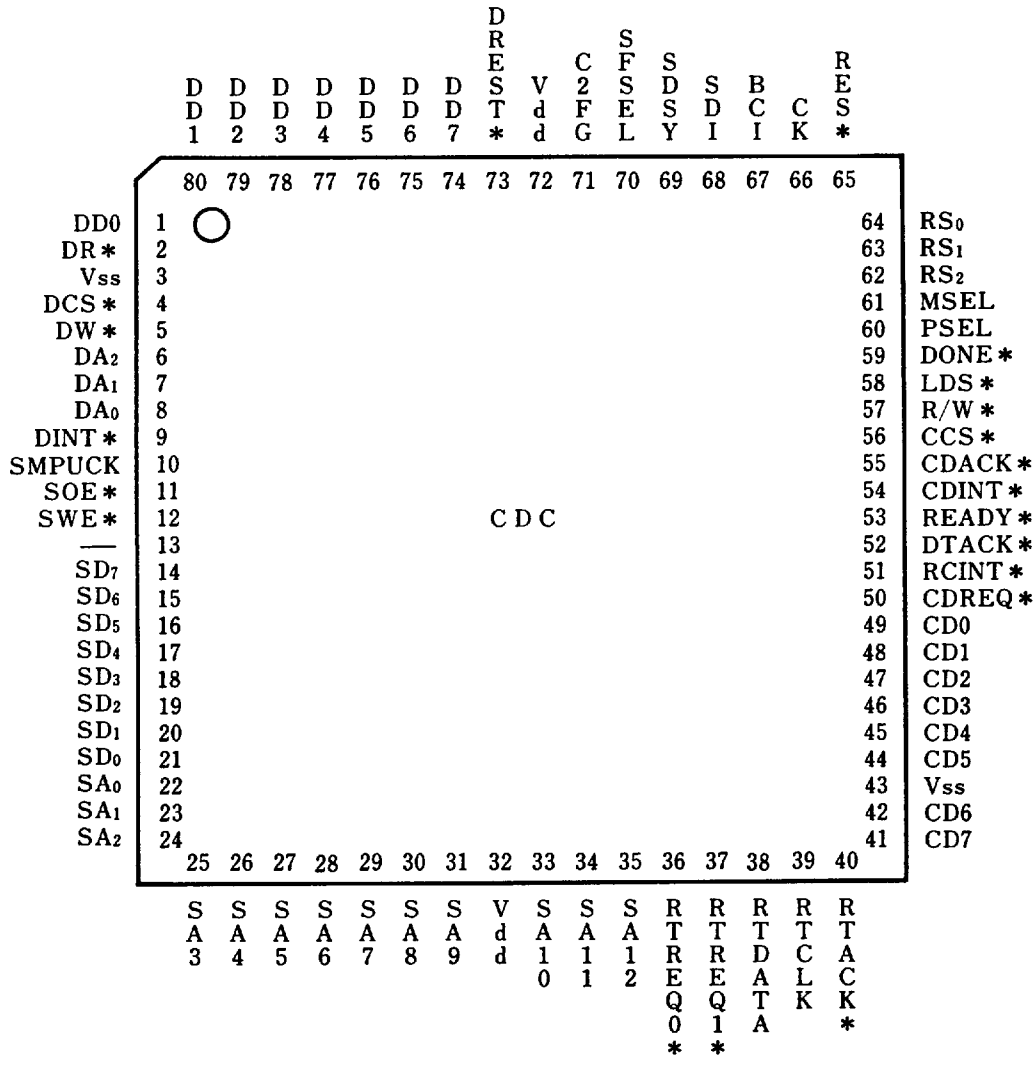


■ BLOCK DIAGRAM



(*indicates a terminal which is active when low.)

■ TERMINAL ASSIGNMENTS



■ TERMINAL FUNCTIONS

Pin number	Pin name	I/O	DT	Pin function
1	DD_0	I/O	TS	Sub-MPU data bus Do
2	DR *	I		Read data strobe for sub-MPU
3	V_{SS}			
4	DCS *	I		Chip select for sub-MPU
5	DW *	I		Write data strobe for sub-MPU
6	DA_2	I		Register select for sub-MPU
7	DA_1	I		Register select for sub-MPU
8	DA_0	I		Register select for sub-MPU
9	DINT *	O	OD	Interrupt request to sub-MPU
10	SMPUCK	O		4 MHz CK/2 clock output
11	SOE *	O		Output enable for S RAM
12	SWE *	O		Write enable for S RAM
13				
14	SD_7	I/O	TS	S RAM data bus
15	SD_6	I/O	TS	S RAM data bus
16	SD_5	I/O	TS	S RAM data bus
17	SD_4	I/O	TS	S RAM data bus
18	SD_3	I/O	TS	S RAM data bus
19	SD_2	I/O	TS	S RAM data bus
20	SD_1	I/O	TS	S RAM data bus
21	SD_0	I/O	TS	S RAM data bus
22	SA_0	O		S RAM address bus
23	SA_1	O		S RAM address bus
24	SA_2	O		S RAM address bus
25	SA_3	O		S RAM address bus
26	SA_4	O		S RAM address bus
27	SA_5	O		S RAM address bus
28	SA_6	O		S RAM address bus
29	SA_7	O		S RAM address bus
30	SA_8	O		S RAM address bus
31	SA_9	O		S RAM address bus
32	Vdd			
33	SA_{10}	O		S RAM address bus
34	SA_{11}	O		S RAM address bus
35	SA_{12}	O		S RAM address bus
36	$RTREQ_0$ *	O		Real time data transfer request to ADP#0
37	$RTREQ_1$ *	O		Real time data transfer request to ADP#1
38	RTDATA	O		Real time transfer data
39	RTCLK	I		Real time transfer clock
40	RTACK*	I		Real time transfer acknowledge

Pin number	Pin name	I/O	DT	Pin function
41	CD_7	I/O	TS	Host data bus D_7
42	CD_6	I/O	TS	Host data bus D_6
43	V_{SS}			
44	CD_5	I/O	TS	Host data bus D_5
45	CD_4	I/O	TS	Host data bus D_4
46	CD_3	I/O	TS	Host data bus D_3
47	CD_2	I/O	TS	Host data bus D_2
48	CD_1	I/O	TS	Host data bus D_1
49	CD_0	I/O	TS	Host data bus D_0
50	CDREQ *	O	OD	DMA transfer request
51	RCINT *	O	OD	Remote control interrupt request
52	DTACK *	O	OD	Data transfer completed ackowledge
53	READY *	O	OD	DMA data ready on bus
54	CDINT *	O	OD	CDC interrupt request
55	CDACK *	I		DMA transfer acknowledge
56	CCS *	I		CDC chip select for host
57	R/W *	I		Host data bus direction
58	LDS *	I		Host data bus strobe
59	DONE *	O	OD	Transfer completed signal
60	PSEL	I		Input data format switch 1
61	MSEL	I		Input data format switch 2
62	RS_2	I		Register select for host
63	RS_1	I		Register select for host
64	RS_0	I		Register select for host
65	RES *	I		CDC hardware select
66	CK	I		8 MHz master clock
67	BCI	I		Input signal bit clock
68	SDI	I		Input signal serial data
69	SDSY	I		Input signal word clock
70	SFSEL	I		LSB First/MSB First switch
71	C2FG	I		Input signal error pointer
72	Vdd			
73	DREST *	O		Sub-MPU reset
74	DD_7	I/O	TS	Sub-MPU data bus D_7
75	DD_6	I/O	TS	Sub-MPU data bus D_6
76	DD_5	I/O	TS	Sub-MPU data bus D_5
77	DD_4	I/O	TS	Sub-MPU data bus D_4
78	DD_3	I/O	TS	Sub-MPU data bus D_3
79	DD_2	I/O	TS	Sub-MPU data bus D_2
80	DD_1	I/O	TS	Sub-MPU data bus D_1

NOTE 1) * indicates active when low.

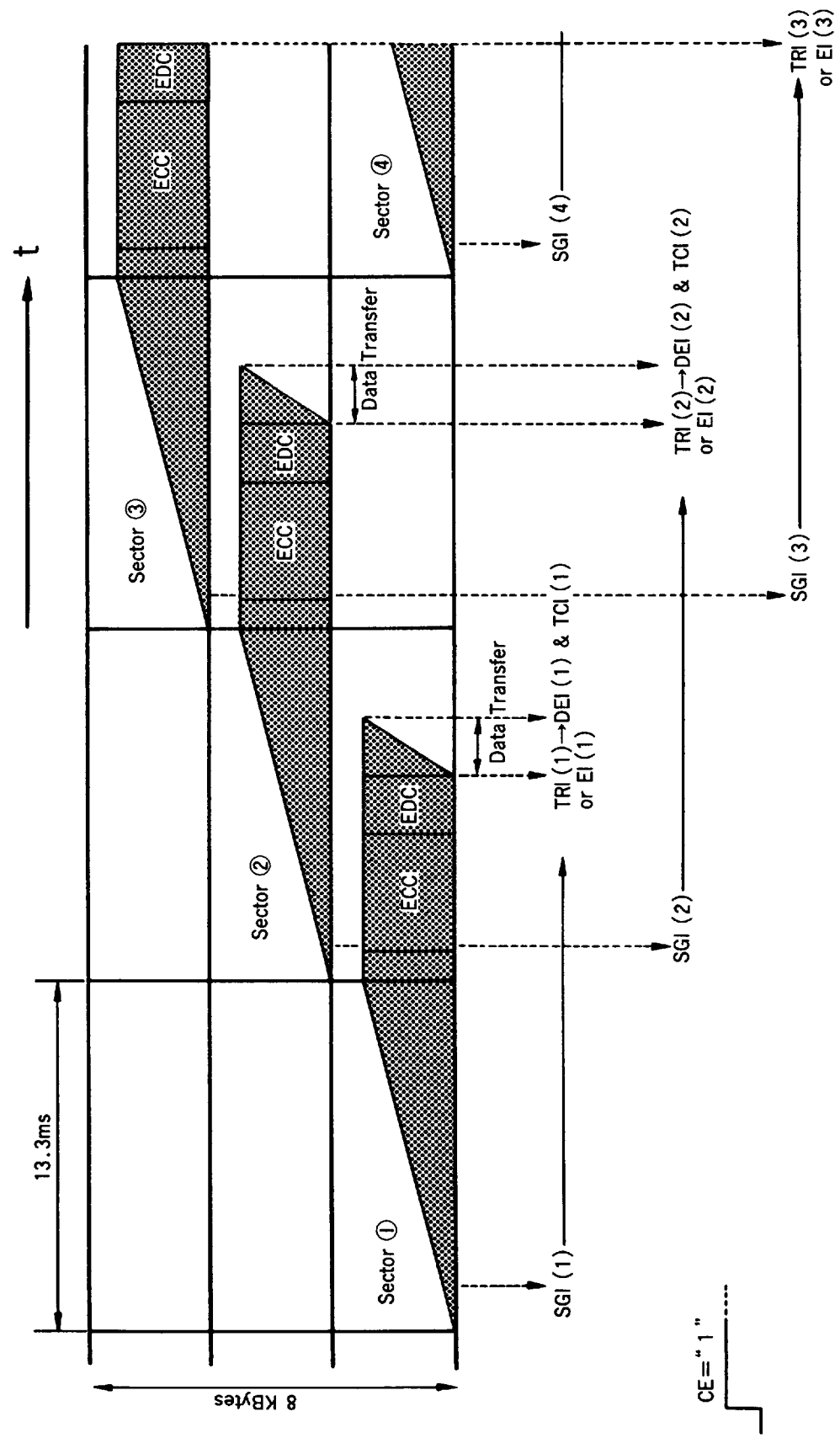
■ SUMMARY OF FUNCTIONS

1. Main Functions and Peripheral Circuitry Interface

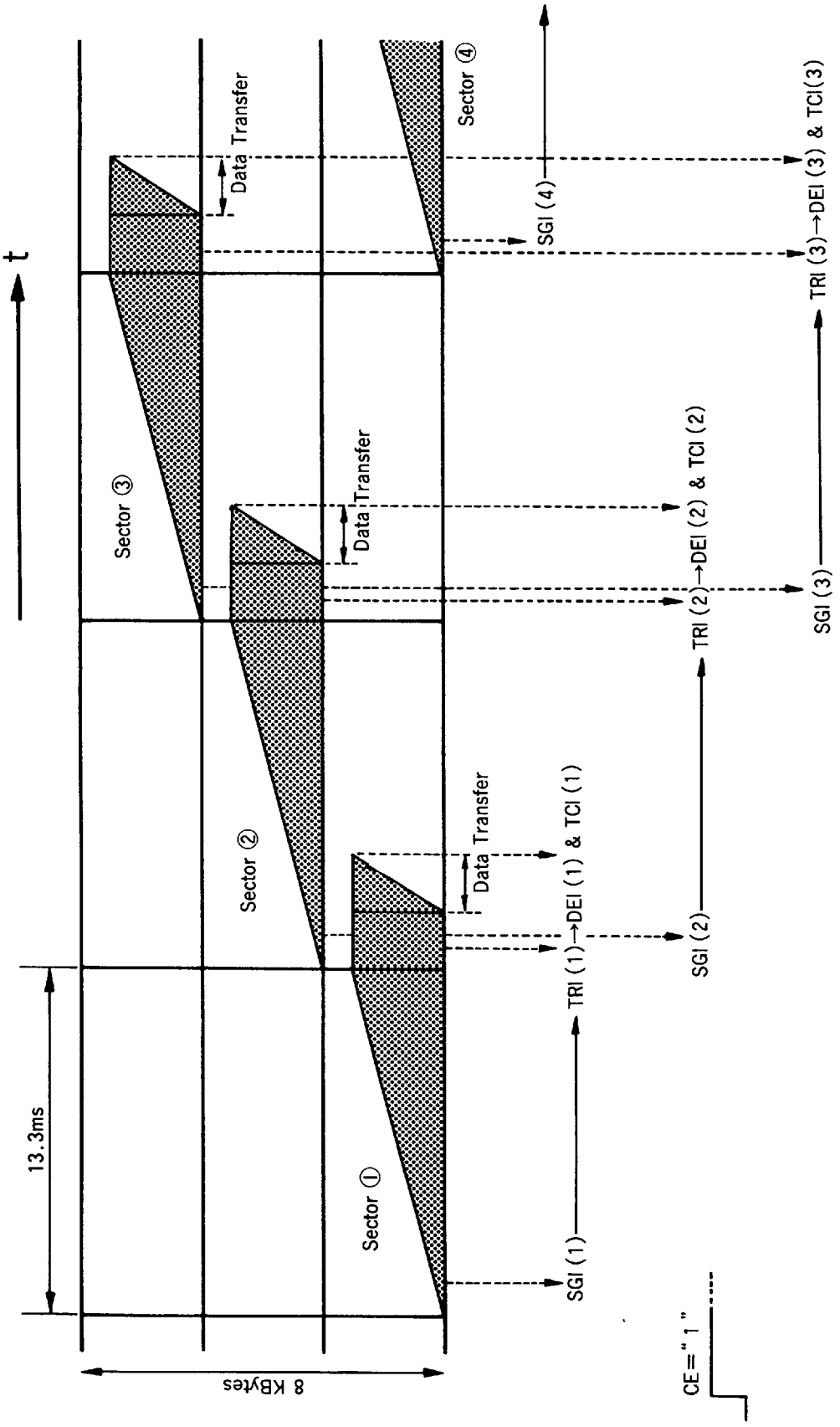
- The CDC has the capacity to detect and correct errors on both a CD-I form 1 and a CD-ROM mode 1. (However, the LSI chip does not use the error pointer which is output from the CD Drive to correct errors.) An outline of the error correction processing time and the relationship between the areas used by the 8K SRAM is shown on the following pages.
- With the sub-MPU controlling the CDC, two systems provide outlets for the output of CD-I ADPCM data. Because of this, even with no external circuits, the YM6064 (ADP) can be connected with two units (e.g. this can easily be set up with a CD-I 4 channel stereo).
- The output data format of the input signal differs according to the CD audio processor being used, so it is necessary to distinguish between the following pins: SFSEL, MSEL, PSEL. Set up according to the listings shown in the chart below.

PSEL	SFSEL	MSEL	Maker
L	L	L	—
L	L	H	—
L	H	L	(I2 S)
L	H	H	—
H	L	L	Matsushita
H	L	H	Yamaha, Sanyo (LSB First)
H	H	L	Toshiba (TC9200 cannot be connected directly), Hitachi
H	H	H	Yamaha, Sony, Mitsubishi, NEC (MSB First)

Data Flow of CD-ROM Mode 1, CD-I Form 1



Data Flow of CD-ROM Mode 2, CD-I Form 2



- This CDC controls operations through use of 68000-type MPU and sub-MPU microprocessors. In order to facilitate operation with these units, all CDC data bus and output terminals are either tri-state or open drain and it is now easier to make direct wiring connections.
  A complete set of control registers is provided in addition to those in the sub-MPU which carry out CD-I and CD-ROM operation switching.

2. 68000-type Registers

REGISTER MAP

REGISTER	R/W *	RS_2	RS_1	RS_0
MCR	0	0	0	0
MSR	1	0	0	0
CR	0	0	0	1
SR	1	0	0	1
PR	0	0	1	0
DR	1	0	1	0
TCR	0	0	1	1
——	1	0	1	1
RCIMR	0	1	0	0
RCIR	1	1	0	0
——	0	1	0	1
RCDR	1	1	0	1

MCR : DMA/IRQ, sub-MPU IRQ, sub-MPU reset
MSR : Sub-MPU ready, sub-MPU read request, DMA status
CR : Command register for the sub-MPU
SR : Status information register from the sub-MPU
PR : Parameter register
DR : Read data register
TCR : Data transfer mode changing register (DMA/software transfer)
RCIMR : Remote control IRQ mask register
RCIR : Remote control IRQ register
RCDR : Remote control data register

3. Sub-MPU Registers

REGISTER MAP

REGISTER	R/W	DA_2	DA_1	DA_0
CC0R	0	0	0	0
CS0R	1	0	0	0
CC1R	0	0	0	1
CS1R	1	0	0	1
ECR	0	0	1	0
ESR	1	0	1	0
CMR	0	0	1	1
SHR	1	0	1	1
BCR	0	1	0	0
HR	1	1	0	0
TCICR	0	1	0	1
HER	1	1	0	1
CSR	0	1	1	0
CCR	1	1	1	0
CRDR	0	1	1	1
CPR	1	1	1	1

CC0R : CDC enable, CD-I/CD-ROM mode change, data transfer mode change
The data offset number of the sector being transferred and the transfer byte number change according to the data transfer mode used. Information on the settings is given in the chart below.

CDROM/CD-I	Mode number	Offset	Transfer byte number	Reproduction mode
CD-I	0	12	2048	FORM1
CD-I	1	12	2324	FORM2
CD-I	2	0	2340	RAWREAD
CD-I	3	12	2486	ERR included
CD-ROM	0	4	2048	
CD-ROM	1	4	2336	
CD-ROM	2	0	2340	
CD-ROM	3	–	–	

CS0R : Influenced by CDC operation status
CD-I mode/CD-ROM mode, data transfer mode number, DMA transfer/ software transfer

CC1R : Host interrupt, sub-MPU ready, status read request, real time audio transfer sector data unaffected

CS1R : Interrupt status read register
Command IRQ, SYNC GET IRQ, transfer completed IRQ, ECC error IRQ, SYNC lost IRQ

ECR : Error correction repeat number set register and P/Q procedure set

ESR : Read register for contents of ECR set

CMR : CDC mask register
Command IRQ, SYNC GET IRQ, transfer request IRQ, transfer completed IRQ, ECC IRQ, SYNC lost IRQ

SHR : Sub-header register (1 set of data consists of 4 bytes of continuous readout)

	CD-I mode	CD-ROM mode
1st byte	File	Minute
2nd byte	Channel	Second
3rd byte	Sub-mode	Block
4th byte	Coding information	Mode

BCR : Buffer clearing register (Clears all SRAM data)
HR : Header register (1 set consists of 4 bytes of continuous readout)
1st byte..... Minute
2nd byte ..... Second
3rd byte..... Block
4th byte ..... Mode
TCICR : Transfer completed IRQ clear register
HER : Header error register
Mode, block, second or minute sets an error flag at any isolated bit.
CSR : Register for sending CDC status information to the host MPU
(1 set consists of 4 bytes of continuous writing)
CCR : Information register for commands from host MPU
CRDR : Remote control data register
CPR : Register for parameters and commands from the host MPU
(1 set of data consists of 8 bytes of continuous readout)

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Supply voltage	Vdd	−0.3	7.0	V
Power consumption	Pd		150	mW
Input voltage	Vin	−0.3	Vdd+0.5	V
Input current	Iin		10	mA
Ambient operating temperature	Top	0	70	°C
Storage temperature	Tstg	−50	125	°C

2. Recommended Operating Conditions

Item	Symbol	Min	Max	Unit
Supply voltage	Vdd	4.75	5.25	V
Ambient temperature	Top	0	70	°C

3. DC Characteristics

- Input terminals (Numbers shown in ( ) are CK, BCI, and RTCLK terminal coefficients.)

Item	Symbol	Min	Max	Unit
Low level input voltage	Vil	−0.3	0.8 (0.4)	V
High level input voltage	Vih	2.0 (2.4)	Vdd+0.5	V
Input leak current	Ili		10	μA

- Output terminals

Item	Symbol	Min	Max	Unit
Low level output voltage	Vol	V_{ss}	0.4	V
High level output voltage	Voh	4.0	Vdd	V
Output leak current	Ilo.		10	μA

- Power terminals

Item	Symbol	Min	Max	Unit
Power current	Idd		30 (Vdd=5.0V)	mA

4. AC Characteristics

Unit: ns

Terminal name	I/O		Min	Max	
SA0～12	O	Tsasu 1	0		Set up time for SOE* falling edge
		Tsasu 2	0		Set up time for SWE* falling edge
		Tsaho	5		Hold time for SWE*
SOE*	O	Toel	80		Low level time
SWE*	O	Twel	50		Low level time
SD0～7	I	Tsdsu	50		Set up time for SOE* rising edge
		Tsdho	0		Hold time for SOE* rising edge
	O	Tsdout		30	Delay time from SWE* falling edge
		Tsdz	0		Time from SWE* rising edge to High Z
CK	I	Tcyc	125(TYP.)		CK cycle
		Tckh	62		High level time
		Tckl	62		Low level time
CCS*	I	Tccsh	150		High level time
		Tccsl	150		Low level time
DTACK*	O	Tdtout		100	Delay from CK falling edge to low level
		Tdtz		100	Time from CCS* rising edge to High Z
LDS*	I	Tldsh	150		High level time
		Tldsl	150		Low level time
R/W*	I	Trwsu	20		Set up time for LDS* falling edge
		Trwho	20		Hold time for LDS* rising edge
RS0～2	I	Trssu	20		Set up time for LDS* falling edge
		Trsho	20		Hold time for LDS* rising edge
CD0～7	I	Tcdsu	30		Set up time for LDS* rising edge
		Tcdho	20		Hold time for LDS* rising edge
	O	Tcdout		100	Delay from LDS* (CK) falling edge
		Tcdz	0	100	Time from LDS*(CDACK*) rising edge to High Z
DCS*	I	Tdcsu	30		Set up time for DW*, DR* falling edge
		Tdcho	30		Hold time for DW*, DR* rising edge
DW*	I	Tdwh	NOTE 2		High level time
		Tdwl	NOTE 2		Low level time
DR*	I	Tdrh	NOTE 2		High level time
		Tdrl	NOTE 2		Low level time

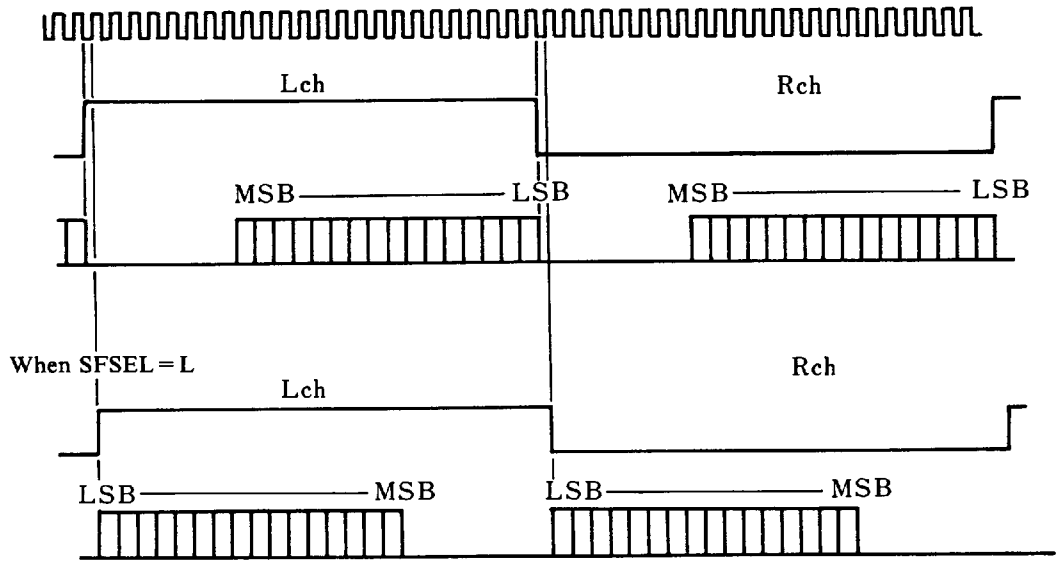
Terminal name	I/O		Min	Max	
DA0~2	I	Tdasu	30		Set up time for DW*, DR* falling edge
		Tdaho	30		Hold time for DW*, DR* rising edge
DD0~7	I	Tddsu	50		Set up time for DR* rising edge
		Tddho	30		Hold time for DR* rising edge
	O	Tddout	100		Delay from DW* falling edge
		Tddz	0		Time from DW* rising edge to High Z
BCI	I	Tbcicyc	400		BCI cycle (normally 2.1168 MHz)
		Tbcih	200		High level time
		Tbcil	200		Low level time
SDSY SDI C2FG	I	Tsdisu	50		Set up time for BCI
		Tsdiho	50		Hold time for BCI
RTACK*	I	Trtal	150		Low level time
RTCLK	I	Trtcyc	120		RTCLK cycle
		Trth	60		High level time
		Trtl	60		Low level time
RTDATA	O	Trtout		80	Delay from RTCLK rising edge
CDACK*	I	Tcdackl	NOTE 1		Time from CK falling edge to low level
		Tcdackh	150		High level time
		Tcdacksu	20		Low level set up time for CK falling edge
		Tcdackho	10		High level hold time for CK falling edge
R/W*	I	Trwdmal	NOTE 1		Low level time from CK falling edge
		Trwdmah	150		High level time
		Trwdmasu	20		Low level set up time for CK falling edge
		Trwdmaho	10		High level hold time for CK falling edge
READY*	O	Treadout		100	Low level delay time from CK rising edge
		Treadz	0	100	Time from CDACK* (R/W*) rising edge to High Z

NOTE 1: Tcdackl (Trwdmal) = 2·Tcyc + 10
NOTE 2: Tdwh = Tdwl = Tdrh = Tdrl = 2·Tcyc + 50

DONE*	O	Tdoneout		100	Low level delay time from CK falling edge
		Tdonez		100	Time from CDACK* (R/W*) rising edge to High Z
CDREQ*	O	Tcdreqz		100	Time from CK falling edge to High Z

- SAMPLE SPC INTERFACE TIMING

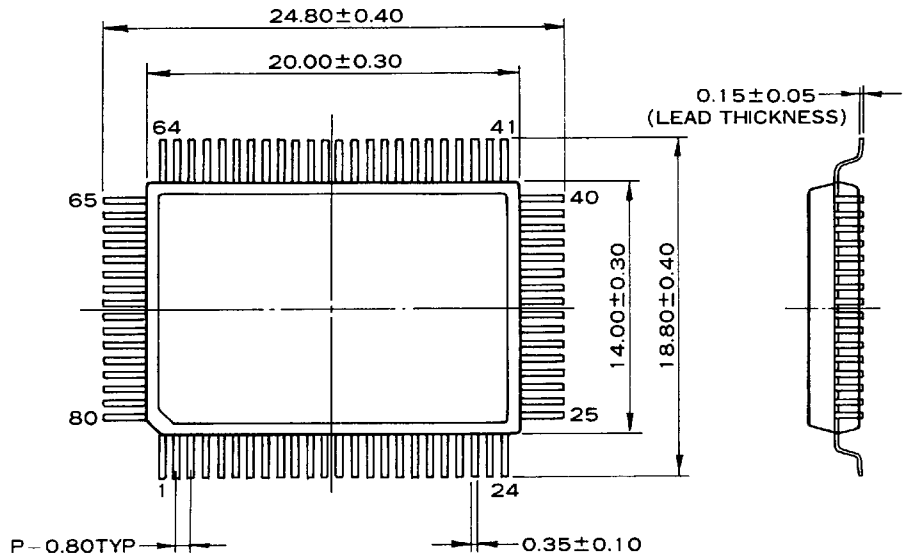
When SFSEL = H

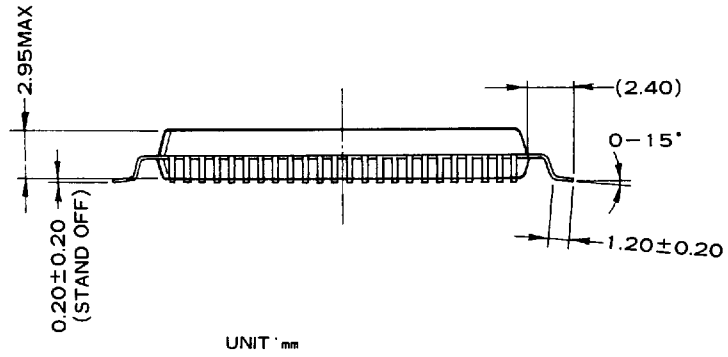


5. Terminal capacitances (f = 1 MHz)

Item	Symbol	Condition	Minimum	Maximum	Unit
Input terminal	C_I			8	pF
Output terminal	C_O	No load		10	pF
I/O terminal	C_{IO}	No load		12	pF
Output load capacitance	C_L			100	pF

■ EXTERNAL DIMENSIONS





UNIT : mm

The specifications of this product are subject to improvement changes without prior notice.

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