Quad Timing Circuits

GENERAL DESCRIPTION

The XR-558 and the XR-559 quad timing circuits contain four independent timer sections on a single monolithic chip. Each of the timer sections on the chip are entirely independent, and each one can produce a time delay from microseconds to minutes, as set by an external R-C network. Each timer has its separate trigger terminal, but all four timers in the IC package share a common reset control.

Both the XR-558 and the XR-559 quad timer circuits are "edge-triggered" devices, so that each timer section can be cascaded, or connected in tandem, with other timer sections, without requiring coupling capacitors.

The XR-558 is designed with open-collector outputs; each output can sink up to 100 mA. The XR-559 is designed with emitter-follower outputs. Each output can source up to 100 mA of load current. The outputs are normally at "low" state, and go to "high" state during the timing interval.

FEATURES

Four Independent Timer Sections
High Current Output Capability
  XR-558: 100 mA sinking capability/output
  XR-559: 100 mA sourcing capability/output
Edge Triggered Controls
Output Stage Independent of Trigger Condition
Wide Supply Range: 4.5 V to 16 V

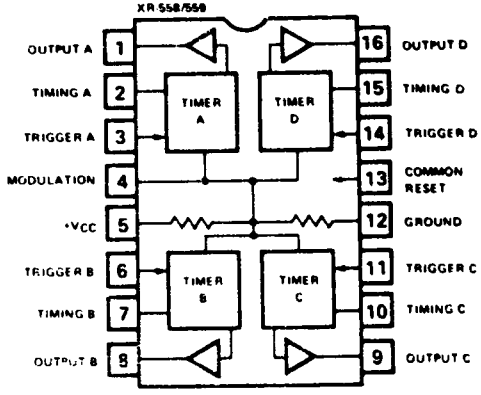
APPLICATIONS

Precision Timing
Pulse Shaping
Clock Synchronization
Appliance Timing

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25°	6 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-558M *	Ceramic	−55°C to +125°C
XR-558CN	Ceramic	0°C to +70°C
XR-558CP	Plastic	0°C to +70°C
XR-559M *	Ceramic	−55°C to +125°C
XR-559CN	Ceramic	0°C to +70°C
XR-559CP	Plastic	0°C to +70°C

*Consult factory for availability

SYSTEM DESCRIPTION

The XR-558 and XR-559 are easy to use quad timers capable of operation with supply voltages between 4.5 V and 18 V. Each section has independent timing and triggering, and can operate over intervals ranging from the low microseconds up through several minutes. The devices are triggered on falling waveforms and are immune to long trigger pulses. When the reset pin (Pin 13) is held below 0.8 V, all four outputs are set low and all triggers are disabled. Timing period accuracy is typically better than 1%, independent of V_{CC}, and drift is better than 150 ppm/°C and 0.5%/V. The timing period, in seconds, equals R times C.

The XR-558 features open collector outputs, capable of sinking 100 mA, that are driven low during the timing interval. The XR-559 has emitter followers, active upon timeout, capable of sourcing 100 mA. The XR-558 sinks load current from $+V_{CC}$, the XR-559 sources load current to ground.

XR-558/559

ELECTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise noted.)

	XR-558M/XR-559M			XR-558C/XR-559C				
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Supply Voltage	4.5		18	4.5		16	V	
Supply Current								V_{CC} = V_{RESET} = 15V
XR-558 Family		21	32		27	36	mA	Outputs Open
XR-559 Family		9	16		12	18	mA	Outputs Open
Timing Accuracy								R = 2 kΩ to 100 kΩ
Initial Accuracy		1	3		2		%	C = 1 μF
Drift with Temperature		150			150		ppm/°C	
Drift with Supply Voltage		0.1			0.1		%/V	
Trigger Characteristics								See Note: 1
Trigger Voltage	0.8	1.5	2.4	0.8	1.5	2.4	V	V_{CC} = 15V
Trigger Current		5	30		10	100	μA	$V_{TRIGGER}$ = 0V
Reset Characteristics								See Note: 2
Reset Voltage	0.8	1.5	2.4	0.8	1.5	2.4	V	
Reset Current		50	300		50		μA	
Threshold Characteristics								Measured at Timing Pins
Threshold Voltage		0.63			0.63		X V_{CC}	(Pins 2, 7, 10 or 15)
Threshold Leakage		15			15		nA	
XR-558 Output Characteristics								See Note: 3
Output Voltage		0.1	0.2		0.1	0.4	V	I_L = 10 mA
Output Voltage		0.7	1.5		1.0	2.0	V	I_L = 100 mA
Output Leakage		10			10		nA	Output High Condition
XR-559 Output Characteristics								See Note: 4
Output Voltage	13	13.6		12.5	13.3		V	I_L = 10 mA, V_{CC} = 15V
Output Voltage	12.5	13.3		12.0	13.0		V	I_L = 100 mA, V_{CC} = 15V
Propagation Delay								
XR-558 Family		1.0			1.0		μsec	
XR-559 Family		0.4			0.4		μsec	
Output Rise-time		100			100		nsec	I_L = 100 mA
Output Fall-time		100			100		nsec	I_L = 100 mA

NOTES:

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.

2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.

3. The XR-558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.

4. The XR-559 output structure is a darlington emitter follower which requires a pull down resistor to ground to source current. The output is normally low and sources current only when switched high.

DESCRIPTION OF CIRCUIT OPERATION

The XR-558/559 quad timing circuits are designed to be used in timing applications ranging from few microseconds up several hours. They provide cost-effective alternative to single-timer IC's in applications requiring a multiplicity of timing or sequencing functions.

Each quad-timer circuit contains four independent timer sections, where each section can generate a time delay set by its own resistor and capacitor, external to the IC. All four timing sections can be used simultaneously, or can be interconnected in tandem, for sequential timing applications. For astable operation, two sections of the quad-timer IC can be interconnected to provide an oscillator circuit whose duty-cycle can be adjusted from close to zero, to nearly 100%.

The generalized test and evaluation circuit for both the XR-558 and the XR-559 quad timer circuits is shown in Figure 1. Note that, the only difference between the two circuit types is the structure of the output circuitry.

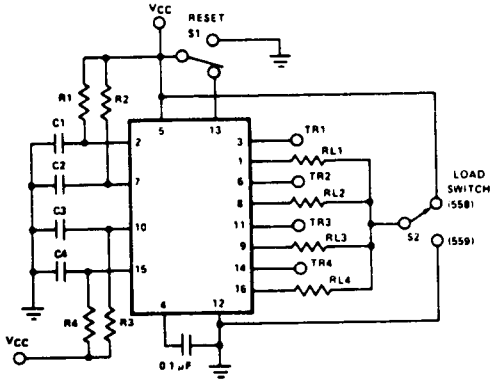


Figure 1. Generalized Test and Evaluation Circuit for XR-558/ XR-559 Quad Timer Circuits

MONOSTABLE OPERATION

In the monostable, or one-shot mode of operation, it is necessary to supply two external components, a resistor and a capacitor, for each section of the timer IC. The timing terminals of those timer-sections not being used can be left open-circuited. The time period is equal to the external RC product. A plot of the timing period, T, as a function of the external R-C combination is shown in Figure 2.

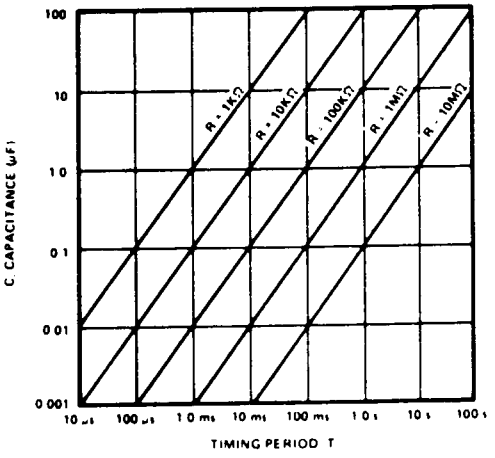


Figure 2. Timing Period, T, as a Function of External R-C Combination (Note: T = 1.0 RC)

ASTABLE OPERATION

For astable, or free-running, operation of the quad timer circuits, it is desirable to cross-couple two of the timer sections on the chip, as shown in Figure 3. In this circuit configuration, the outputs of each section are direct-coupled to the opposite trigger input. Thus, the "high" and "low" half-periods of the output can be set by the external R-C products, as R_1C_1 and R_2C_2, respectively. The frequency of oscillation, and the output duty-cycle are given as:

$$\text{Frequency of Oscillation} = \frac{1}{R_1 C_1 + R_2 C_2}$$

$$\text{Output Duty-Cycle} = \frac{R_2 C_2}{R_1 C_1 + R_2 C_2}$$

The frequency of oscillation can be externally controlled by applying a control-voltage to the control terminal (pin 4). Since the control terminal is common to all the timer sections, the duty cycle of the output waveform is not effected by the modulation voltage; thus the circuit can function as a variable-frequency, fixed duty-cycle oscillator.

The frequency of oscillation increases as the voltage at the control terminal (pin 4) is lowered below its open-circuit value.

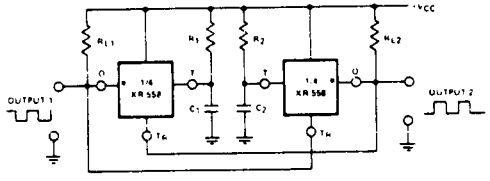


Figure 3. Typical Circuit Connection for Astable Operation Using Two Timer-Sections. (Note: For XR-559, R_{L1} and R_{L2} are Connected from Outputs to Ground.)

OUTPUT STRUCTURE

The XR-558 family of quad timers have "open-collector" NPN-type output stages. Each output can individually sink up to 100 mA of load current. However, with more than one output active, the total current capability is limited by the power-dissipation rating of the IC package (see Absolute Maximum Ratings). In the normal operation of the circuit, each output will require a pull-up resistor to $+V_{CC}$. The output is normally "low" state (i.e. sinking current) when the timer is at reset; and goes to "high" state during the timing cycle.

The XR-559 family of quad timers have Darlington NPN "emitter-follower" type outputs. Each output can source up to 100 mA, during its "high" state. The total amount of output current, available from all outputs, is limited by the package power dissipation rating. For normal operation of the circuit, a pull-down resistor is required from each output to ground. The output of XR-559 is normally low (i.e. at "off-state"), and goes to "high" state when the circuit is triggered.

TRIGGER INPUTS

Each timer section of the quad-timer IC's has its own trigger input. The trigger level is set at nominally +1.5 V, and the trigger input is *edge-triggered* on the falling edge of an input trigger pulse. In other words, for proper triggering, the trigger signal must first go "high" and then go "low". If both the trigger and the reset controls are activated, the reset control overrides the trigger input.

RESET INPUT

The reset control (pin 13) is common to all four timer section and resets all of the timer sections simultaneously.

The reset voltage must be brought below 0.8 V to insure reset condition. When reset is activated, all the outputs go to "low" state. While the reset is active, the trigger inputs are inhibited. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.

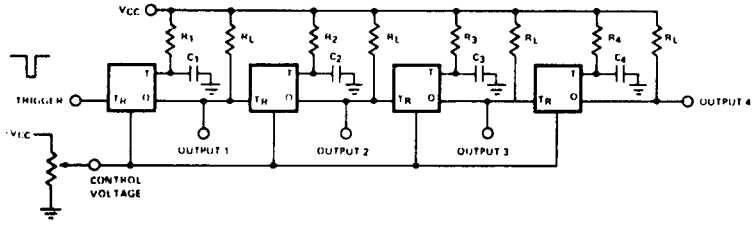
CONTROL VOLTAGE

The control voltage terminal (pin 4) is common to all four timer sections of the XR-558 or the XR-559. This terminal allows the internal threshold voltages of all four timer sections to be modulated, and thus provides the control of the pulse-width or the duty-cycle of the output waveforms. The range of this control voltage is from 0.5 V to $+V_{CC}$ minus 1 Volt. This range provides an over-all timing variation of approximately 50:1. Since the time period of each timer section is proportional to the control voltage, all four timing periods can be simultaneously varied, and their relative ratios remain unchanged over the adjustment range.

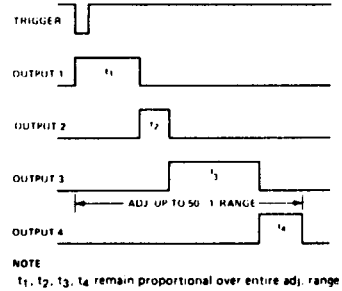
APPLICATIONS EXAMPLE

Sequential Timer:

Figure 4 shows a typical application for the quad-timer in sequential timing application. For illustration purposes, the XR-558 is used in the example. Note that, when triggered, the circuit produces four sequential time delays, where the duration of each output is independently controlled by its own R-C time constant. Yet, all four outputs can be modulated over a 50:1 range, and remain proportional over this entire range. Since each timer section is edge-triggered, the sections can be cascaded by direct coupling of respective outputs and trigger inputs.

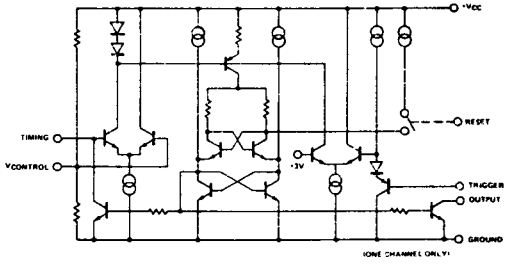


(a) Circuit Connection

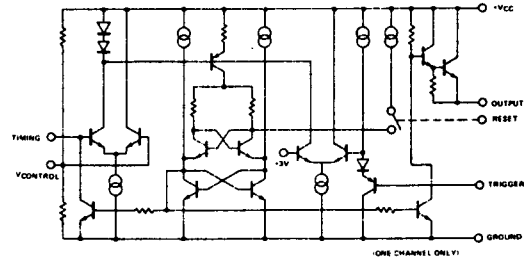


(b) Timing Waveforms

Figure 4. Using the XR-558 as a Four-Stage Sequential Timer with Voltage Control Capability



XR-558 EQUIVALENT SCHEMATIC



XR-559 EQUIVALENT SCHEMATIC

EXAR

XR-1488/1489A

Quad Line Driver/Receiver

GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. the XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

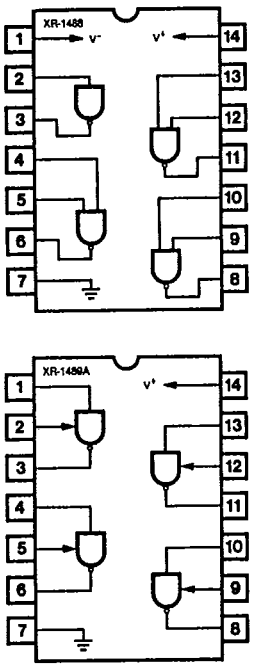
ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-1488	±15 Vdc
XR-1489A	+10 Vdc
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	6.7 mW/°C
Plastic Package	650 mW/°C
Derate above +25°C	5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAMS



SYSTEM DESCRIPTION

The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a ±10 mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/μS limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to ±30 V. The output can typically source 3 mA and sink 20 mA.