

R/W Preamplifier for 3 Terminal Recording Heads, 4, 6, or 8 Channels

GENERAL DESCRIPTION

The XR-511 is a high speed, low noise head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-511 is compatible with 3 1/2" to 14" multiple platter drives and features low noise, large dynamic range, and high bandwidth. Several packaging options extend usefulness to applications requiring six or eight center-tapped read/write heads. Multiple devices are easily cascaded for drives with more heads.

The XR-511 features a pinout with all head ports on one side of the circuit. This eases flex cable or PC board layout by eliminating crossovers. The XR-511R option includes internal damping resistors facilitating use in systems requiring minimum external circuit complexity.

XR-511, manufactured with a high speed bipolar process, operates on +5 V and +12 V. It is offered in a variety of packages, both surface mount and DIP.

FEATURES

- Complete Head Interfacing Functions, Read and Write
- Low Noise Preamplifier
- High Dynamic Range and Bandwidth
- Pinout Optimized for Easy Layout
- Available in Four, Six and Eight Head Versions
- Easily Cascaded for Larger Systems
- Full Featured Power Monitor
- TTL Compatible Control Inputs
- Optional Internal Damping Resistors

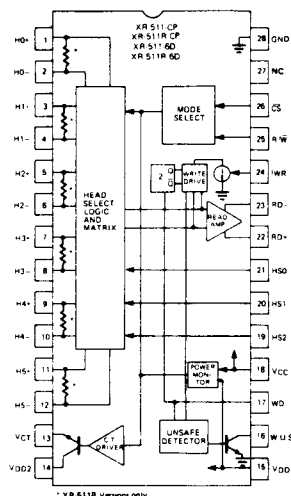
APPLICATIONS

Hard Disk Drives with MIG, ferrite, or composite heads

ABSOLUTE MAXIMUM RATINGS

V_{DD}	15V
V_{CC}	6V
Digital Inputs	-0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-511-4D	24 Pin SO	0°C to 70°C
XR-511-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-511-6CJ	28 Pin PLCC	0°C to 70°C
XR-511-6D	28 Pin SO	0°C to 70°C
XR-511-BCP	40 Pin Plastic DIP	0°C to 70°C
XR-511-8CJ	44 Pin PLCC	0°C to 70°C
XR-511-8D	32 Pin SO	0°C to 70°C
XR-511R-4D	24 Pin SO	0°C to 70°C
XR-511R-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-511R-6CJ	28 Pin PLCC	0°C to 70°C
XR-511R-6D	28 Pin SO	0°C to 70°C
XR-511R-8CP	40 Pin Plastic DIP	0°C to 70°C
XR-511R-8CJ	44 Pin PLCC	0°C to 70°C
XR-511R-8D	32 Pin SO	0°C to 70°C

SYSTEM DESCRIPTION

The XR-511 consists of a low noise preamplifier for reading from center tapped magnetic heads, a write current source for writing to the heads, a switching matrix to select one of eight heads, and associated control and monitoring functions. Less than 1.0 nV/√Hz (nominal) noise allows error free operation with small input signals. Over 40 mA of write current are available.

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ELECTRICAL SPECIFICATIONS

Test Conditions: TA = 25°C, V_{CC} = 5 V, V_{DD} = 12 V, I_W = 40 mA, R_D = 750Ω, C_L (R_D+, R_D-) ≤ 20 pF, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
I _{CC}	Supply Current		30	35 mA	mA	V _{CC} = 5.5 V, Read or Idle Mode V _{CC} = 5.5 V, Write Mode
I _{DD}	Supply Current			20 40 20	mA mA mA	V _{DD} = 13.2 V, Idle Mode V _{DD} = 13.2 V, Read Mode V _{DD} = 13.2 V, Write Mode, I _W = 0 mA
PD	Power Dissipation			400 600 670 800	mW mW mW mW	Idle Mode - V _{CC} - 5.5 V, V _{DD} = 13.2 V Read Mode - V _{CC} - 5.5 V, V _{DD} = 13.2 V I _W = 40 mA, R _{CT} = 160Ω I _W = 40 mA, R _{CT} = 0Ω
V _{CT}	Center Tap Voltage		5.0 7.0		V V	Read Mode Write Mode
V _{PM}	Power Monitor Protection	3.7 8.5	4.0 9.6	4.4 10.5	V V	V _{CC} to Disable Write V _{DD1} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V _{OL}	Saturation Voltage		0.2	0.5	V	I _{OL} = 8 mA
I _{OH}	Leakage Current			100	μA	V _{OH} = 5 V
V _{IL}	Input Low Voltage			0.8	V	
V _{IH}	Input High Voltage	2.0			V	
I _{IL}	Input Low Current	-0.4			mA	V _{IL} = 0.8 V
I _{IH}	Input High Current			100	μA	V _{IH} = 2.0 V
WRITE CHARACTERISTICS						
	Write Current Accuracy	-5		5	%	Error from I _W = R _W ^{2.5V}
	Recommended Write Current Range	10		40	mA	
	Differential Head Voltage Swing	7.0	11		V	Peak (Inductive Load)
	Unselected Differential Head Current			85	μA	
	Unselected Transient Current			2	mA	Peak

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
WRITE CHARACTERISTICS						
K_I	Differential Output Capacitance	10		15	pF	XR-511 XR-511R WUS = Unsafe
	Differential Output Resistance	635	750	865	K Ω	
	WD Rate/Transistion Freq.	125	500		KHz	
K	Current Source Factor		1			$K_I I_W$ (Current through R_W)
K	Write Current Constant	2.375	2.50	2.625	V	$K = I_W \cdot R_W$
	Write Protection Leakage Current	-200		200	μ A	Per Side, $V_{CC} \leq 3.7$ V $V_{DD} \leq 8.5$ V
V_{OS}	Preamplifier Output Offset Voltage	-20		+20	mV	Write or Idle Mode
V_{CM}	Preamplifier Output Common Mode Voltage		5.3		V	Write or Idle Mode
	Preamplifier Output Leakage Current	-100		100	μ A	Write or Idle Mode, $R_D = R_{D-} = 6$ V
READ MODE						
A_V	Differential Voltage Gain	85		115	V/V	$V_{IN} = 1$ mVp-p at 300 kHz. $R_{L+} = R_{L-} = 1$ k Ω DC input voltage where gain drops 10%. $V_{IN} = V_i + 0.5$ mVp-p at 300 kHz.
	Dynamic Range	-3		+3		
R_{IN}	Differential Input Resistance	2	8		K Ω	XR-511 XR-511R
		530	650	790	Ω	
C_{IN}	Differential Input Capacitance			20	pF	
e_{ni}	Input Noise Voltage		1.0	1.5	nV/ $\sqrt$ Hz	$L_h = 0$, $R_h = 0$, BW = 15 MHz
BW	Bandwidth	30	60		MHz	-3 dB Point, $ Z_s \leq 5 \Omega$, $V_{IN} = 1$ mVp-p
I_B	Input Bias Current		10	45	μ A	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} - V_{CT} + 100$ mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1} , V_{DD2} or V_{CC}

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
READ MODE (cont)						
V_{CM}	Channel Separation	45	60			Unselected Channel: $V_{IN} = 100$ mVp-p at 5 MHz. Selected Channel $V_{IN} = 0$ V
	Output Offset Voltage	-440	-+50	440	mV	
	Common Mode Output Voltage	4.5	5.5	6.5	V	
ΔV_{CM}	VCM Change from Write to Read		500		mV	Common Mode Output Voltage Change from Write to Read or Read to Write Per Side
	Head Current Leakage	-200		200	μ A	
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	1	μ s	Note 1 Notes 2,3
	Write to Read		0.1	1	μ s	
CS	Start-up Delay		0.1	1	μ s	Notes 1,2 Note 3 Note 2, Switching between any heads.
	Inhibit Delay		0.1	1	μ s	
	Head Switching Delay		0.1	1	μ s	
WUS	Write Unsafe					$I_W = 35$ mA, See Figure 1, TD1 $I_W = 35$ mA, See Figure 1, TD2
	Safe to Unsafe	1.6		8.0	μ s	
	Unsafe to Safe		0.2	1	μ s	
I_W	Head Current					Note 4, See Figure 1, TD3 Note 5 10% to 90% or 90% to 10% point
	Propagation Delay		2	25	ns	
	Asymmetry		0.1	2	ns	
	Rise or Fall Time		1	20	ns	

Note 1: Delay to 90% of I_W .

Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.

Note 3: Delay to 90% Decay of I_W .

Note 4: From 50% Points. $L_H = 0\mu H$, $R_H = \infty\Omega$.

Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

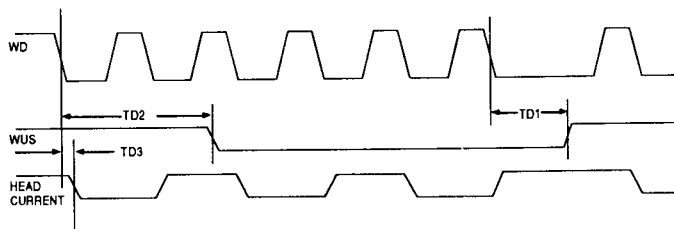


Figure 1. Write Mode Timing Diagram

A full-featured power monitor circuit disables the write mode during power-up and low operating voltage conditions, protecting data integrity. Improved write stability over 501-type devices is achieved by employing a unity gain write current constant.

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select (LS) and Read/ Write (R/W) must be pulled low. The desired head, selected by HSO to HS2, is driven by a differential current sink of magnitude I_W , set by R_{IW} . Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT} , which is "high" in the write mode. Write unsafe (WUS) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: -open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode. The power supply monitor disables writing when V_{CC} drops below 4 V and/or V_{DD1} drops below 9 V.

Read Mode

Pulling R/W high enables the data readback mode. A low noise, high gain differential amplifier increases the weak read signal amplitude and provides low output impedance drive for the following stage (Pulse Detector).

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-511 is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-511R option has 750 Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-511R option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-511 lead to a certain degree of electrostatic discharge (ESD) susceptibility. so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W , typically between 20 mA and 40 mA, is determined by a single resistor, R_{IW} .

$$R_{IW} = \frac{2500}{I_W}$$

where I_W is in mA and R_{IW} is in Ohms.

Device power dissipation is reduced by a resistor, R_{CT} , connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage is then dropped across the resistor.

With the nominal 12 V supply, R_{CT} is calculated as

$$R_{CT} = \frac{130}{I_W} \text{ (55)}$$

where R_{CT} is in Ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small surface mount packages. All XR-511 packages are suitable for continuous operation under worst case conditions without requiring R_{CT} . If R_{CT} is not used, V_{DD2} is directly connected to V_{DD1} .

Write Unsafe Indicator (WUS)

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exists. Four conditions; open head, open center tap, no write current and write data transition rate too low are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS. This output is for indication only, intended for signaling a controller, and does not stop the write operation. A pull-up resistor of from 2 k Ω to 10 k Ω is necessary for operation of this open collector output.

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Power Monitor Considerations

A power monitor circuit protects data integrity by preventing erroneous writing during power up and low voltage periods. The power monitor disables write current when V_{CC} is below about 4 V and/or V_{DD1} is below about 9 V. Hysteresis avoids unwanted toggling about the thresholds. At V_{CC} and V_{DD1} levels above these thresholds, operation is fully controllable,

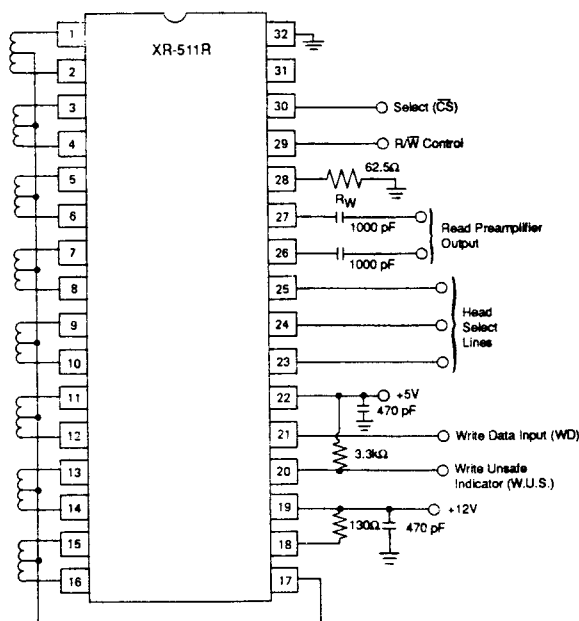
Device operation at standard voltages ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{DD1} = 12\text{ V} \pm 10\%$) is not affected in any way and is fully specified.

Read mode operation is not affected by the power monitor circuitry.

Read Mode Design Considerations

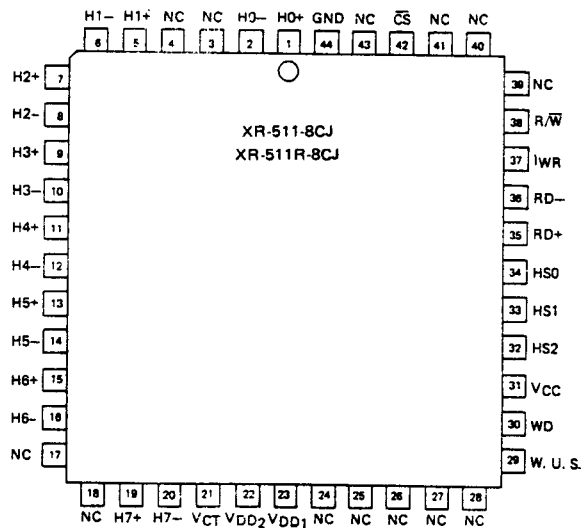
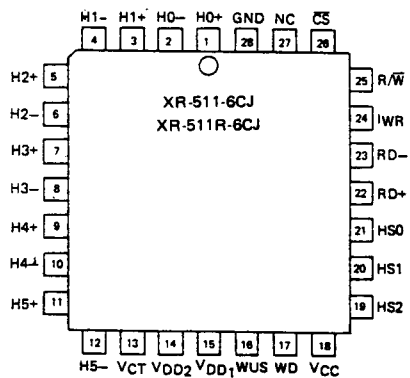
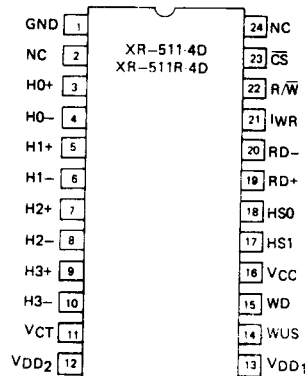
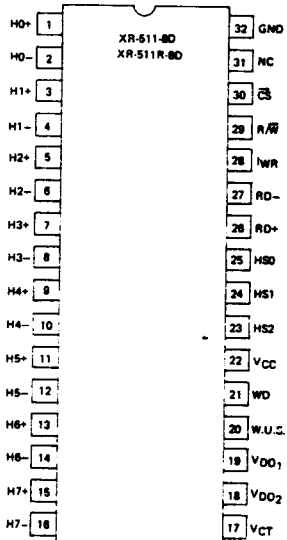
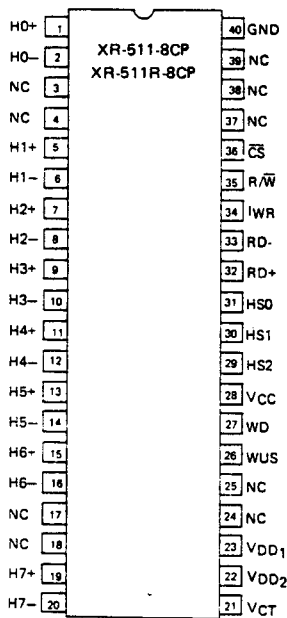
The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (1.0 nV/ $\sqrt{\text{Hz}}$ typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 5.5 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 μA .

The XR-511 read preamplifier is specially designed to minimize output common mode voltage changes between writes mode and read mode, thus reducing switching transients that slow write to read recovery time. DC shifts are typically held under 500 mV from the 5.5 V nominal bias level.



XR 511R Typical Application Circuit

NOTE: Non 'R' Versions Require External Damping Resistors



XR-511-6CP/511R-6CP/511-6D/511R-6D 28 Pin Package Pinout shown on front page.