Universal Data Buffer

GENERAL DESCRIPTION

The XR-2124 is a logic circuit designed to perform the data buffer function for modem systems. Both asynchronous to synchronous and synchronous to asynchronous conversion are performed at data rates up to 9600 bits per second. The XR-2124 is selectable for character lengths of 9 or 10 bits. Separate enable/disable inputs are supplied for async to sync and sync to async converter sections. These inputs allow the same data lines to be used for asynchronous or synchronous operation.

The receive data buffer section (sync to async) accepts input sync data (typically from the modem demodulator) and converts it to an async data format. The transmit data buffer (async to sync) accepts input async format data and it is synchronized to the selected data rate which is typically sent to the modulator. This section also provides break signal automatic extension.

The data rate is selected by changing the clock in frequency.

The XR-2124 is constructed using silicon gate CMOS technology for low power operation. Operation is designed for an input clock frequency up to 2.5 MHz. The XR-2124, available in a 14 Pin package, is designed for single 5 volt operation.

FEATURES

Data Rates to 9.6 KBS
Bell 212A Programmable
Asynchronous to Synchronous Conversion
Synchronous to Asynchronous Conversion
Independent Disable Input for
  Receiver and Transmitter Sections
Break Signal Automatic Extension for Transmitter
Single 5 Volt Operation
Selected Data Rate +1%, −2.5% Operation

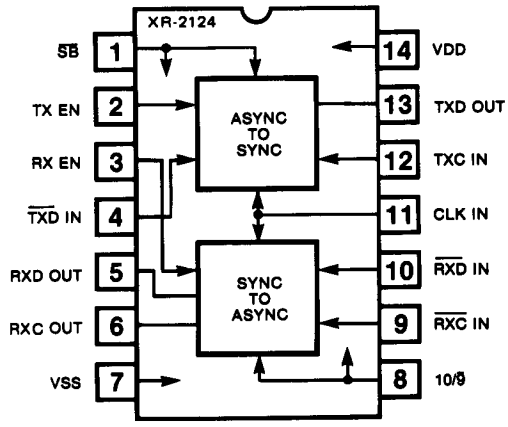
APPLICATIONS

Modem Data Buffers
Terminal Data Buffers

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3 to +7.0 V
Input Voltage	-0.3 to V_{DD} +0.3
DC Input Current (any input)	±10 mA
Power Dissipation (Package Limitation)	250 mW
Storage Temperature Range	-65°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2124CN	Ceramic	0°C to 70°C
XR-2124CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2124 provides the complete interface between synchronous and character - asynchronous data systems. The synchronous side consists of two data lines, T_{XD} and R_{XD}, each with their respective clocks, T_{XC} and R_{XC}. The synchronous portion is designed for data rates up to 9.6 KBPS. The asynchronous side handles data oriented in characters where the actual data bits are bracketed by a start and stop bit. Character lengths are 9 or 10 bit (7 or 8 data bits), pin selectable.

To perform this interface, the XR-2124 consists of two main sections: synchronous to asynchronous (receive section) converter to reinsert stop bits deleted by the sending modem. The other section is the asynchronous to synchronous converter (transmit section) to add or delete stop bits to correct the transmit data rate to the rate selected (CLK IN ÷ 256). This section also extends the break signal to two character lengths plus three bits when it comes in at a shorter period.

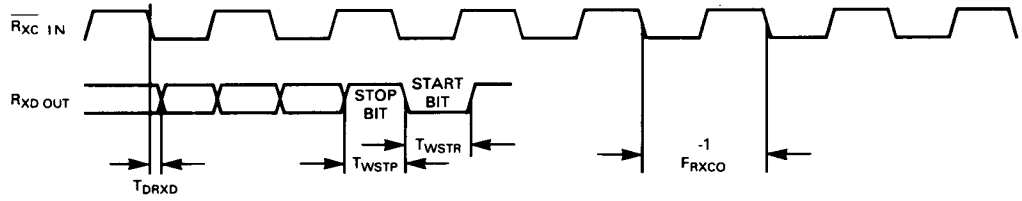
A standby mode is included to put the XR-2124 in a low supply current, non-operative, mode on command.

ELECTRICAL CHARACTERISTICS

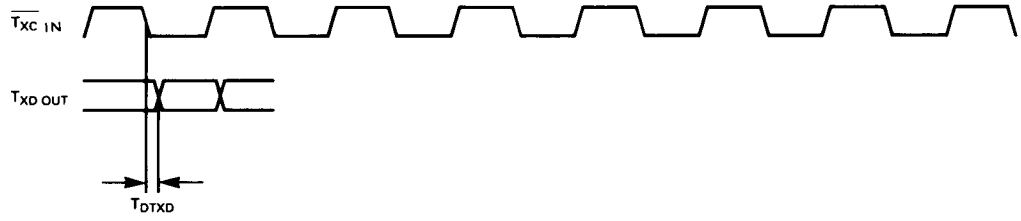
Test Conditions: V_{DD} = 5 V ±5%, T_A = 0°C to 70°C, CLK IN = 307.2 KHz ±0.01%, Data Rate = 1200 BPS, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS						
V_{OL}	Output Low Voltage		0.05	0.8	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400μA
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
I_{OL}	Output Low Current		2		mA	
I_{OH}	Output High Current			−400	μA	
I_{IN}	Input Current			±10	μA	V_{IN} = 0 - V_{DD}
I_{DD}	Supply Current Quiesent		100	250	μA	
I_{DD}	Supply Current Standby			10	μA	
AC CHARACTERISTICS: $f_{TXC\ IN}$ = 1200 Hz ±0.01%, $f_{RXC\ IN}$ = 1200 Hz ±0.01%.						
t_{wstr}	Start Bit Width		820		μs	
t_{wstp}	Stop Bit Width 9 Bit Character 10 Bit Character		 938 951		 μs μs	 Reinserted Stop Bits and (n) (820 μs) long
f_{txd}	$\overline{TXD}$ IN Bit Rate	1170	1200	1212	BPS	
t_{dtxd}	TXD Out Delay Time			200	ns	C_L @ 50 pf; 10/$\overline{9}$ = Hi
t_{drxd}	RXD Out Delay Time			200	ns	10/$\overline{9}$ = Hi
f_{rxco}	RXC Out Frequency		1219		Hz	

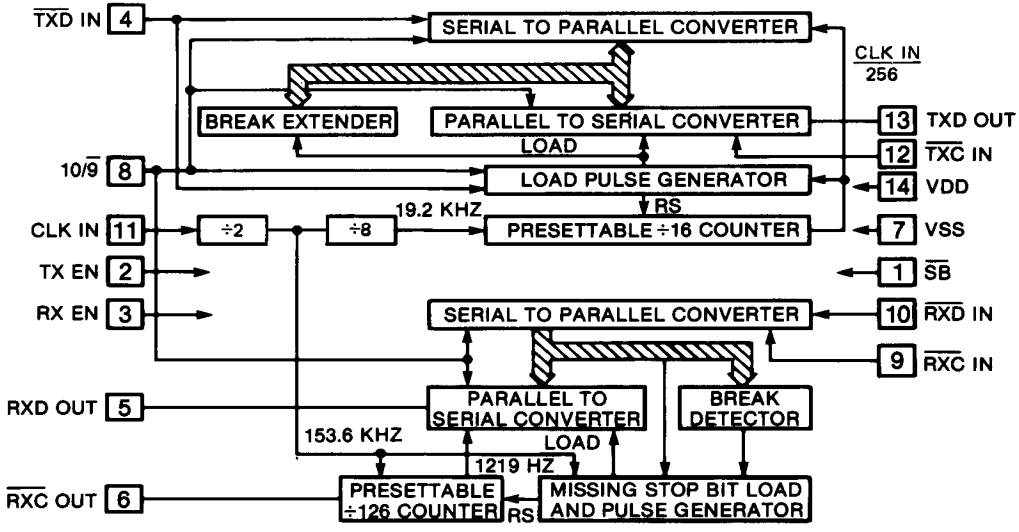
RECEIVE TIMING



TRANSMIT TIMING



TRANSMIT AND RECEIVE TIMING CHARACTERISTICS



FREQUENCIES SHOWN ARE FOR 1200 BPS OPERATION,
CLK IN = 307.2 KHZ

EQUIVALENT SCHEMATIC DIAGRAM

DESCRIPTION OF INPUTS AND OUTPUTS

Pin	Name	Description
1	$\overline{SB}$	This pin places the XR-2124 in a non-operative, low quiesent current mode.
2	T_{XEN}	An enable input for the transmitter section (async to sync). When enabled, async to sync conversion is performed on $\overline{T_{XD}}$ IN. When disabled, the data on T_{XD} OUT will be identical to that of $\overline{T_{XD}}$ IN (flow through mode) In Bell 212A type modem applications the sync to async will be disabled for 300 BPS FSK operation and for 1200 BPS synchronous operation.
3	R_{XEN}	An enable input for the receiver section (sync to async). When enabled, sync to async conversion is performed on $\overline{R_{XD}}$ IN. When disabled, the data on R_X OUT will be identical to that of $\overline{R_{XD}}$ IN (flow through mode). In Bell 212A type modem applications the sync to async will be disabled for 300 BPS FSK operation and for 1200 BPS synchronous operation.
4	$\overline{T_{XD}}$ IN	The transmitter data input. This is a serial data stream with a data rate of data rate selected +1%/-2.5% (T_X EN active).
5	R_{XD} OUT	The asynchronous serial data out-from the sync to async converter (R_X EN active). The data rate of this signal is 1219 BPS for Bell 212A applications.
6	R_{XC} OUT	Received clock output.
7	V_{SS}	Ground pin.
8	$10/\overline{9}$	Asynchronous character length selection input. Ten bit (start bit, 8 data bits and a stop bit) or nine bit (7 data bits) can be selected.
9	$\overline{R_{XC}}$ IN	The receive clock input which typically is supplied by the demodulator (XR-2122). The frequency should be data rate selected ±0.01%.
10	$\overline{R_{XD}}$ IN	The synchronous serial data input which is typically from the demodulator data output (R_{XD} of the XR-2122). The data rate of this signal is data rate selected ±0.01%.
11	CLK IN	Master clock input which sets the desired data rate. Data rate = CLK IN /256.
12	T_{XC} IN	The transmit clock input which is typically supplied by the modulator (XR-2121). The frequency should be data rate selected ±0.01%.
13	T_{XD} OUT	The synchronous serial data output which typically goes to the modulator input (XR-2121). The data rate of this signal is data rate selected ±0.01%.
14	VDD	This pin provides the input for the positive power supply which should be +5 ±0.25 volts.

CONTROL INPUTS

Table 1 gives the logic conditions for the various control inputs of the XR-2124.

PIN	NAME	FUNCTION LOGIC HIGH	FUNCTION LOGIC LOW
1	SB	Normal Operation	Standby Mode
2	T_{XEN}	Transmitter Enabled	Transmitter Disabled
3	R_{XEN}	Receiver Enabled	Receiver Disabled
8	10/9	10 Bit Character	9 Bit Character

Table 1. Control Input Conditions

PRINCIPLES OF OPERATION

The XR-2124 performs the complete asynchronous to synchronous and synchronous to asynchronous conversion on the serial transmit and receive data paths in modem systems. This conversion allows the sync modulator/demodulator such as the XR-2121/XR-2122 to communicate with the async DTE. The async format is character type as shown in Figure 1.

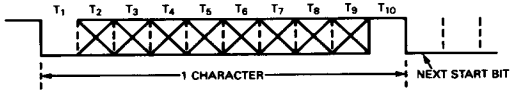


FIGURE 1. ASYNC CHARACTER

Figure 1 shows each character starting with a start bit (T1) followed by either 7 or 8 data bits (8 shown → T2 T9) and ending by a stop bit T10. This makes a total character length of eithr 9 or 10 bits, which the XR-2124 can be selected for by pin 8, 10/9.

The XR-2124 can also provide "flow through" operation by disabling the transmit and receive sections using pins 2 and 3, T_{XEN} and R_{XEN}. This mode would be used for 1200 BPS sync mode or 300 BPS bit async operation in Bell 212A type modems.

Figure 2 illustrates a typical connection of the XR-2124. Pins 2 and 3 (T_{XEN} and R_{XEN}) are used to toggle the XR-2124 between synchronous and asynchronous modes. The main function of the XR-2124 is to synchronize asynchronous data selected data rate +1%, −2.5% from the DTE to synchronous data for the modulator, and to take synchronous demodulated data and convert it to the asynchronous format for the DTE.

The break detector serves to distinguish between an actual break character and two consecutive nulls with the stop bit deleted. It forces reinsertion of the stop bit between the nulls and passes.

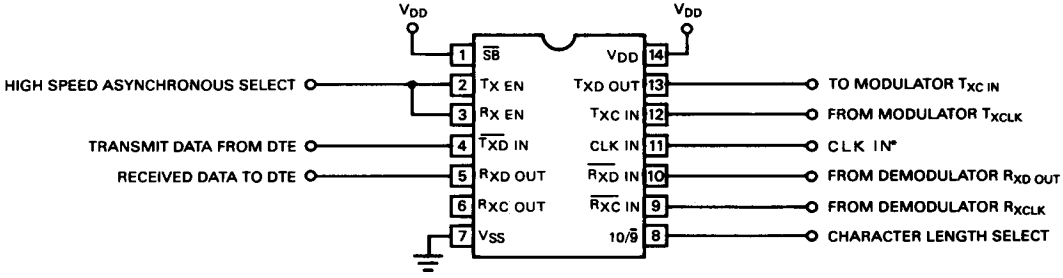


Figure 2. Typical Connection XR-2124

$$*\text{DATA RATE (BPS)} = \frac{\text{CLK IN}}{256}$$