



Value Series Flash Memory Card (AMD based) 4, 8, 16 MEGABYTE

General Description

The WEDC Value Series (FV) Flash memory cards offers a low cost linear Flash solid state storage solution for code and data storage, high performance disk emulation, mobile PC and embedded applications.

The WEDC FVB Value series is based on AMD Flash memories. Current cards are based on the AMD 29F016 (2MB) device whose manufacturer and device code is 01 and ADH respectively. The symmetrically blocked architecture and single 5V operation provides a cost effective, high performance, nonvolatile storage solution. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

The Value series is designed as a simple x16 linear array of Flash devices. Two Flash devices in parallel provide the lower and upper bytes for the 16 bit access. The Value series does not provide access of the ODD byte (D8 - D15) on the even byte data path (D0 - D7).

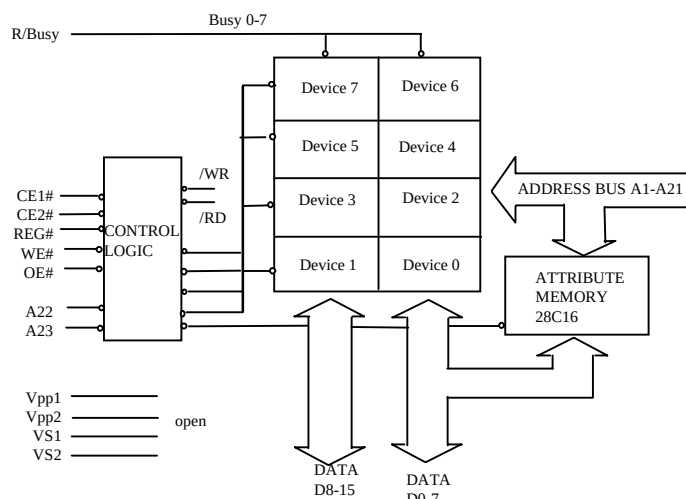
WEDC's standard Value Series Flash Card is shipped with no attribute memory or CIS (Card Information Structure) information. An option for 2KB of attribute memory with CIS information is available. The CIS for the WEDC Value series may also be stored in Block 0 (even bytes, D0 - D7 only) of the Flash memory, this option is available by request only.

WEDC's standard cards are shipped with WEDC Logo. Cards are also available in blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information Custom artwork.

Features

- Low cost Linear Flash Card
- Single 5 Volt Supply
- Based on AMD Flash Components
 - very low power without entering reset mode
 - allows standard access from low power mode
- Fast Read Performance
 - 150ns Maximum Access Time
- x16 Data Interface
 - Odd byte not accessible on Even byte
- High Performance Random Writes
 - 10µs Typical Word Write Time
- Automated Write and Erase Algorithms
 - AMD Command Set
- 50µA Typical Deep Power-Down
- 100,000 Erase Cycles per Block
- 64K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor

Block Diagram



Note: Configuration above for 16MB card using 16Mbit components.



Pinout

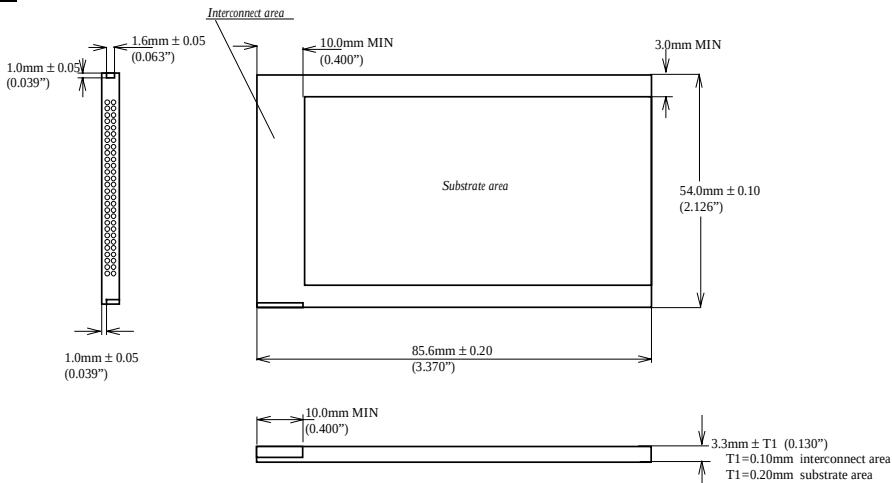
Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	NC
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	N.C.
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	
50	A21	I	Address bit 21	4MB(2)
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	I	Address bit 22	8MB(2)
54	A23	I	Address bit 23	16MB(2)
55	A24	I	Address bit 24	N.C.
56	A25	I	Address bit 25	N.C.
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	HIGH
59	Wait#	O	Extended Bus cycle	LOW
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	
63	BVD1	O	Bat. Volt. Detect 1	
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:

- 1. RDY/BSY is an open drain output, external pull-up resistor is required.
- 2. Shows density for which specified address bit is MSB. Higher order address bits are no connects (i.e., 4MB A21 is MSB A22 - A25 are NC).

Mechanical





Card Signal Description

Symbol	Type	Name and Function
A0 - A25	INPUT	ADDRESS INPUTS: A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not decoded since the card is x16 only. The memory will wrap at the card density boundary. The system should not try to access memory beyond the card density. The upper addresses are not connected.
DQ0 - DQ15	INPUT/OUTPUT	DATA INPUT/OUTPUT: DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ0 - DQ7 constitute the lower (even) byte and DQ8 - DQ15 the upper (odd) byte. DQ15 is the MSB.
CE1#, CE2#	INPUT	CARD ENABLE 1 AND 2: CE1# enables even byte accesses, CE2# enables odd byte accesses. Odd byte (DQ8 - DQ15) can not be accessed on DQ0 - DQ7.
OE#	INPUT	OUTPUT ENABLE: Active low signal enabling read data from the memory card.
WE#	INPUT	WRITE ENABLE: Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	READY/BUSY OUTPUT: Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. Open Drain output, pull-up resistor is required.
CD1#, CD2#	OUTPUT	CARD DETECT 1 and 2: Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins.
WP	OUTPUT	WRITE PROTECT: This signal is pulled low internally. This signifies write protect = "off " for all cases.
VPP1, VPP2	N.C.	PROGRAM/ERASE POWER SUPPLY: Not connected for 5V only card.
VCC		CARD POWER SUPPLY: 5.0V for all internal circuitry.
GND		GROUND: for all internal circuitry.
REG#	INPUT	ATTRIBUTE MEMORY SELECT : only used with cards built with optional attribute memory.
RST	INPUT	RESET: Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down signal for the memory array.
WAIT#	OUTPUT	WAIT: This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	BATTERY VOLTAGE DETECT: These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	VOLTAGE SENSE: Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V, 16 bit card has been inserted.
RFU		RESERVED FOR FUTURE USE
N.C.		NO INTERNAL CONNECTION TO CARD: pin may be driven or left floating

Functional Truth Table

READ function

Function Mode	/CE2	/CE1	/OE	/WE
Standby Mode	H	H	X	X
Low Byte Access	H	L	L	H
Word Access (16 bits)	L	L	L	H
Odd-Byte Only Access	L	H	L	H

Common Memory

	/REG	D15-D8	D7-D0
	X	High-Z	High-Z
	H	High-Z	Even-Byte
	H	Odd-Byte	Even-Byte
	H	Odd-Byte	High-Z

Attribute Memory

	/REG	D15-D8	D7-D0
	X	High-Z	High-Z
	L	High-Z	Even-Byte
	L	Not Valid	Even-Byte
	L	Not Valid	High-Z

WRITE function

Function Mode	/CE2	/CE1	/OE	/WE
Standby Mode	H	H	X	X
Low Byte Access	H	L	H	L
Word Access (16 bits)	L	L	H	L
Odd-Byte Only Access	L	H	H	L

	/REG	D15-D8	D7-D0
	X	X	X
	H	X	Even-Byte
	H	Odd-Byte	Even-Byte
	H	Odd-Byte	X

	/REG	D15-D8	D7-D0
	X	X	X
	L	X	Even-Byte
	L	X	Even-Byte
	L	X	X

**Absolute Maximum Ratings** ⁽¹⁾

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Storage Temperature	-40°C to +85 °C
Voltage on any pin relative to VSS	-0.5V to VCC+0.5V
VCC supply Voltage relative to VSS	-0.5V to +7.0V

Note:

(1) Stress greater than those listed under “Absolute Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics ⁽¹⁾

Symbol	Parameter	Density (Mbytes)	Notes	Typ ⁽³⁾	Max	Units	Test Conditions
I _{CCR}	VCC Read Current	4,8,16			40	mA	VCC = 5.25V tcycle = 150ns
I _{CCW}	VCC Program Current	4,8,16			65	mA	
I _{CCE}	VCC Erase Current	4,8,16			65	mA	
I _{CCS}	VCC Standby Current For max capacity 16MB	4,8,16	2	10	100	μA	VCC = 5.25V Control Signals = VCC

CMOS Test Conditions: VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

Notes:

1. All currents are for Byte mode and are RMS values unless otherwise specified.
2. Control Signals: CE₁#, CE₂#, OE#, WE#, REG#.
3. Typical: VCC = 5V, T = +25C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I _{LI}	Input Leakage Current	1,2		±20	μA	VCC = VCCMAX Vin =VCC or VSS
I _{LO}	Output Leakage Current	1		±20	μA	VCC = VCCMAX Vout =VCC or VSS
V _{IL}	Input Low Voltage	1	0	0.8	V	
V _{IH}	Input High Voltage	1	3.85	VCC+0.5	V	
V _{OL}	Output Low Voltage	1		0.4	V	IOL = 3.2mA
V _{OH}	Output High Voltage	1	VCC-0.4	VCC	V	IOH = -2.0mA
V _{LKO}	VCC Erase/Program Lock Voltage	1	3.2	4.2	V	

Notes:

1. Values are the same for byte and word wide modes for all card densities.
2. Exceptions: Leakage currents on CE₁#, CE₂#, OE#, REG# and WE# will be < 500 μA when VIN = GND due to internal pull-up resistors. Leakage currents on RST will be <150μA when VIN=VCC due to internal pull-down resistor.



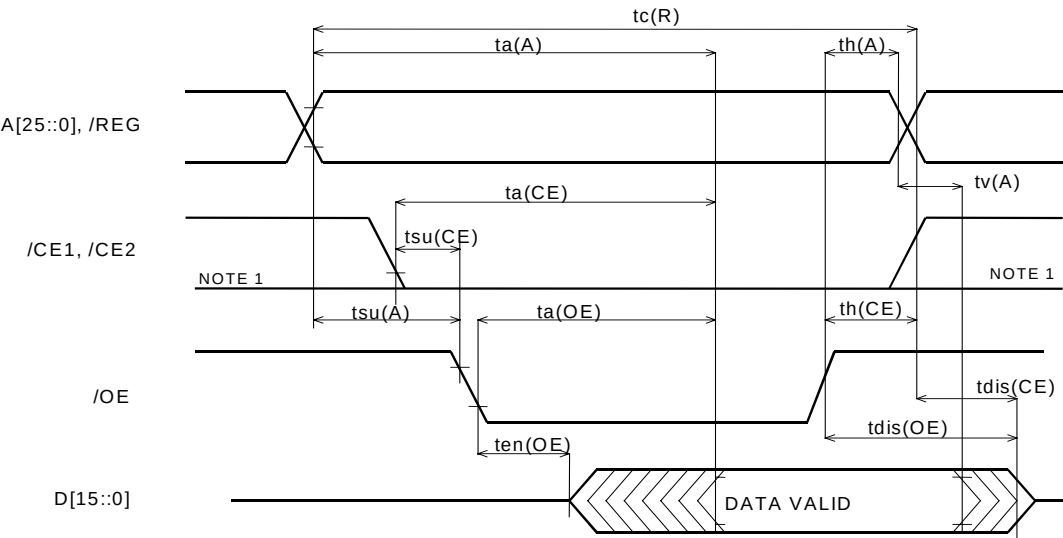
AC Characteristics

Read Timing Parameters

		150ns		
SYMBOL (PCMCIA)	Parameter	Min	Max	Unit
$t_c(R)$	Read Cycle Time	150		ns
$t_a(A)$	Address Access Time		150	ns
$t_a(CE)$	Card Enable Access Time		150	ns
$t_a(OE)$	Output Enable Access Time		75	ns
$t_{su}(A)$	Address Setup Time		20	ns
$t_{su}(CE)$	Card Enable Setup Time		0	ns
$t_h(A)$	Address Hold Time		20	ns
$t_h(CE)$	Card Enable Hold Time		20	ns
$t_v(A)$	Output Hold from Address Change		0	ns
$t_{dis}(CE)$	Output Disable Time from CE#		75	ns
$t_{dis}(OE)$	Output Disable Time from OE#		75	ns
$t_{en}(CE)$	Output Enable Time from CE#	5		ns
$t_{en}(OE)$	Output Enable Time from OE#	5		ns
$t_{rec(RST)}^{(2)}$	Power Down recovery to Output Delay. VCC = 5V		500	ns

- Notes:
- 1. AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.
 - 2. Minimum width of reset pulse 500ns.

Read Timing Diagram



Note: Signal may be high or low in this area

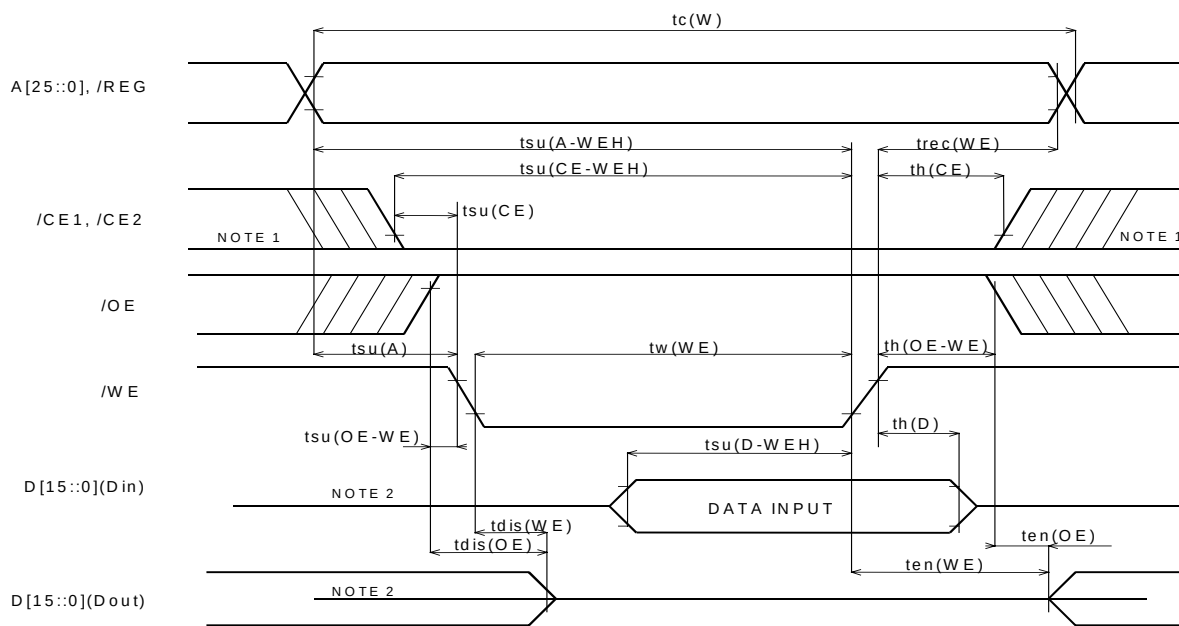


Write Timing Parameters

SYM (PCMCIA)	Parameter	150ns		Unit
		Min	Max	
t_{cW}	Write Cycle Time	150		ns
$t_w(WE)$	Write Pulse Width	80		ns
$t_{su}(A)$	Address Setup Time	20		ns
$t_{su}(A-WEH)$	Address Setup Time for WE#	100		ns
$t_{su}(CE-WEH)$	Card Enable Setup Time for WE#	100		ns
$t_{su}(D-WEH)$	Data Setup Time for WE#	50		ns
$t_h(D)$	Data Hold Time	20		ns
$t_{rec}(WE)$	Write Recover Time	20		ns
$t_{dis}(WE)$	Output Disable Time from WE#		75	ns
$t_{dis}(OE)$	Output Disable Time from OE#		75	ns
$t_{en}(WE)$	Output Enable Time from WE#	5		ns
$t_{en}(OE)$	Output Enable Time from OE#	5		ns
$t_{su}(OE-WE)$	Output Enable Setup from WE#	10		ns
$t_h(OE-WE)$	Output Enable Hold from WE#	10		ns
$t_{su}(CE)$	Card Enable Setup Time from OE#	0		ns
$t_h(CE)$	Card Enable Hold Time	20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Write Timing Diagram



Notes:

- Signal may be high or low in this area.
- When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

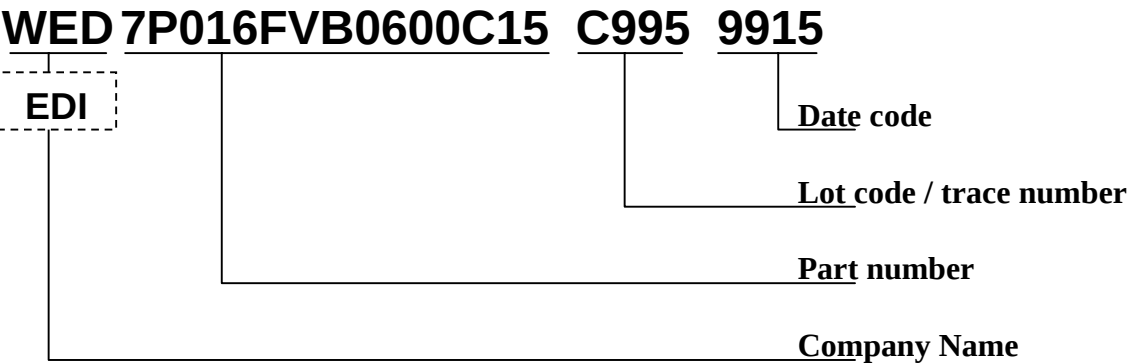
Data Write and Erase Performance ^(1,3)

VCC = 5V ± 5%, T_A = 0C to + 70C

Parameter	Notes	Min	Typ ⁽¹⁾	Max	Units	Comments
Word/Byte Program time	2,4		7µs	1ms		Note 2, 4
Block Erase Time	2		1	15	sec	Excludes 00H prog. prior to erasure

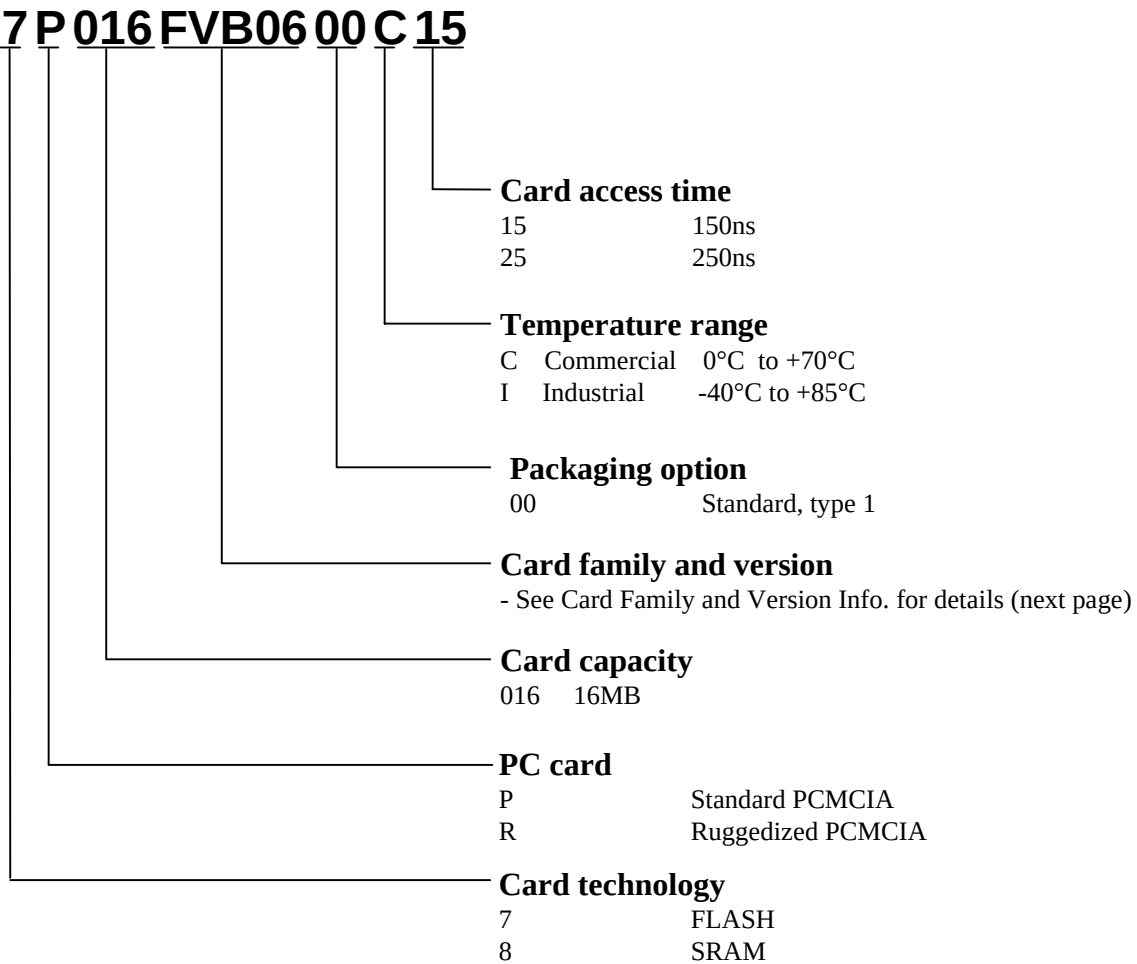
- Notes:**
- 1. Typical: Nominal voltages and T_A = 25C.
 - 2. Excludes system overhead.
 - 3. Valid for all speed options.
 - 4. To maximize system performance RDY/BSY# signal or component status register should be polled.

PRODUCT MARKING



Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING



Ordering Information

7P XXX FVB YY SS T ZZ

where

XXX:	004	4MB
	008	8MB
	016	16MB
YY:	05	29F016 base
	06	29F016 w/attribute memory
SS:	00	WEDC Silkscreen
	01	Blank Housing, Type I
	02	Blank Housing, Type I Recessed
T:	C	Commercial
	I	Industrial
ZZ:	15	150ns

Part Number Table - Common Options

EDI Part Number	Density	Speed	Flash Component	Attribute Memory
AMD Based Cards				
EDI7P004FVB0500C15	4MB	150ns	29F016	NO
EDI7P004FVB0600C15	4MB	150ns	29F016	2K EEPROM
EDI7P008FVB0500C15	8MB	150ns	29F016	NO
EDI7P008FVB0600C15	8MB	150ns	29F016	2K EEPROM
EDI7P016FVB0500C15	16MB	150ns	29F016	NO
EDI7P016FVB0600C15	16MB	150ns	29F016	2K EEPROM



CIS Data - Cards Based on 29F016 Components with Attribute Memory

Address	Value	Description
00H	01H	CISTPL_DEVICE
02H	03H	TPL_LINK
04H	53H	FLASH = 150ns (device writable)
06H	0EH	CARD SIZE: 4MB
	1EH	8MB
	3EH	16MB
08H	FFH	END OF TUPLE
0AH	18H	CISTPL_JEDEC_C
0CH	02H	TPL_LINK
0EH	01H	AMD - ID
10H	ADH	29F016 - ID
12H	17H	CISTPL_DEVICE_A
14H	04H	TPL_LINK
16H	42H	EEPROM - 250ns
18H	01H	Device Size = 2KBytes
1AH	FFH	END OF TUPLE
1CH	1EH	CISTPL_DEVICEGEO
1EH	06H	TPL_LINK
20H	02H	DGTPL_BUS
22H	11H	DGTPL_EBS
24H	01H	DGTPL_RBS
26H	01H	DGTPL_WBS
28H	01H	DGTPL_PART
2AH	01H	FLASH DEVICE NON-INTERLEAVED
2CH	20H	CISTPL_MANFID
2EH	04H	TPL_LINK
30H	F6H	EDI TPLMID_MANF: LSB
32H	01H	EDI TPLMID_MANF: MSB
34H	00H	LSB: Number Not Assigned
36H	00H	MSB: Number Not Assigned
38H	15H	CISTPL_VERS1
3AH	47H	TPL_LINK
3CH	05H	TPLL1_MAJOR
3EH	00H	TPLL1_MINOR
40H	45H	E
42H	44H	D
44H	49H	I
46H	37H	7
48H	50H	P
4AH	30H	0
4CH	30H	0
4EH		x
50H	46H	F
52H	56H	V
54H	42H	B
56H	30H	0
58H	36H	6
5AH	2DH	-
5CH	2DH	-
5EH	2DH	-
60H		y
62H		y

Address	Value	Description
64H	20H	SPACE
66H	00H	END TEXT
68H	43H	C
6AH	4FH	O
6CH	50H	P
6EH	59H	Y
70H	52H	R
72H	49H	I
74H	47H	G
76H	48H	H
78H	54H	T
7AH	20H	SPACE
7CH	45H	E
7EH	4CH	L
80H	45E	E
82H	43H	C
84H	54H	T
86H	52H	R
88H	4FH	O
8AH	4EH	N
8CH	49H	I
8EH	43H	C
90H	20H	SPACE
92H	44H	D
94H	45H	E
96H	53H	S
98H	49H	I
9AH	47H	G
9CH	4EH	N
9EH	53H	S
A0H	20H	SPACE
A2H	49H	I
A4H	4EH	N
A6H	43H	C
A8H	4FH	O
AAH	52H	R
ACH	50H	P
AEH	4FH	O
B0H	52H	R
B2H	41H	A
B4H	54H	T
B6H	45H	E
B8H	44H	D
BAH	20H	SPACE
BCH	00H	END TEXT
BEH	31H	1
C0H	39H	9
C2H	39H	9
C4H	37H	7
C6H	00H	END TEXT
C8H	FFH	END OF TUPLE
CAH	FFH	CISTPL_END
CCH	00H	INVALID ADDRESS

Note: In the part number, value x will be substituted with the proper capacity and value yy with the proper card speed.



Revision History

revision	rev date	description
0	Jan-98	initial release
1	Jun-99	logo/name change
2	May-00	added page 8
3	Aug-00	Changed pg. 5&6

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