

NE56610/11/12 Series

System Reset

Rev 0

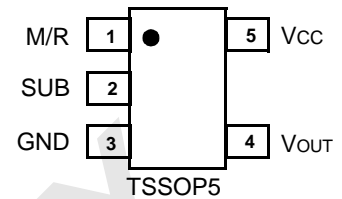
February, 2001

Preliminary Product Specification

General Description

The NE56610/11/12 series is a family of devices designed to generate a reset signal for a variety of microprocessor and logic systems. Accurate reset signals are generated during momentary power interruptions or when ever power supply voltages sag to intolerable levels. The NE56610/11/12 incorporates an internal timer to provide reset delay and ensure proper operating voltage has been attained. In addition, a manual reset pin is available. An Open Collector output topology is incorporated to provide adaptability for a wide variety of logic and microprocessor systems.

NE56610/11/12 is available in the TSSOP5 surface mount package.



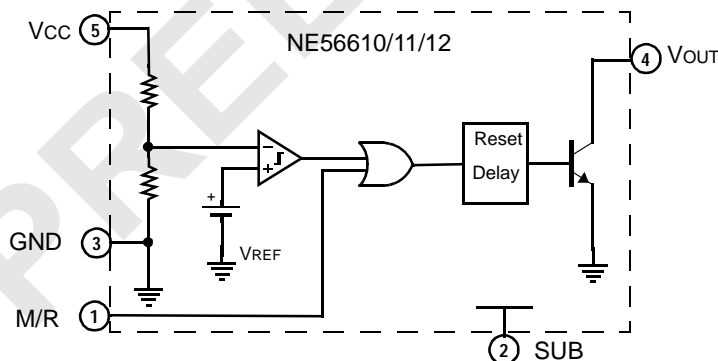
Features

- 12V DC Maximum Operating Voltage
- Low Operating Voltage (0.65 V)
- Internal Reset Delay Timer
 - NE56610 (50 mS Typical)
 - NE56611 (100mS Typical)
 - NE56612 (200mS Typical)
- Offered in Reset Thresholds of 2.0, 2.7, 2.8, 2.9, 3.0, 3.1, 4.2, 4.3, 4.4, 4.5, 4.7 V DC
- Available in SSOP5 Surface Mount Package
- Manual Reset Input

Applications

- Micro-Computer Systems
- Logic Systems
- Battery Monitoring Systems
- Back-Up Power Supply Circuits
- Voltage Detection Circuits
- Mechanical Reset Circuits

Simplified Device Diagram



Ordering Information

Description	Temperature Range	Order Code	DWG#
5-pin SOT23 (TSSOP5) plastic surface mount	-20 - +75 °C	NE56610-xxGW	TSSOP5
System Reset (100mS Typical Internal Reset Delay)	-20 - +75 °C	NE56611-xxGW	TSSOP5
System Reset (200mS Typical Internal Reset Delay)	-20 - +75 °C	NE56612-xxGW	TSSOP5

Note: Each device has 6 (six) detection voltage options, indicated by the -xx on the order code:

XX	Detect Voltage (Typ.)	XX	Detect Voltage (Typ.)
-25	2.5	-39	3.9
-27	2.7	-42	4.2
-29	2.9	-45	4.5

Pin Designation and Description

Pin Designation	Pin No	Pin Name	Function
	1	M/R	Manual Reset input. Connect to ground when not using.
	2	SUB	Substrate Pin. Connect to ground.
	3	GND	Ground
	4	VOUT	Reset High Output pin
	5	Vcc	Positive Power Supply Input

Maximum Ratings

Parameter	Symbol	Rating	Unit
Storage Temperature Range	TSTG	-40 - +125	°C
Ambient Operating Temperature Range	TA	-20 - +75	°C
Power Supply Voltage	VCC max.	-0.3 - +12	V
Manual Reset Input Voltage	VRES max	-0.3 - +12	V
Power Dissipation	Pd	150	mW

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Ambient Operating Temperature Range	TA	-20 - +75	°C
Power Supply Voltage	VCC max.	-0.3 - +12	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise specified.

Note 1: Unless otherwise stated, M/R pin should always be connected to ground.

Parameter	Symbol	Test Circuit	Part#	Min	Typ	Max	Unit
Threshold Detection V _{CC} Falling R _L = 470Ω, V _{OL} ≤ 0.4V	V _s	1	-45	4.3	4.5	4.7	V
			-42	4.0	4.2	4.4	
			-39	3.7	3.9	4.1	
			-29	2.75	2.90	3.05	
			-27	2.55	2.70	2.85	
			-25	2.35	2.50	2.65	
Hysteresis Voltage V _{CC} = Rising then Falling ($\Delta V_s = V_{SH} - V_{SL}$) R _L = 470Ω	ΔV_s	1	All	30	50	100	mV
Threshold Temperature Coefficient R _L = 470Ω, T _A = -20°C - +75°C	T _C / V _s	1	All		±0.01		% / °C
Low-level Output Voltage V _{CC} = V _s min. -0.05V, R _L = 470Ω	V _{OL}	1	All		0.1	0.4	V
Output Leakage Current V _{CC} = 10V	I _{OH}	1	All			±0.1	μA
Circuit ON Current V _{CC} = V _s min. -0.05V, R _L = ∞	I _{CCL}	1	All		300	500	μA
Circuit OFF Current V _{CC} = V _s typ./0.85V, R _L = ∞	I _{CCH}	1	All		15	25	μA
Reset Delay Time High (see note 1) R _L = 4.7kΩ C _L = 100pF	T _{DLH}	2	NE56610	30	50	75	mS
			NE56611	60	100	150	
			NE56612	120	200	300	
Reset Delay Time Low (see note 2) R _L = 4.7kΩ, C _L = 100pF	T _{PHL}	2	All		20		mS
Operating Supply Voltage R _L = 4.7kΩ, V _{OL} ≤ 0.4V	V _{OPL}	1	All		0.65	0.85	V
Output ON Current 1 V _{CC} = V _s min. -0.05V, R _L = 0	I _{OL1}	1	All	8			mA
Output On Current 2 V _{CC} = V _s min. -0.05V, R _L = 0 T _A = -20°C - +75°C	I _{OL2}	1	All	6			mA
M/R Threshold High	V _{M/RH}		All	2.0			V
M/R Threshold High V _{M/RH} = 2.0V	I _{M/RH}		All		10	60	μA
M/R Threshold Low	V _{M/RL}		All	-0.3		0.8	V

NOTES:

- T_{DLH} measured with V_{CC} = (V_s typ. -0.4V) and abruptly transitioning to (V_s typ. +0.4V). T_{DLH} is duration from V_{CC} transition high to output transition high.
- T_{DHL} measured with V_{CC} ≥ (V_s typ. +0.4V) and abruptly transitioning to (V_s typ. -0.4V). T_{DHL} is duration from V_{CC} transition low to output transition low.
- Ramp M/R voltage until Output Reset goes low.

Typical Performance Curves

Figure 1. Normalized Detection versus Temperature

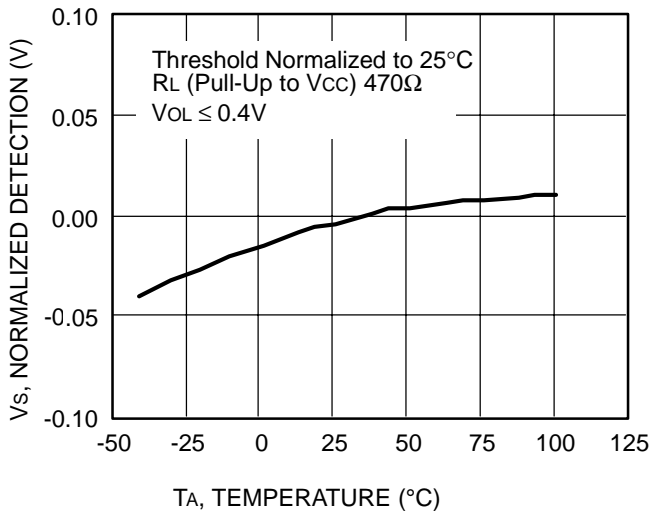


Figure 2. Circuit ON Current versus Temperature

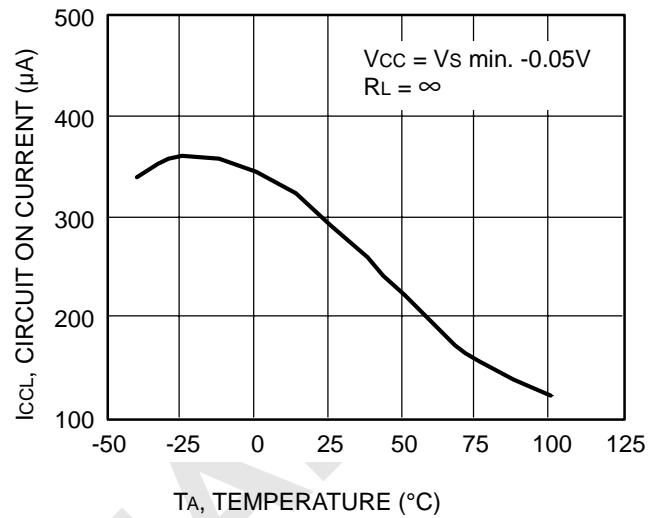


Figure 3. Detection Hysteresis versus Temperature

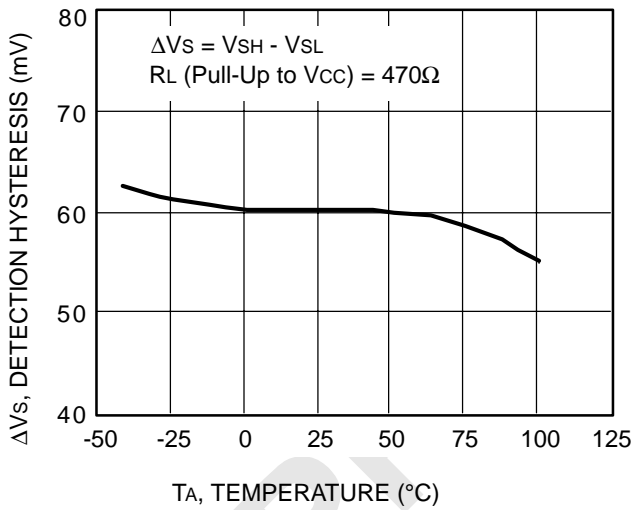


Figure 4. Circuit OFF Current versus Temperature

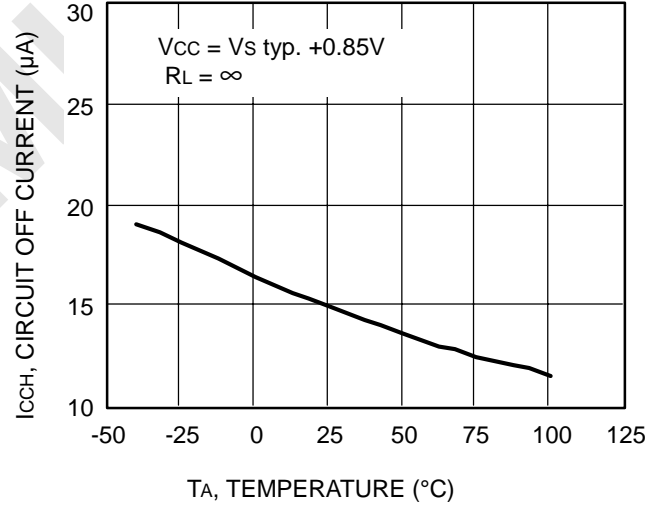


Figure 5. Low-Level Output Voltage versus Temperature

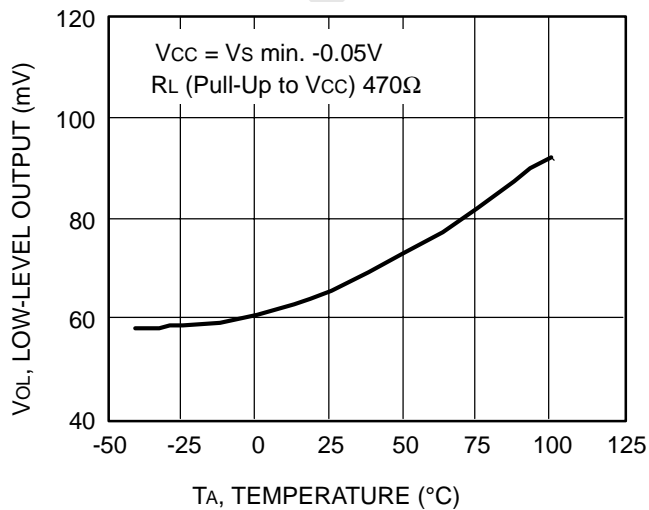
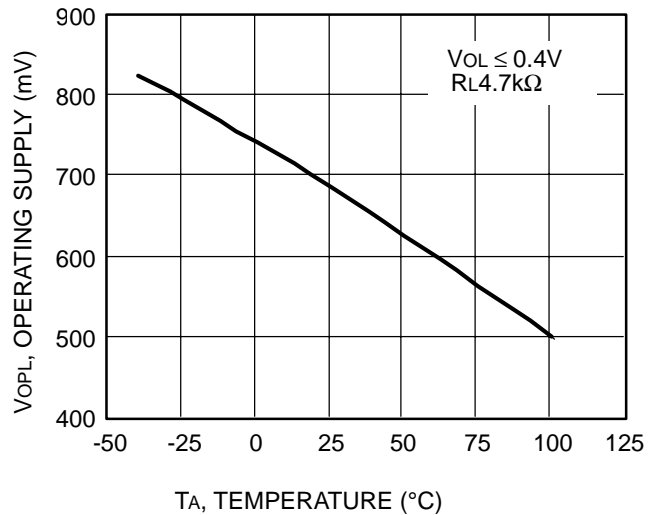


Figure 6. Operating Supply Voltage versus Temperature



Typical Performance Curves (continued)

Figure 7. Output ON Current versus Temperature

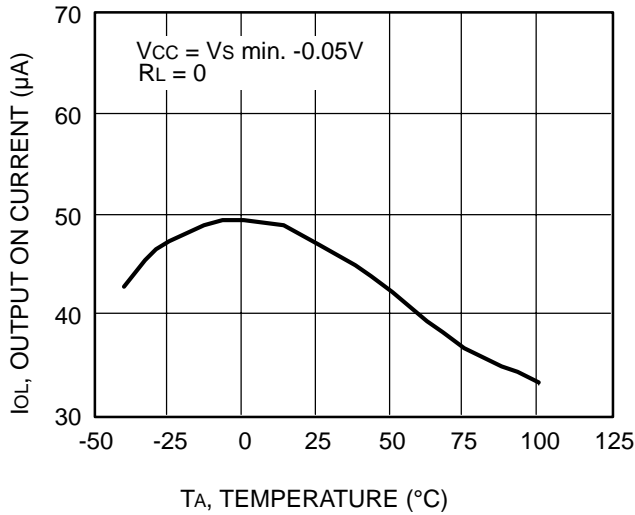


Figure 8. M/R Input High Current versus Temperature

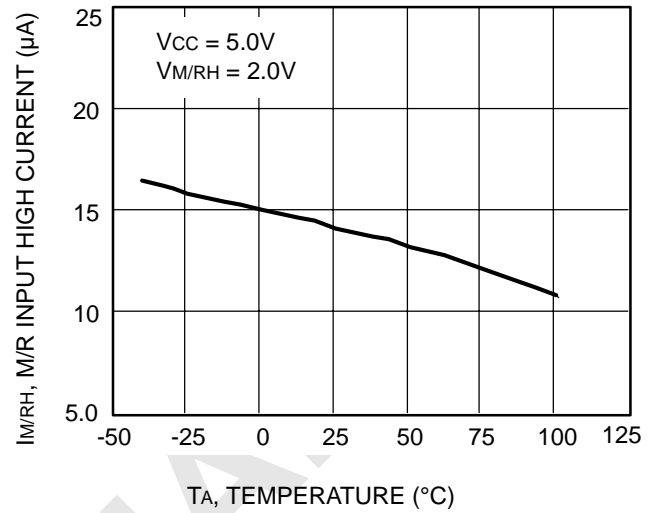


Figure 9. Reset Delay Time High versus Temperature

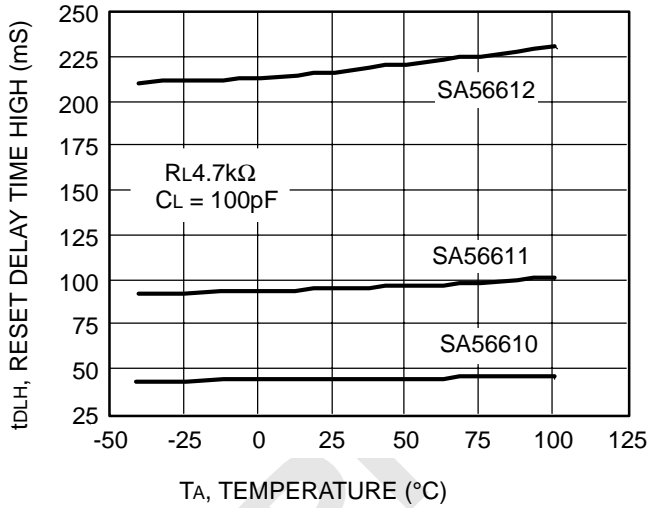


Figure 10. M/R Threshold High versus Temperature

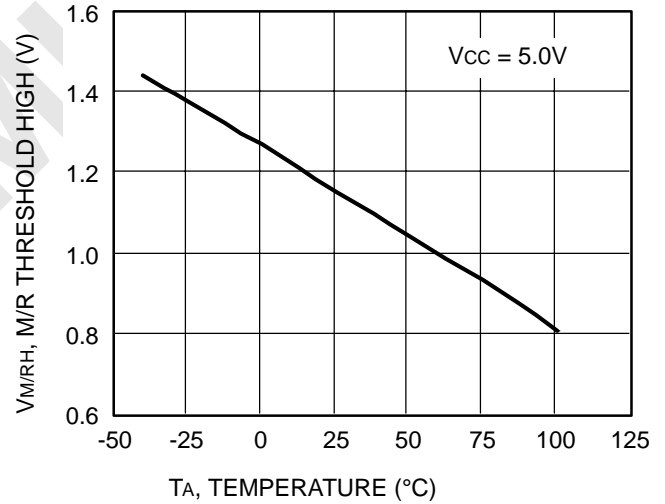


Figure 11. Reset Delay Time Low versus Temperature

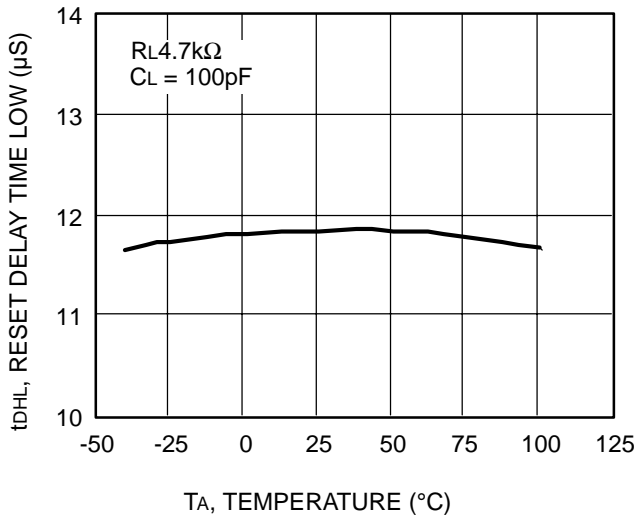
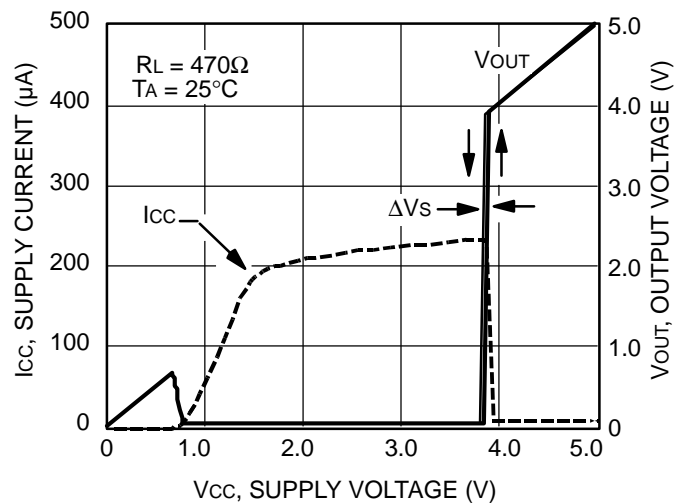
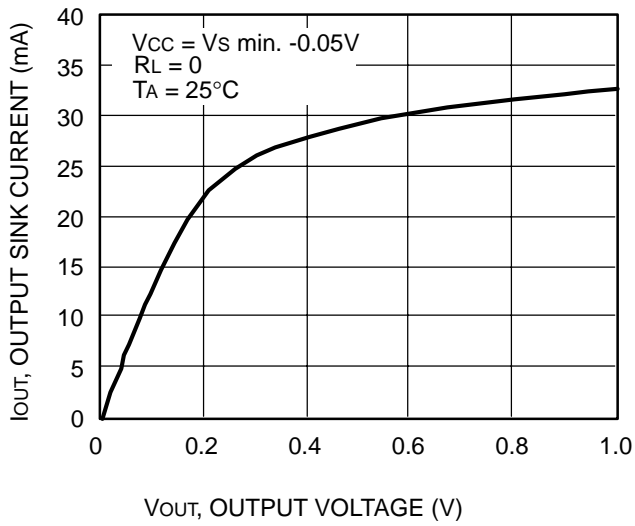


Figure 12. Icc and Vout versus Supply Voltage



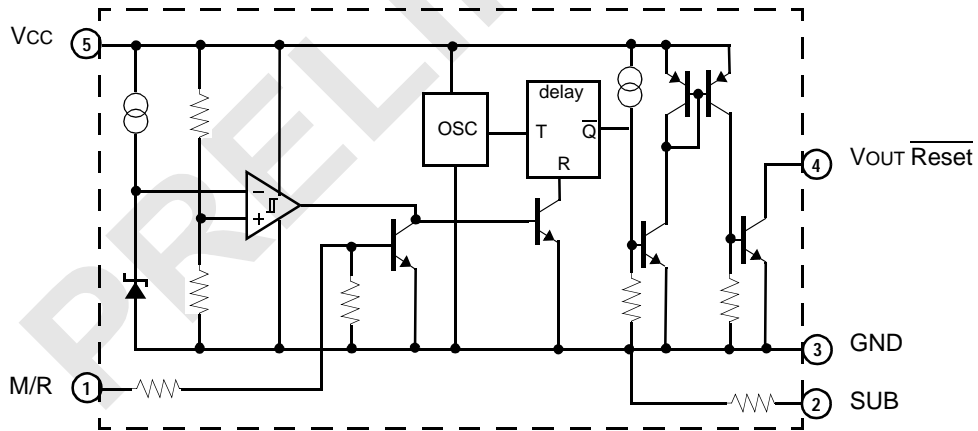
Typical Performance Curves (continued)

Figure 13. Output Sink Current versus Output Voltage



Technical Discussion

Figure 14. Functional Schematic



TIMING DIAGRAM

The Timing Diagram shown in Figure 15 depicts the operation of the device. Letters indicate events on the Time axis.

A: At start-up, event "A", the Vcc and Reset voltages begin to rise. Also the Reset voltage initially rises but then abruptly returns to a low state. This is due to Vcc reaching the level (approximately 0.8V) that activates the internal bias circuitry.

B: At event "B", the "H" transport delay time (TPLH) is initiated. This is caused by and coincident to Vcc reaching the threshold level of VSH. At this level the device is in full operation. The Reset output remains off as Vcc rises above VSH. This is normal.

C: At event "C" Vcc is above the undervoltage detect threshold and the "H" transport delay time (TPLH) has elapsed. At this point the device removes the hold on the VOUT reset. VOUT Reset goes high.

In a microprocessor based system these events remove the reset from the microprocessor, allowing it to function normally.

D-E: At "D", Vcc begins to ramp down causing VOUT to follow it. Vcc continues to sag until the VSL undervoltage threshold is reached at "E". At that time, reset signal is generated (VOUT Reset goes low).

E-F: Between "E" and "F", Vcc recovers and starts increasing.

F: At "F", Vcc reaches the VSH upper threshold. Once again, the "H" transport delay time (TPLH) is initiated.

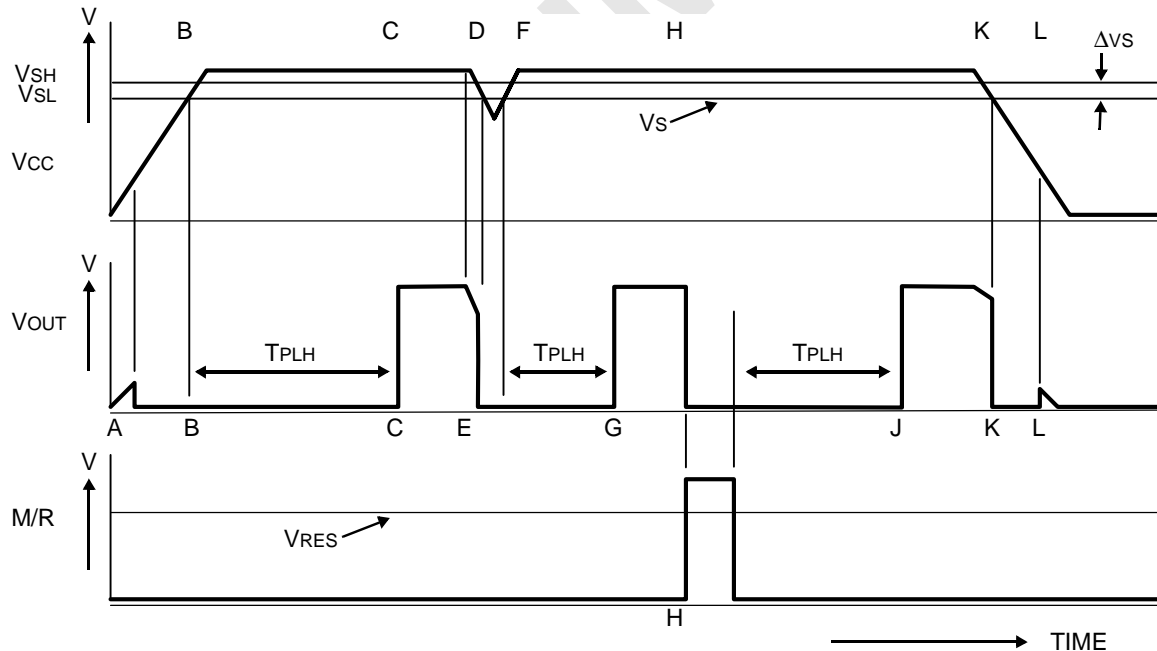
G: At "G", Vcc is above the undervoltage detect threshold and the "H" transport delay time (TPLH) has elapsed. At this point the device removes the hold on the VOUT reset. VOUT Reset goes high.

H-J: At event "H", Vcc is normal, but a manual reset signal from the logic device is applied at the M/R pin. With the falling edge of the manual reset signal, the "H" transport delay time (TPLH) is initiated. At "J", transport delay time (TPLH) has elapsed and the Vout reset goes high.

K: At event "K" Vcc sags to the point where the VSL undervoltage threshold point is reached and at that level VOUT reset goes low.

L: At event "L" the Vcc voltage has deteriorated to a level where normal internal circuit bias is no longer able to maintain a VOUT reset and as a result may exhibit a slight rise to something less than 0.8V. As Vcc decays even further, VOUT reset also decreases to zero.

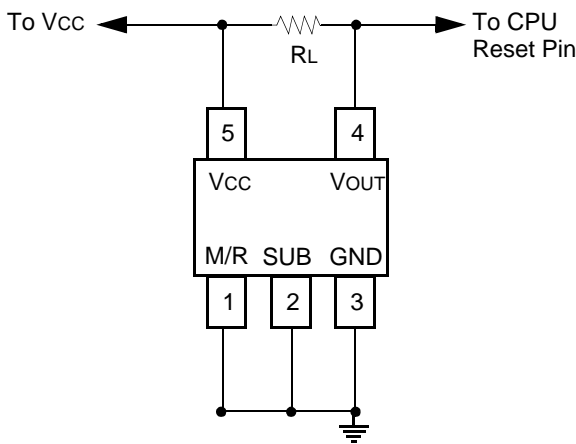
Figure 15. Timing Diagram



Application Information

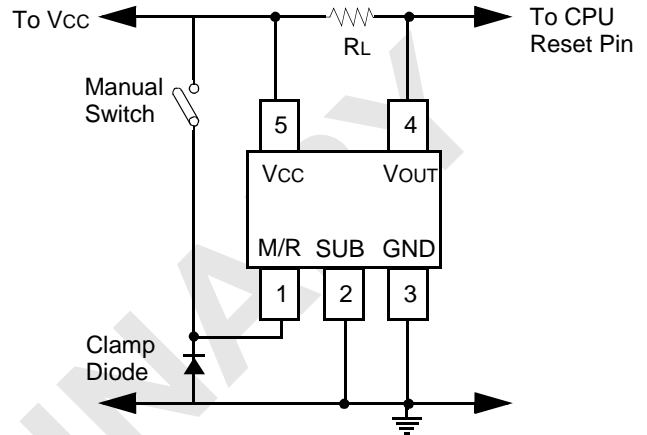
When the manual reset is not needed, the M/R, manual reset pin is connected to ground as shown in Figure 16 - Typical Hard Reset Circuit. A capacitor connected from VCC to ground is recommended when the VCC supply impedance is appreciably high. This may be the situation with a poor quality or aged battery.

Figure 16. Typical Hard Reset Circuit



The second example, shown in Figure 17 - Manual Reset Circuit, incorporates a manual reset switch from the M/R pin to VCC. When the manual switch is closed, VOUT reset is logic high. Conversely, when it is opened, VOUT reset is logic low. As a precaution a clamp diode is placed from the M/R pin to ground to insure that the pin does not go below - 0.3V.

Figure 17. Manual Reset Circuit



Test Circuits

Figure 16. Test Circuit 1

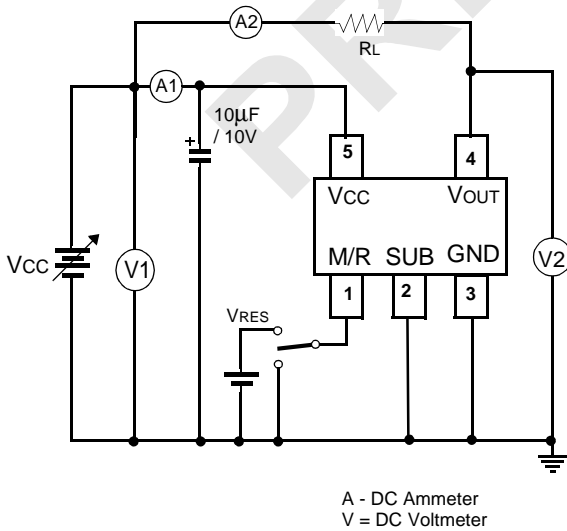
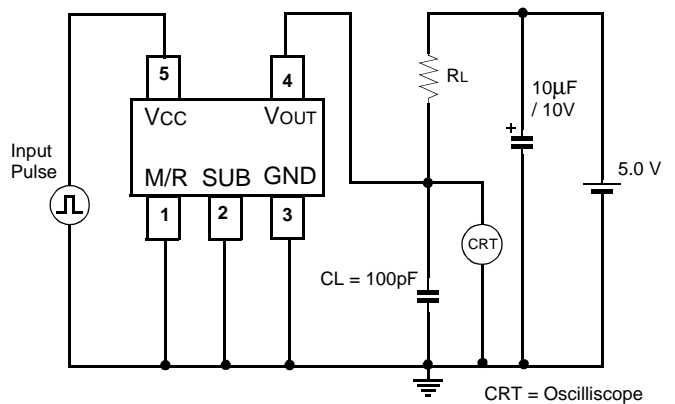
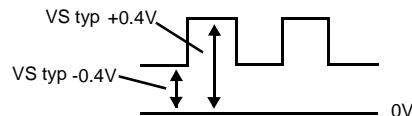


Figure 17. Test Circuit 2

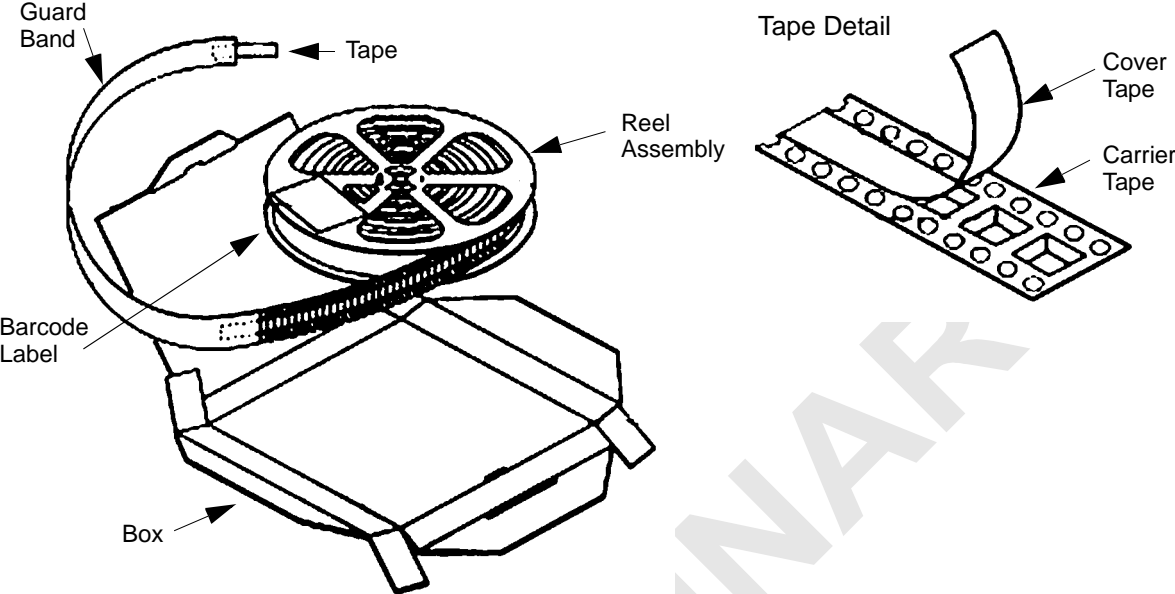


Input Pulse



Packing Method

The NE56610/11/12 is packed in reels, as shown here



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PRELIMINARY