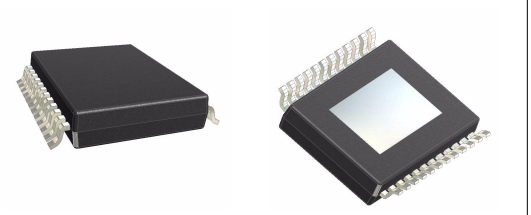
VND600PEP

DOUBLE CHANNEL HIGH SIDE SOLID STATE RELAY

TARGET SPECIFICATION

TYPE	$R_{DS(on)}$	I_{lim}	V_{CC}
VND600PEP	30mΩ	25A	36V

- DC SHORT CIRCUIT CURRENT: 25A
- CMOS COMPATIBLE INPUTS
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT-DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST: LOSS OF GROUND AND LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (*)



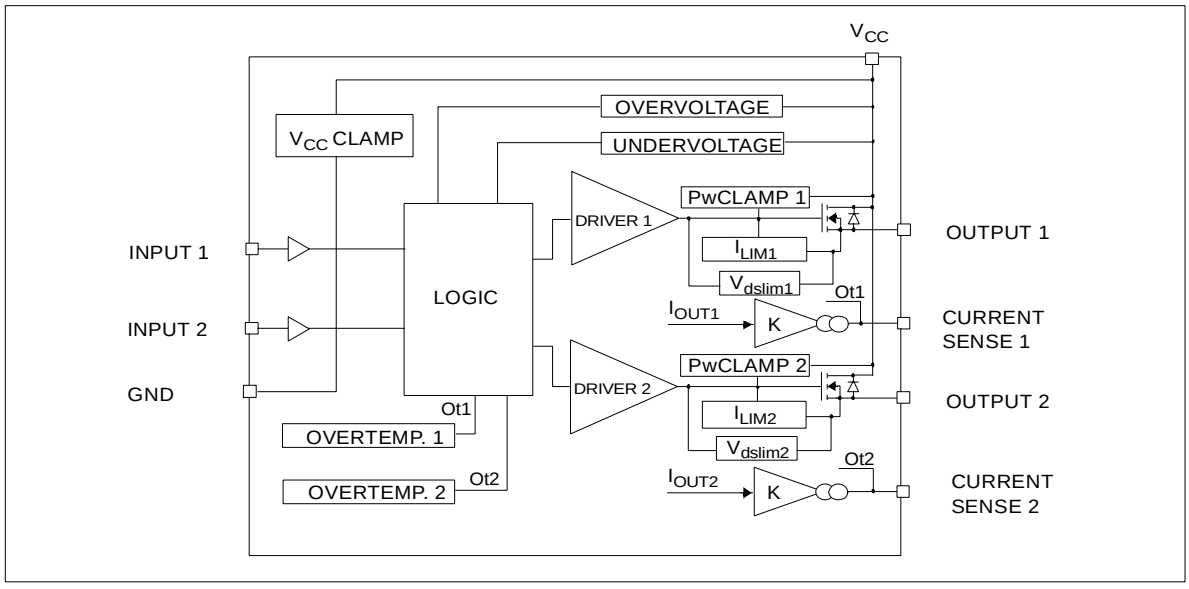
PowerSSO-24

ORDER CODES		
PACKAGE	**TUBE**	**T&R**
PowerSSO-24	VND600PEP	VND600PEP13TR

DESCRIPTION

The VND600PEP is a monolithic device made using STMicroelectronics VIPower M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device has two channels in high side configuration; each channel has an analog sense output on which the sensing current is proportional (according to a known ratio) to the corresponding load current. Built-in thermal shut-down and outputs current limitation protect the chip from over temperature and short circuit. Device turns off in case of ground pin disconnection.

BLOCK DIAGRAM

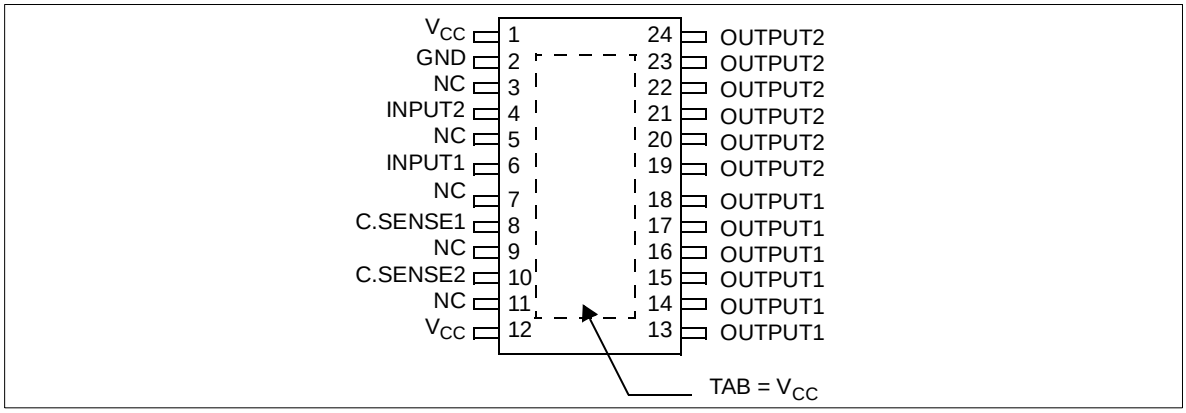


(*) See application schematic at page 8

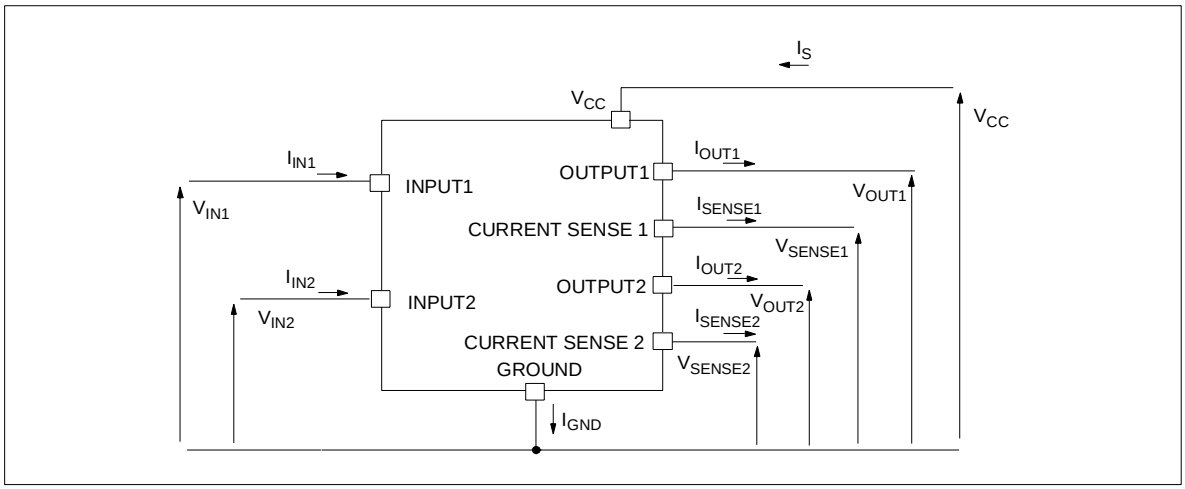
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	Output current	Internally limited	A
I_R	Reverse output current	-21	A
I_{IN}	Input current	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	-3 +15	V V
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - CURRENT SENSE - OUTPUT - V_{CC}	 4000 2000 5000 5000	 V V V V
P_{tot}	Power dissipation at T_c=25°C	96	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{thj\text{-}case}$ (1)	Thermal resistance junction-case	(MAX)	1.8	°C/W
$R_{thj\text{-}case}$ (2)	Thermal resistance junction-case	(MAX)	1.3	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	(MAX)	60 (*)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 1cm^2 of Cu (at least 35µm thick).

Note: (1) one channel ON - (2) two channels ON

ELECTRICAL CHARACTERISTICS ($8V<V_{CC}<36V$; $-40°C<T_j<150°C$; unless otherwise specified)

(Per each channel)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC} (**)	Operating supply voltage		5.5	13	36	V
V_{USD} (**)	Undervoltage shutdown		3	4	5.5	V
V_{OV} (**)	Overvoltage shutdown		36			V
R_{ON}	On state resistance	I_{OUT}=5A; T_j=25°C			30	mΩ
		I_{OUT}=5A; T_j=150°C			60	mΩ
		I_{OUT}=3A; V_{CC}=6V			100	mΩ
V_{clamp}	Clamp Voltage	I_{CC}=20mA (see note 3)	41	48	55	V
I_S (**)	Supply current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V		12	40	µA
		Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V; T_j=25°C		12	25	µA
		On state; V_{IN}=5V; V_{CC}=13V; I_{OUT}=0A; R_{SENSE}=3.9kΩ			6	mA
$I_{L(off1)}$	Off State Output Current	V_{IN}=V_{OUT}=V_{SENSE}=0V	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=V_{SENSE}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=V_{SENSE}=0V; V_{CC}=13V; T_j =125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=V_{SENSE}=0V; V_{CC}=13V; T_j =25°C			3	µA

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	R_L=2.6Ω (see figure 1)		30		µs
$t_{d(off)}$	Turn-on delay time	R_L=2.6Ω (see figure 1)		30		µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L=2.6Ω (see figure 1)		See relative diagram		V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L=2.6Ω (see figure 1)		See relative diagram		V/µs

PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	DC short circuit current	V_{CC}=13V	25	40	70	A
		5.5V<V_{CC}<36V			70	A
T_{TSD}	Thermal shut-down temperature		150	175	200	°C
T_R	Thermal reset temperature		135			°C
T_{HYST}	Thermal hysteresis		7	15		°C
V_{demag}	Turn-off output voltage clamp	I_{OUT}=2A; V_{IN}=0V; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.5A; T_j= -40°C...+150°C		50		mV

(**) Per device.

ELECTRICAL CHARACTERISTICS (continued)

CURRENT SENSE ($9V \leq V_{CC} \leq 16V$) (See figure 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2}=0.5A; V_{SENSE}=0.5V; other channels open; T_j= -40°C...150°C	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	I_{OUT1} or I_{OUT2}=0.5A; V_{SENSE}=0.5V; other channels open; T_j= -40°C...150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2}=5A; V_{SENSE}=4V; other channels open; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current Sense Ratio Drift	I_{OUT1} or I_{OUT2}=5A; V_{SENSE}=4V; other channels open; T_j=-40°C...150°C	-6		+6	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2}=15A; V_{SENSE}=4V; other channels open; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current Sense Ratio Drift	I_{OUT1} or I_{OUT2}=15A; V_{SENSE}=4V; other channels open; T_j=-40°C...150°C	-6		+6	%
$V_{SENSE1,2}$	Max analog sense output voltage	V_{CC}=5.5V; $I_{OUT1,2}$=2.5A; R_{SENSE}=10kΩ V_{CC}>8V, $I_{OUT1,2}$=5A; R_{SENSE}=10kΩ	2 4			V V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC}=13V; R_{SENSE}=3.9kΩ		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in overtemperature condition	V_{CC}=13V; T_j>T_{TSD}; All Channels Open		400		Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE} (see note 4)			500	µs

LOGIC INPUT (Channels 1,2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	V_{IN}=1.25V	1			µA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	High level input current	V_{IN}=3.25V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}=-1mA	6	6.8 -0.7	8	V V

Note 3: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.
Note 4: current sense signal delay after positive input slope.

Note: Sense pin doesn't have to be left floating.

TRUTH TABLE (per channel)

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 1: Switching Characteristics (Resistive load R_L=2.6Ω)

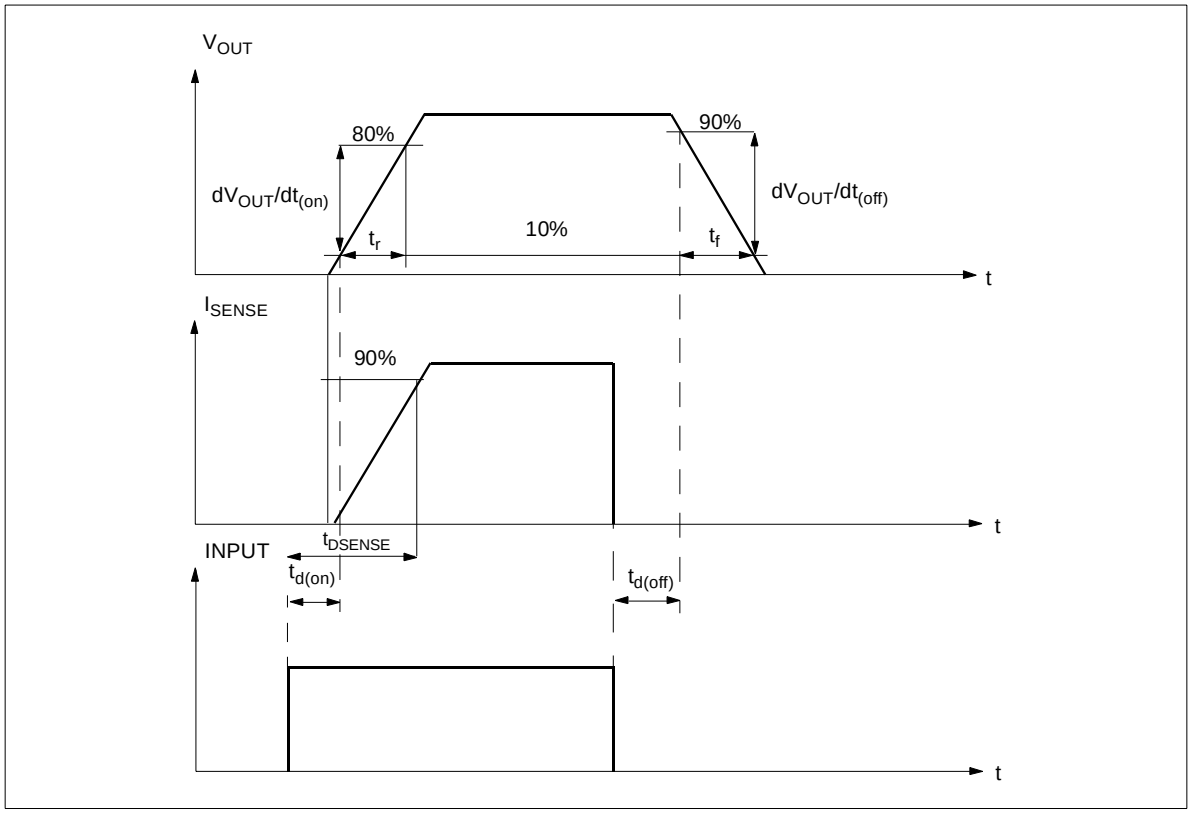
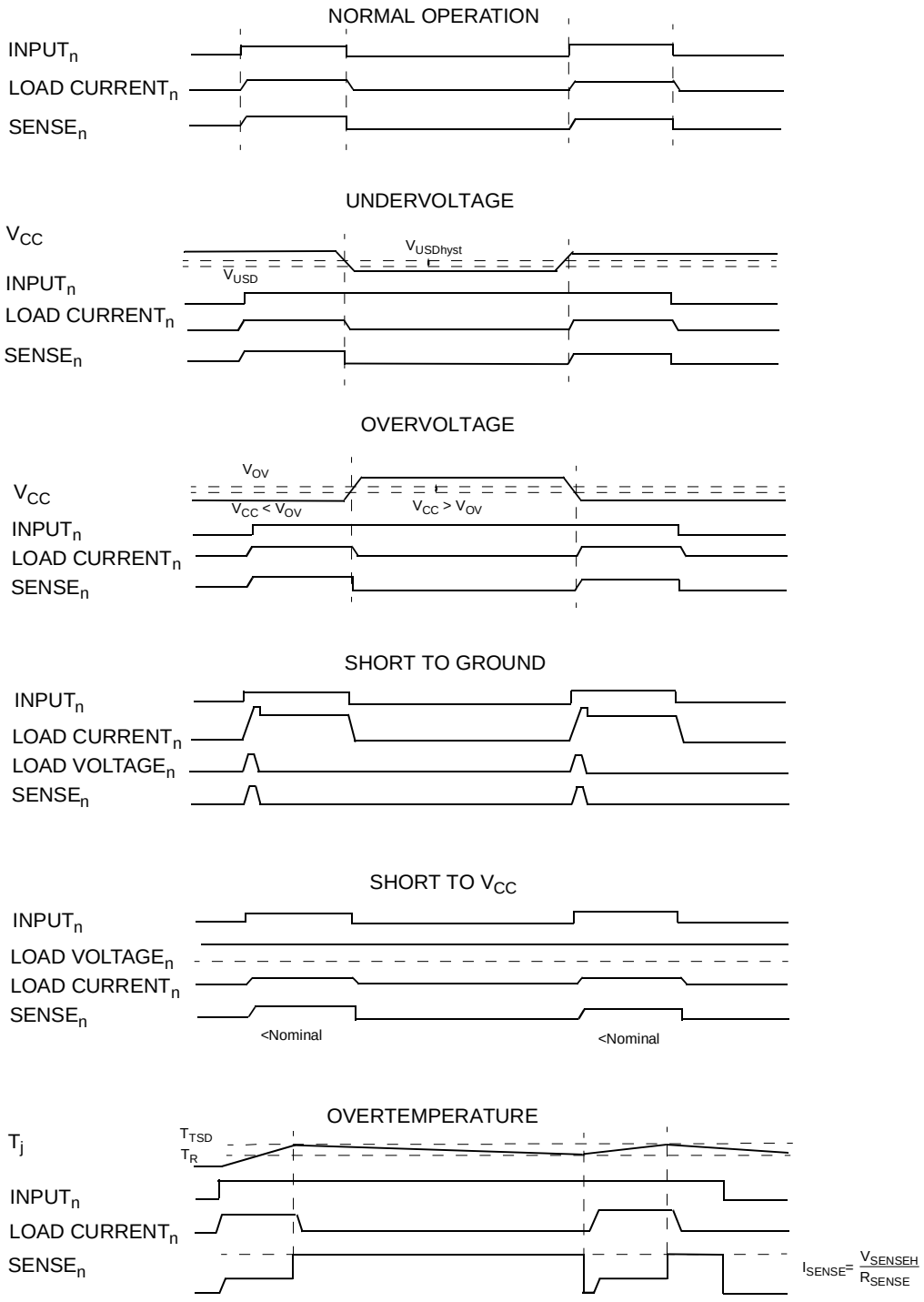
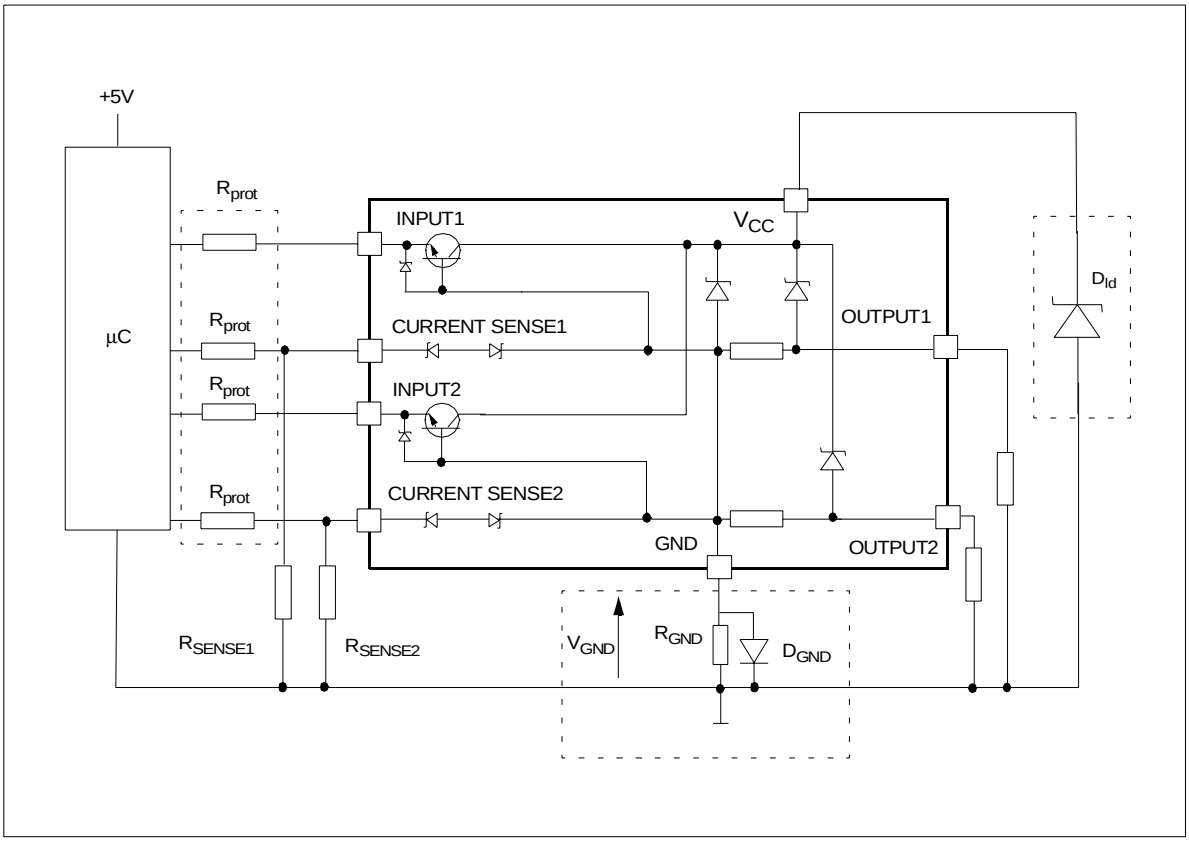


Figure 2: Waveforms



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / I_{S(on)max}$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input thresholds and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$$

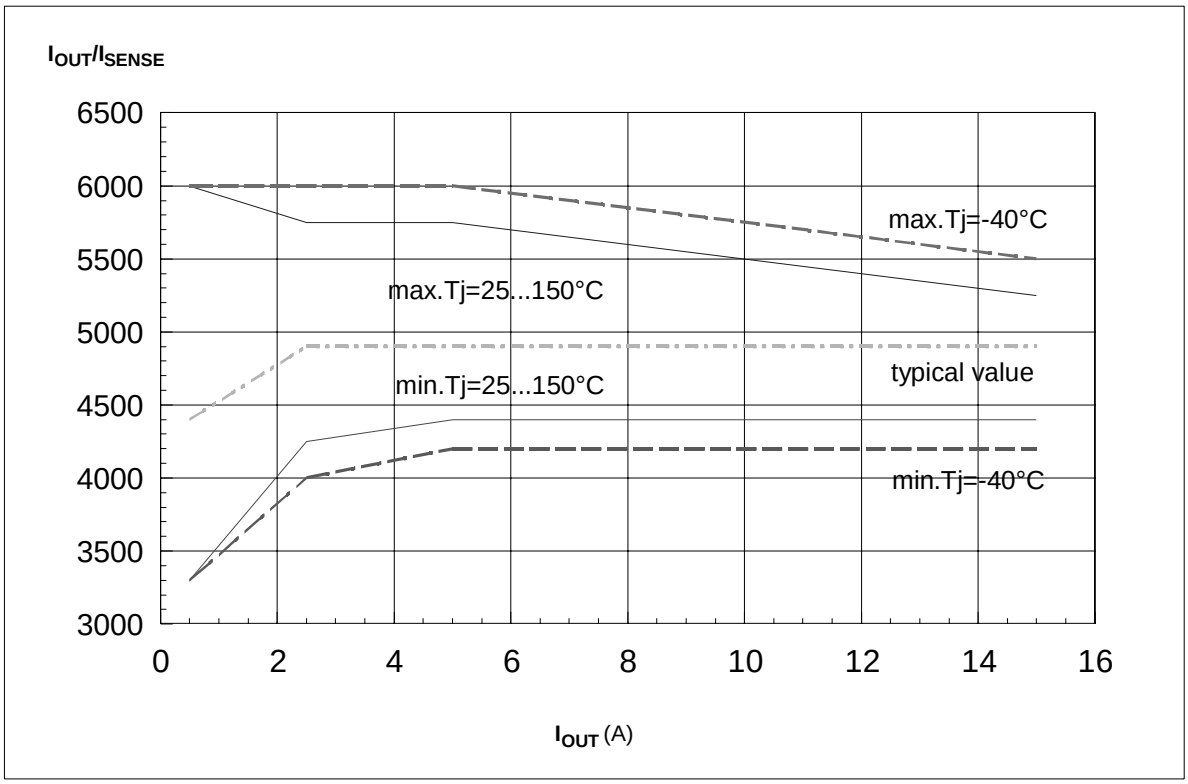
Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended R_{prot} value is 10kΩ.

Figure 3: I_{OUT}/I_{SENSE} versus I_{OUT}



PowerSSO-24™ MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	1.9		2.22
A2	1.9		2.15
a1	0		0.07
b	0.34	0.4	0.46
c	0.23		0.32
D	10.2		10.4
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10º
X	3.9		4.3
Y	6.1		6.5