Revision History

No.	History	Date	Remark
0.1	1) Defined target spec. 2) Corrected Pin assignment table	July 2004	

DESCRIPTION

Hynix HYMP112S64MP8 series is unbuffered 200-pin double data rate 2 Synchronous DRAM Small Outline Dual In-Line Memory Modules (DIMMs) which are organized as 128Mx64 high-speed memory arrays. Hynix HYMP112S64MP8 series consists of eight 128Mx8 DDR2 SDRAMs in 63 ball FBGA Dual Die Pacakge(DDP)s. Hynix HYMP112S64MP8 series provide a high performance 8-byte interface in 67.60mm X 30.00mm form factor of industry standard. It is suitable for easy interchange and addition.

Hynix HYMP512S64MP8 series is designed for high speed and offers fully synchronous operations referenced to both rising and falling edges of differential clock inputs. While all addresses and control inputs are latched on the rising edges of the clock, Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 4-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_1.8. High speed frequencies, programmable latencies and burst lengths allow variety of device operation in high performance memory system.

Hynix HYMP512S64MP8 series incorporates SPD(serial presence detect). Serial presence detect function is implemented via a serial 2,048-bit EEPROM. The first 128 bytes of serial PD data are programmed by Hynix to identify DIMM type, capacity and other the information of DIMM and the last 128 bytes are available to the customer.

FEATURES

- 1GB (128M x 64) Unbuffered DDR2 SO - DIMM based on 128Mx8 DDR2 DDP SDRAMs
- JEDEC standard Double Data Rate2 Synchronous DRAMs (DDR2 SDRAMs) with 1.8V +/- 0.1V Power Supply
- All inputs and outputs are compatible with SSTL_1.8 interface
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- Fully differential clock operations (CK & /CK)
- Programmable CAS Latency 3 / 4 /5 supported
- Programmable Burst Length 4 / 8 with both sequential and interleave mode
- Auto refresh and self refresh supported
- 7.8us refresh period at Lower than T_{CASE} 85℃, 3.9us(85℃ < T_{CASE} ≤ 95℃)
- Serial Presence Detect(SPD) with EEPROM
- Lead free product

ORDERING INFORMATION

Type	Part No.	Description	CL-tRCD-tRP	Form Factor
PC2-3200 (DDR2-400)	HYMP112S64(L)MP8-E4	2 rank 1GB Lead-free SO-DIMM	4-4-4	200pin Unbuffered SO-DIMM 67.60 mm x 30,00 mm (MO-224)
	HYMP112S64(L)MP8-E3		3-3-3	
PC2-4300 (DDR2-533)	HYMP112S64(L)MP8-C5		5-5-5	
	HYMP112S64(L)MP8-C4		4-4-4	

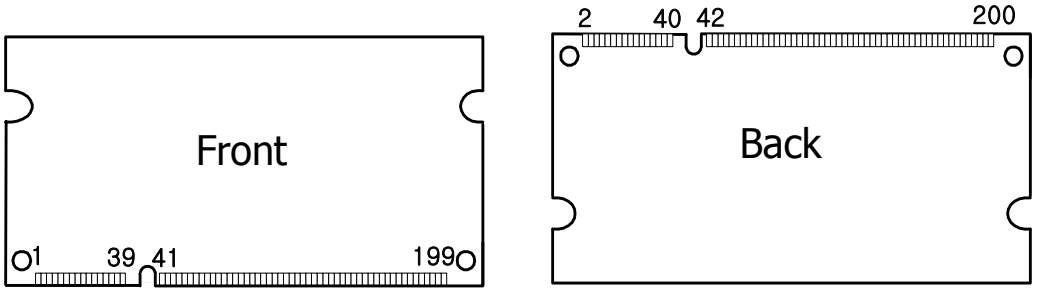
PIN Functional Description

Symbol	Type	Polarity	Pin Description
CK[1:0], $\overline{CK}$[1:0]	Input	Cross Point	The system clock inputs. All adress an commands lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop(DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
/S[1:0]	Input	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S}$0; Rank 1 is selected by $\overline{S}$1
/RAS, /CAS, /WE	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, $\overline{CAS}$, $\overline{RAS}$ and $\overline{WE}$ define the operation to be excecuted by the SDRAM.
BA[1:0]	Input		Selects which DDR2 SDRAM internal bank of four or eight is activated.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM mode register.
A[9:0], A10/ AP, A[15:11]	Input		During a Bank Activate command cycle, difines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high., autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle., AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ[63:0]	In/Out		Data Input/Output pins.
DM[7:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS[7:0], $\overline{DQS}$[7:0]	In/Out	Cross point	The data strobe, associated with one data byte, sourced whit data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed approriately.
RESET	Input	Active Low	When hign, the PLL outputs are always driven when the PLL input clock is active. When low, the PLL remains locked on the input clock, if active, but output clocks are stopped. Pulled high via 10KßŸ resistor on the SO-DIMM . Only used on DDR2 SO-DIMMs with a PLL.
V_{DD}, V_{DD}SPD,V_{SS}	Supply		Power supplies for core, I/O, Serial Presense Detect, and ground for the module.
SDA	In/Out		This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resister must be connected to V_{DD} to act as a pull up.
SCL	Input		This signals is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to VDD to act as a pull up.
SA[1:0]	Input		Address pins used to select the Serial Presence Detect base address.
TEST	In/Out		The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules(SODIMMs).

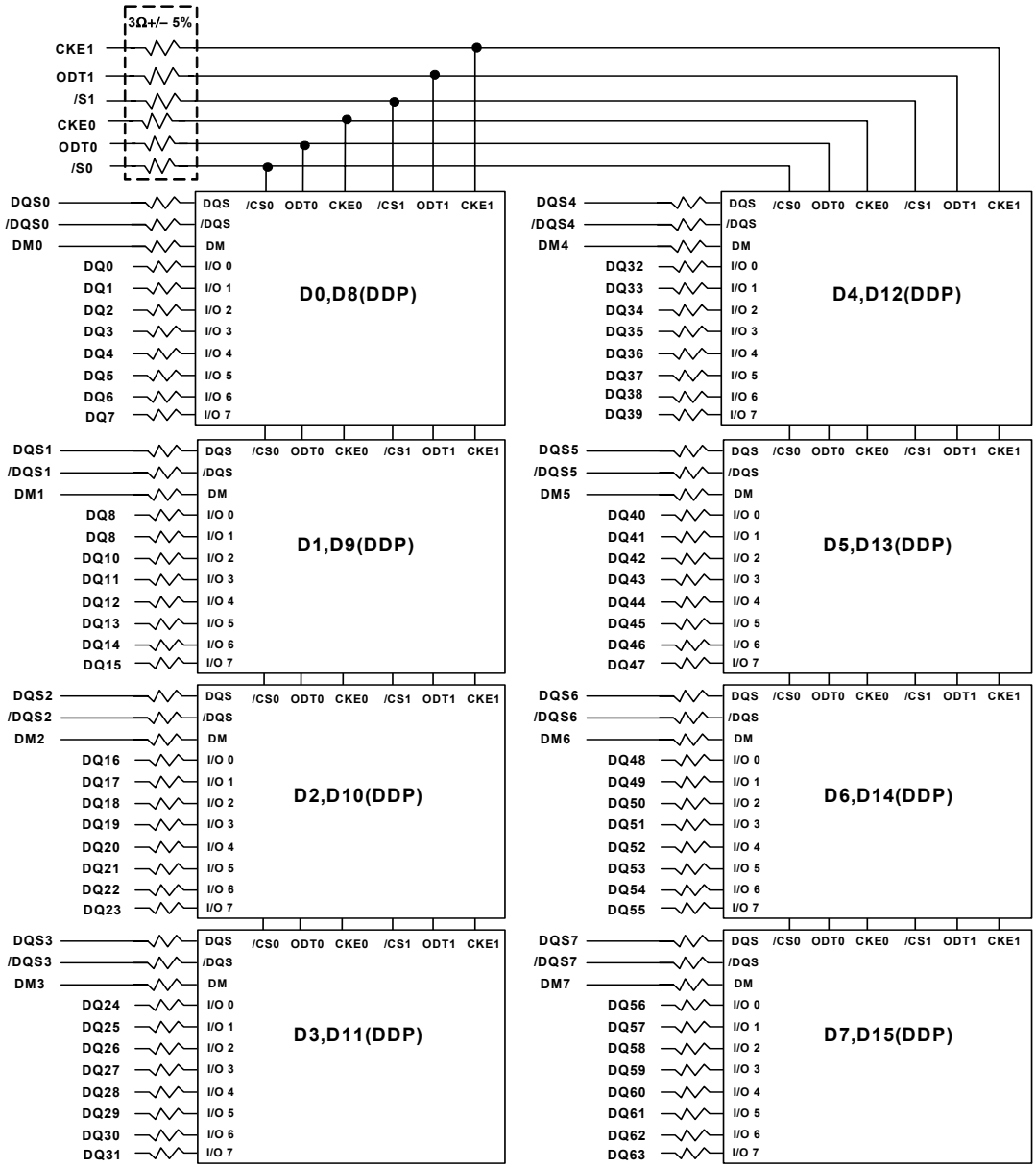
PIN ASSIGNMENT

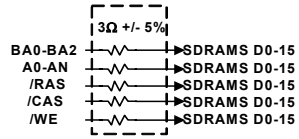
Pin NO.	Front Side	Pin NO.	Back Side	Pin NO.	Front Side	Pin NO.	Back Side	Pin NO.	Front Side	Pin NO.	Back Side	Pin NO.	Front Side	Pin NO.	Back Side
1	VREF	2	VSS	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	VSS	4	DQ4	53	VSS	54	VSS	103	VDD	104	VDD	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	VSS	156	VSS
7	DQ1	8	VSS	57	DQ19	58	DQ23	107	BA0	108	$\overline{RAS}$	157	DQ48	158	DQ52
9	VSS	10	DM0	59	VSS	60	VSS	109	$\overline{WE}$	110	$\overline{S}$0	159	DQ49	160	DQ53
11	$\overline{DQS}$0	12	VSS	61	DQ24	62	DQ28	111	VDD	112	VDD	161	VSS	162	VSS
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	$\overline{CAS}$	114	ODT0	163	NC,TEST	164	CK1
15	VSS	16	DQ7	65	VSS	66	VSS	115	NC/$\overline{S}$1	116	A13	165	VSS	166	$\overline{CK}$1
17	DQ2	18	VSS	67	DM3	68	$\overline{DQS}$3	117	VDD	118	VDD	167	$\overline{DQS}$6	168	VSS
19	DQ3	20	DQ12	69	NC	70	DQS3	119	NC/ODT1	120	NC	169	DQS6	170	DM6
21	VSS	22	DQ13	71	VSS	72	VSS	121	VSS	122	VSS	171	VSS	172	VSS
23	DQ8	24	VSS	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	VSS	28	VSS	77	VSS	78	VSS	127	VSS	128	VSS	177	VSS	178	VSS
29	$\overline{DQS}$1	30	CK0	79	CKE0	80	NC/CKE1	129	$\overline{DQS}$4	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK}$0	81	VDD	82	VDD	131	DQS4	132	VSS	181	DQ57	182	DQ61
33	VSS	34	VSS	83	NC	84	NC/A15	133	VSS	134	DQ38	183	VSS	184	VSS
35	DQ10	36	DQ14	85	BA2	86	NC/A14	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS}$7
37	DQ11	38	DQ15	87	VDD	88	VDD	137	DQ35	138	VSS	187	VSS	188	DQS7
39	VSS	40	VSS	89	A12	90	A11	139	VSS	140	DQ44	189	DQ58	190	VSS
41	VSS	42	VSS	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	VSS	193	VSS	194	DQ63
45	DQ17	46	DQ21	95	VDD	96	VDD	145	VSS	146	$\overline{DQS}$5	195	SDA	196	VSS
47	VSS	48	VSS	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS}$2	50	NC	99	A3	100	A2	149	VSS	150	VSS	199	VDDSPD	200	SA1

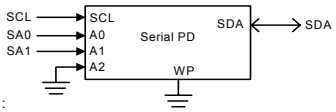
Pin Location



FUNCTIONAL BLOCK DIAGRAM

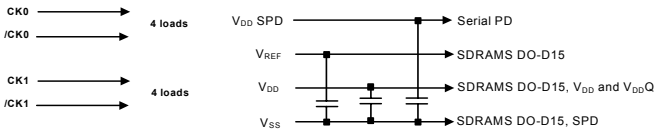






Notes :

1. Unless otherwise noted, resistor values are 22 Ω ± 5%
2. DQ wring may differ form that described in this drawing; however , DQ,DM,DQS,/DQS relationships are maintained as shown.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Operating temperature(ambient)	T_{OPR}	0 ~ +55	°C	1
DRAM Component Case Temperature Range	TCASE	0 ~+95	°C	2
Operating Humidity(relative)	H_{OPR}	10 to 90	%	1
Storage Temperature	TSTG	-50 ~ +100	°C	1
Storage Humidity(without condensation)	H_{STG}	5 to 95	°C	1
Barometric Pressure(operating & storage)	P_{BAR}	105 to 69	K Pascal	1,3

Note :

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Expousure to absolute maximum rating conditions for extended periods may affect reliablility.
2. If the DRAM case temperature is Above 85°C, the Auto-Refresh command interval has to be reduced to tREFI=3.9μs. For Measurement conditions of T_{CASE}, please refer to the JEDEC document JESD51-2.
3. Up to 9850 ft.

Operating Condtions(AC&DC)

DC OPERATING CONDITIONS (SSTL_1.8)

Parameter	Symbol	Min	Max	Unit	Note
Power Supply Voltage	VDD	1.7	1.9	V	
	VDDQ	1.7	1.9	V	1
Input Reference Voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	2
EEPROM Supply Voltage	VDDSPD	1.7	3.6	V	
Termination Voltage	VTT	VREF-0.04	VREF+0.04	V	3

Note :

1. V_{DDQ} must be less than or equal to V_{DD}.
2. Peak to peak ac noise on V_{REF} may not exeed +/-2% V_{REF}(dc)
3. VTT of transmitting device must track VREF of receiving device.

Input DC Logic Level

Parameter	Symbol	Min	Max	Unit	Note
Input High Voltage	VIH(DC)	VREF + 0.125	VDDQ + 0.3	V	
Input Low Voltage	VIL(DC)	-0.30	VREF - 0.125	V	

Input AC Logic Level

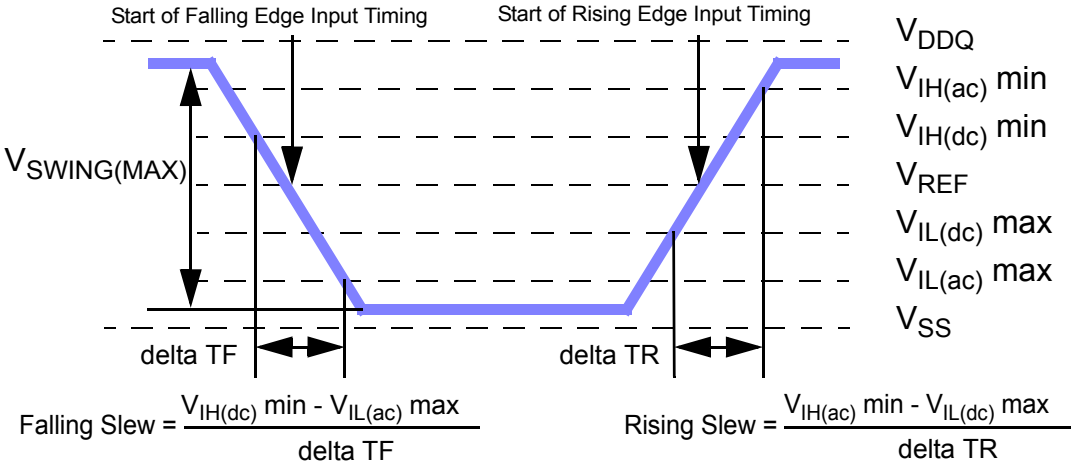
Parameter	Symbol	Min	Max	Unit	Note
AC Input logic High	VIH(AC)	VREF + 0.250	-	V	
AC Input logic Low	VIL(AC)	-	VREF - 0.250	V	

AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Notes:

1. Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)}$ max to $V_{IH(ac)}$ min for rising edges and the range from $V_{IH(dc)}$ min to $V_{IL(ac)}$ max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



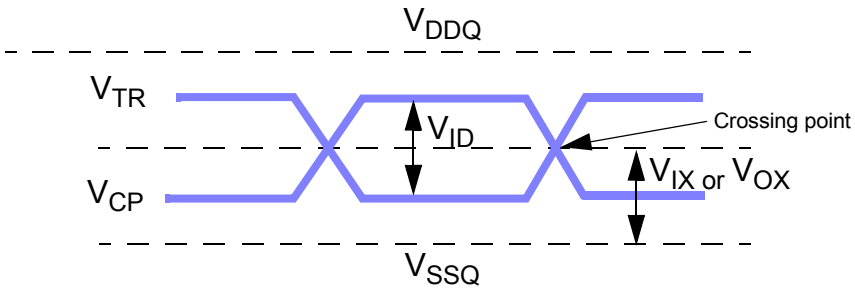
< Figure : AC Input Test Signal Waveform >

Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID} (ac)	ac differential input voltage	0.5	VDDQ + 0.6	V	1
V_{IX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2

Note:

1. VIN(DC) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
2. VID(DC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input (such as CK, DQS, LDQS or UDQS) level and VCP is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to VIH(DC) - V IL(DC).



< Differential signal levels >

Notes:

1. VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to VIH(AC) - V IL(AC).
2. The typical value of VIX(AC) is expected to be about 0.5 * VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ . VIX(AC) indicates the voltage at whitch differential input signals must cross.

Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	1

Notes:

1. The typical value of VOX(AC) is expected to be about 0.5 * V DDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ . VOX(AC) indicates the voltage at whitch differential output signals must cross.

Output Buffer Levels

Output AC Test Conditions

Symbol	Parameter	SSTL_18 Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.603	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} - 0.603	V	
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

1. The VDDQ of the device under test is referenced.

Output DC Current Drive

Symbol	Parameter	SSTI_18 Class II	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

1. V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.
2. V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.
3. The dc value of V_{REF} applied to the receiving device is set to V_{TT}
4. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3) along a 21 ohm load line to define a convenient driver current for measurement.

OCD defalut characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		12.6	18	23.4	ohms	1,2
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate	Sout	1.5	-	5	V/ns	1,4,5,6

Note:

1. Absolute Specifications (0°C ≤ T_{CASE} ≤ +95°C; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V)
2. Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from vil(ac) to vih(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC.
6. DRAM output slew rate specification applies to 400MT/s & 533MT/s speed bins. Output slew rate at 667&800MT/s will be added with JEDEC process.

PIN Capacitance (VDD=1.8V,VDDQ=1.8V, TA=25℃. f=1MHz)

Parameter	Pin	Symbol	Min,	Max,	Unit
Input Capacitance	CK0, /CK0	CCK	15	33	pF
Input Capacitance	CKE0, /CS	CI1	44	65	pF
Input Capacitance	Address, /RAS, /CAS, /WE	CI2	27	65	pF
Input Capacitance	DQ,DM,DQS, /DQS	CIO	8	12	pF

Note :

1. Pins not under test are tied to GND.
2. These value are guaranteed by design and tested on a sample basis only.

IDD Specifications

HYMP112S64(L)MP8		PC2 3200	PC2 4300	Unit	Note
Parameter	**Symbol**	**max.**	**max.**		
Operating one bank active-precharge current	IDD0	920	1040	mA	
Operating one bank active-read-precharge current	IDD1	1000	1120	mA	
Precharge power-down current	IDD2P	48	64	mA	
Precharge quiet standby current	IDD2Q	520	600	mA	
Precharge standby current	IDD2N	560	640	mA	
Active power-down current	IDD3P(F)	240	320	mA	
	IDD3P(S)	48	64	mA	
Active Standby Current	IDD3N	720	840	mA	
Operating burst read current	IDD4R	1320	1440	mA	
Operating Current	IDD4W	1320	1440	mA	
Burst auto refresh current	IDD5B	1560	1600	mA	
Self Refresh Current	IDD6	80	80	mA	
	IDD6(L)	48	48	mA	
Operating bank interleave read current	IDD7	1960	2160	mA	

IDD Meauarement Conditions

Symbol	Conditions		Units
IDD0	**Operating one bank active-precharge current**; ^{t}CK = $^{t}CK(IDD)$, ^{t}RC = $^{t}RC(IDD)$, ^{t}RAS = ^{t}RAS-min(IDD);CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING;Data bus inputs are SWITCHING		mA
IDD1	**Operating one bank active-read-precharge curren** ; IOUT = 0mA;BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = $^{t}CK(IDD)$, ^{t}RC = ^{t}RC (IDD), ^{t}RAS = $^{t}RASmin(IDD)$, ^{t}RCD = $^{t}RCD(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands ; Address bus inputs are SWITCHING ; Data pattern is same as IDD4W		mA
IDD2P	**Precharge power-down current** ; All banks idle ; ^{t}CK = $^{t}CK(IDD)$; CKE is LOW ; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2Q	**Precharge quiet standby current**;All banks idle; ^{t}CK = $^{t}CK(IDD)$;CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2N	**Precharge standby current**; All banks idle; ^{t}CK = $^{t}CK(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD3P	**Active power-down current**; All banks open; ^{t}CK = $^{t}CK(IDD)$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	mA
		Slow PDN Exit MRS(12) = 1	mA
IDD3N	**Active standby current**; All banks open; ^{t}CK = $^{t}CK(IDD)$, ^{t}RAS = $^{t}RASmax(IDD)$, ^{t}RP =$^{t}RP(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = $^{t}CK(IDD)$, ^{t}RAS = $^{t}RASmax(IDD)$, ^{t}RP = $^{t}RP(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = $^{t}CK(IDD)$, ^{t}RAS = $^{t}RASmax(IDD)$, ^{t}RP = $^{t}RP(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING;; Data pattern is same as IDD4W		mA
IDD5B	**Burst refresh current**; ^{t}CK = $^{t}CK(IDD)$; Refresh command at every $^{t}RFC(IDD)$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0V; CKE £ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		mA
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $^{t}RCD(IDD)$-1*$^{t}CK(IDD)$; ^{t}CK = $^{t}CK(IDD)$, ^{t}RC = $^{t}RC(IDD)$, ^{t}RRD = $^{t}RRD(IDD)$, ^{t}RCD = 1*$^{t}CK(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions		mA

Note:

1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD

   LOW is defined as Vin ≤ VILAC(max)

   HIGH is defined as Vin ≥ VIHAC(min)

   STABLE is defined as inputs stable at a HIGH or LOW level

   FLOATING is defined as inputs at VREF = VDDQ/2

   SWITCHING is defined as:

   inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and

   inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

Electrical Characteristics & AC Timings

Speed Bins and CL,tRCD,tRP,tRC and tRAS for Corresponding Bin

Speed	DDR2-533(C4)	DDR2-533(C5)	DDR2-400(C3)	DDR2-400(C4)	Unit
Bin(CL-tRCD-tRP)	4-4-4	5-5-5	3-3-3	4-4-4	
Parameter	min	min	min	min	
CAS Latency	4	5	3	4	ns
tRCD	15	18.75	15	20	ns
tRP	15	18.75	15	20	ns
tRC	60	63.75	55	65	ns
tRAS	45	45	40	45	ns

AC Timing Parameters by Speed Grade

Parameter	Symbol	DDR2-400		DDR2-533		Unit	Note
		Min	Max	Min	Max		
Data-Out edge to Clock edge Skew	tAC	-600	600	-500	500	ps	
DQS-Out edge to Clock edge Skew	tDQSCK	-500	500	-500	450	ns	
Clock High Level Width	tCH	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width	tCL	0.45	0.55	0.45	0.55	CK	
Clock Half Period	tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	ns	
System Clock Cycle Time	tCK	5000	8000	3750	8000	ps	
DQ and DM input hold time	tDH	400	-	350	-	ps	1
DQ and DM input setup time	tDS	400	-	350	-	ps	1
Control & Address input Pulse Width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input pulse witdth for each input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
Data-out high-impedance window from CK, /CK	tHZ	-	tAC max	-	tAC max	ps	
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	350	-	300	ps	
DQ hold skew factor	tQHS	-	450	-	400	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	

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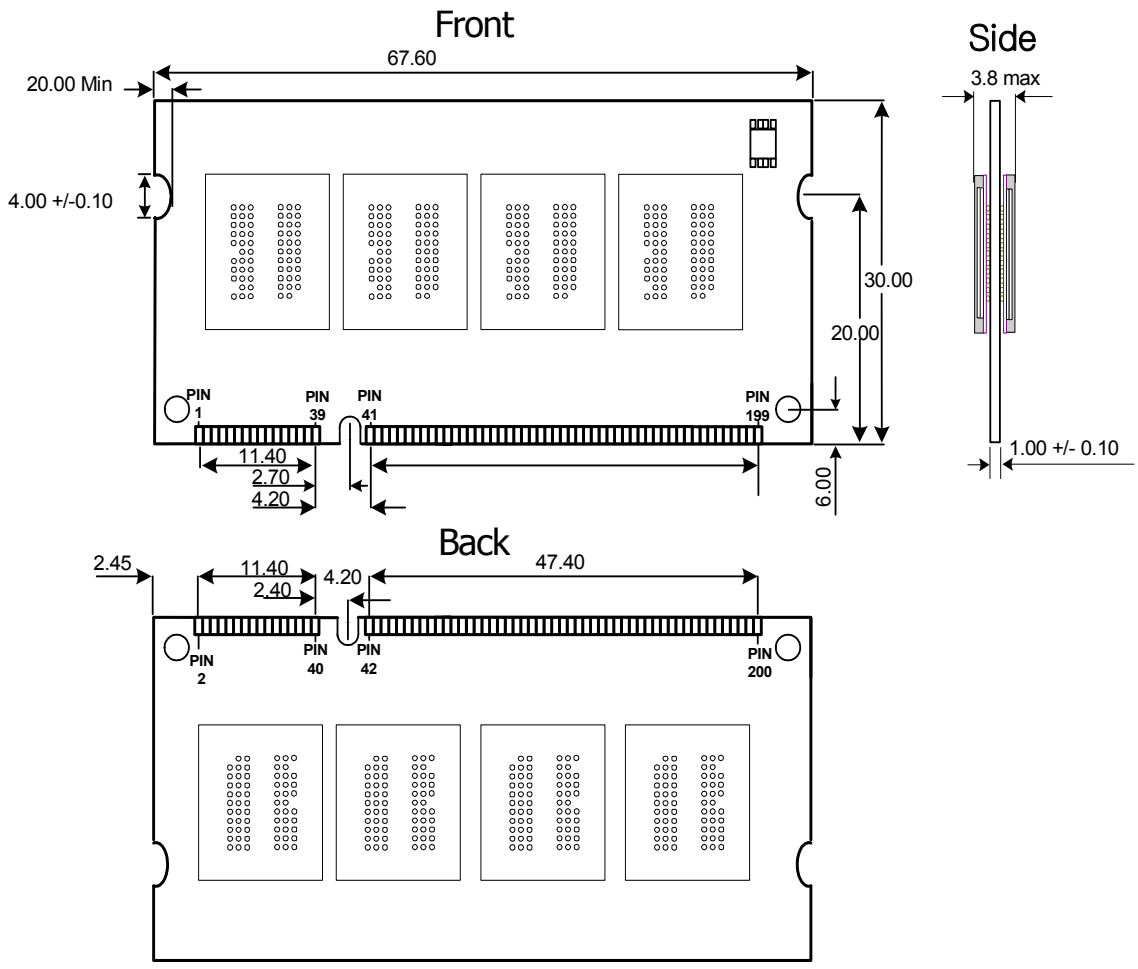
Parameter	Symbol	DDR2 400		DDR2 533		Unit	Note
		Min	Max	Min	Max		
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	
Write preamble	tWPRE	0.25	-	0.25	-	tCK	
Address and control input hold time	tIH	600	-	500	-	ps	
Address and control input setup time	tIS	600	-	500	-	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Auto-Refresh to Active/Auto-Refresh command period	tRFC	105	-	105	-	ns	
Row Active to Row Active Delay	tRRD	7.5	-	7.5	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	-	15	-	ns	
Auto Precharge Write Recovery + Precharge Time	tDAL	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	tCK	
Write to Read Command Delay	tWTR	10	-	7.5	-	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2		2		tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	^{t}CKE	3		3		tCK	
ODT turn-on delay	^{t}AOND	2	2	2	2	tCK	
ODT turn-on	^{t}AON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	
ODT turn-on(Power-Down mode)	^{t}AONPD	tAC(min)+2	2tCK+ tAC(max)+1	tAC(min)+2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	^{t}AOF	tAC(min)	tAC(max)+ 0.6	tAC(min)	tAC(max)+ 0.6	ns	
ODT turn-off (Power-Down mode)	^{t}AOFPD	tAC(min)+2	2.5tCK+ tAC(max)+1	tAC(min)+2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	
Average periodic Refresh Interval	tREFI	-	7.8	-	7.8	us	2
	tREFI	-	3.9	-	3.9	us	3

Note :

1. For details and notes, please refer to the relevant HYNIX component datasheet(HY5PS1G821(L)M).
2. 0°C ≤ TCASE ≤ 85°C
3. 85°C < TCASE ≤ 95°C

PACKAGE OUTLINE



note:
1. all dimension Units are millimeters.
2. all outline dimensions and tolerances match up to the JEDEC standard.

SPD SPECIFICATION

(128Mx64 Unbuffered Lead-free DDR2 SO-DIMM)

SERIAL PRESENCE DETECT

Bin Sort : E3(DDR2 400 3-3-3), E4(DDR2 400 4-4-4), C4(DDR2 533 4-4-4), C5(DDR2 533 5-5-5)

Byte#	Function Description	Speed Grade	Function Supported	Hexa Value	Note
0	Number of bytes utilized by module manufacturer	all	128 Bytes	80	
1	Total number of Bytes in SPD device	all	256 Bytes	08	
2	Fundamental memory type	all	DDR2 SDRAM	08	
3	Number of row address on this assembly	all	14	0E	1
4	Number of column address on this assembly	all	10	0A	1
5	Number of DIMM ranks	all	30.0mm/stack/2rank	71	
6	Module data width	all	64 Bits	40	
7	Module data width (continued)	all	-	00	
8	Voltage Interface level of this assembly	all	SSTL 1.8V	05	
9	DDR SDRAM cycle time at CL=5	E3,E4	5.0 ns	50	2
		C4,C5	3.75 ns	3D	2
10	DDR SDRAM access time from clock (tAC)	E3,E4	+/-0.6ns	60	
		C4,C5	+/-0.5ns	50	
11	DIMM Configuration type	all	non-ECC	00	
12	Refresh Rate and Type	all	7.8us & Self refresh	82	
13	Primary DDR SDRAM width	all	x8	08	
14	Error Checking DDR SDRAM data width	all	None	00	
15	Reserved		-	00	
16	Burst Lengths Supported	all	4,8	0C	
17	Number of banks on each SDRAM Device	all	4	04	
18	CAS latency supported	all	3, 4, 5	38	
19	Reserved		-	00	
20	DIMM Type	all	SO-DIMM	04	
21	DDR SDRAM module attributes	all	Normal	00	
22	DDR SDRAM device attributes : General	all	-	00	
23	DDR SDRAM cycle time at CL=4(tCK)	E3,E4,C5	5.0ns	50	2
		C4	3.75ns	3D	
24	DDR SDRAM access time from clock at CL=4(tAC)	E3,E4,C5	+/-0.6ns	60	2
		C4	+/-0.5ns	50	
25	DDR SDRAM cycle time at CL=3(tCK)	E3,C4	5.0ns	50	2
		E4,C5	Undefined	00	
26	DDR SDRAM access time from clock at CL=3(tAC)	E3,C4	+/-0.6ns	60	2
		E4,C5	Undefined	00	
27	Minimum Row Precharge Time(tRP)	E3, C4	15ns	3C	
		E4	20ns	50	
		C5	18.75ns	4B	
28	Minimum Row Activate to Row Active delay(tRRD)	all	7.5ns	1E	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay(tRCD)	E3, C4	15ns	3C	
		E4	20ns	50	
		C5	18.75ns	4B	
30	Minimum active to precharge time(tRAS)	E3	40ns	28	
		E4,C4,C5	45ns	2D	
31	Module rank density	all	512MB	80	
32	Address and command input setup time before clock (tIS)	E3, E4	0.6ns	60	
		C4, C5	0.5ns	50	
33	Address and command input hold time after clock (tIH)	E3, E4	0.6ns	60	
		C4, C5	0.5ns	50	
34	Data input setup time before clock (tDS)	E3, E4	0.40ns	40	
		C4, C5	0.35ns	35	
35	Data input hold time after clock (tDH)	E3, E4	0.40ns	40	
		C4, C5	0.35ns	35	
36	Write recovery time(tWR)	all	15ns	3C	
37	Internal write to read command delay(tWTR)	E3, E4	10ns	28	
		C4, C5	7.5ns	1E	
38	Internal read to precharge command delay(tRTP)	all	7.5ns	1E	
39	Memory analysis probe characteristics		Undefined	00	
40	Extension of byte 41 tRC and byte 42 tRFC	E3,E4,C4	Undefined	00	
		C5	tRC extended	50	
41	Minimum active / auto-refresh time (tRC)	E3	55ns	37	
		C4	60ns	3C	
		E4	65ns	41	
		C5	63.75ns	3F	

- continued -

Byte#	Function Description	Speed Grade	Function Supported	Hexa Value	Note
42	Minimum auto-refresh to active/auto-refresh command period(tRFC)	all	105ns	69	
43	Maximum cycle time (tCK max)	all	8.0ns	80	
44	Maximim DQS-DQ skew time(tDQSQ)	E3, E4	0.35ns	23	
		C4, C5	0.30ns	1E	
45	Maximum read data hold skew factor(tQHS)	E3, E4	0.45ns	2D	
		C4, C5	0.40ns	28	
46	PLL Relock time		No PLL	00	
47~61	Superset information(may be used in future)		Undefined	00	
62	SPD Revision code		1.0	10	
63	Checksum for Bytes 0~62	E3	-	C5	
		E4	-	4C	
		C4	-	3F	
		C5	-	23	
64	Manufacturer JEDEC ID Code		Hynix JEDEC ID	AD	
65~71	--------- Manufacturer JEDEC ID Code		-	00	
72	Manufacturing location		Hynix(Korea Area) HSA(United States Area) HSE(Europe Area) HSJ(Japan Area) Singapore Asia Area	0* 1* 2* 3* 4* 5*	6
73	Manufacture part number(Hynix Memory Module)		H	48	
74	-------- Manufacture part number(Hynix Memory Module)		Y	59	
75	-------- Manufacture part number(Hynix Memory Module)		M	4D	
76	Manufacture part number (DDR2 SDRAM)		P	50	
77	---------Manufacture part number(Memory density)		1	31	
78	Manufacture part number(Module Depth)		1	31	
79	------- Manufacture part number(Module Depth)		2	32	
80	Manufacture part number(Module type)		S	53	
81	Manufacture part number(Data width)		6	36	
82	-------Manufacture part number(Data width)		4	34	
83	Manufacture part number(Package type)		M	4D	
84	Manufacture part number(Package material)		P	50	
85	Manufacture part number(Component configuration)		8	38	
86	Manufacture part number(Hyphen)		'-'	2D	
87	Manufacture part number(Minimum cycle time)	E3, E4	E	45	
		C4, C5	C	43	
88	-------Manufacture part number(Minimum cycle time)	E3	3	33	
		E4,C4	4	34	
		C5	5	35	
89~90	Manufacture part number(T.B.D)		Blank	20	
91	Manufacture revision code(for Component)				
92	Manufacture revision code (for PCB)				
93	Manufacturing date(Year)				3
94	Manufacturing date(Week)				3
95~98	Module serial number				4
99~127	Manufacturer specific data (may be used in future)		Undefined	00	5
128~255	Open for customer use		Undefined	00	5

Note :

1. The bank address is excluded
2. This value is based on the component specification
3. These bytes are programmed by code of date week & date year
4. These bytes apply to Hynix's own Module Serial Number System
5. These bytes undefined and coded as '00h'
6. Refer to Hynix Web Site

Byte 83~84, Low Power Part

Byte #	Function Description	Speed Grade	Function Supported	Hexa Value	Note
83	Manufacture part number(Low power part)		L	4C	
84	Manufacture part number(Package type)		M	4D	