



A82DL32x4T(U) Series

***Stacked Multi-Chip Package (MCP) Flash Memory and SRAM,
A82DL32x4T(U) 32 Megabit (4Mx8 Bit/2Mx16 Bit) CMOS 3.3 Volt-only,
Simultaneous Operation Flash Memory and 4M (256Kx16 Bit) Static RAM***

Preliminary

Document Title

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Revision History

| <u>Rev. No.</u> | <u>History</u> | <u>Issue Date</u> | <u>Remark</u> |
|------------------------|-----------------------|--------------------------|----------------------|
| 0.0 | Initial issue | August 21, 2005 | Preliminary |



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DISTINCTIVE CHARACTERISTICS

MCP Features

- Single power supply operation 2.7 to 3.6 volt
- High Performance
 - Access time as fast as 70ns
- Package 69-Ball TFBGA (8x11x1.4 mm)
- Industrial operating temperature range: -40°C to 85°C for -U; -25°C to 85°C for -I

Flash Features

ARCHITECTURAL ADVANTAGES

- Simultaneous Read/Write operations
 - Data can be continuously read from one bank while executing erase/program functions in other bank
 - Zero latency between read and write operations
- Multiple bank architectures
 - Three devices available with different bank sizes (refer to Table 2)
- Package
 - 69-Ball TFBGA (8x11x1.4 mm)
- Top or bottom boot block
- Manufactured on 0.18 μ m process technology
 - Compatible with AM42DL32x4G devices
- Compatible with JEDEC standards
 - Pinout and software compatible with single-power-supply flash standard

PERFORMANCE CHARACTERISTICS

- High performance
 - Access time as fast as 70ns
 - Program time: 7 μ s/word typical utilizing Accelerate function
- Ultra low power consumption (typical values)
 - 2mA active read current at 1MHz
 - 10mA active read current at 5MHz
 - 200nA in standby or automatic sleep mode
- Minimum 1 million write cycles guaranteed per sector
- 20 Year data retention at 125°C
 - Reliable operation for the life of the system

SOFTWARE FEATURES

- Supports Common Flash Memory Interface (CFI)
- Erase Suspend/Erase Resume

- Suspends erase operations to allow programming in same bank
- Data Polling and Toggle Bit
 - Provides a software method of detecting the status of program or erase cycles
- Unlock Bypass Program command
 - Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- Any combination of sectors can be erased
- Ready/Busy output (RY/BY)
 - Hardware method for detecting program or erase cycle completion
- Hardware reset pin ($\overline{\text{RESET}}$)
 - Hardware method of resetting the internal state machine to reading array data
- $\overline{\text{WP}}$ /ACC input pin
 - Write protect ($\overline{\text{WP}}$) function allows protection of two outermost boot sectors, regardless of sector protect status
 - Acceleration (ACC) function accelerates program timing
- Sector protection
 - Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
 - Temporary Sector Unprotect allows changing data in protected sectors in-system

LP SRAM Features

- Power supply range: 2.7V to 3.6V
- Access times: 70 ns (max.)
- Current:
 - Very low power version: Operating: 35mA(max.)
Standby: 10uA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Output enable and two chips enable inputs for easy application
- Data retention voltage: 2.0V (min.)

GENERAL DESCRIPTION

The A82DL32x4T(U) family consists of 32 megabit, 3.0 volt-only flash memory devices, organized as 2,097,152 words of 16 bits each or 4,194,304 bytes of 8 bits each. Word mode data appears on I/O₀–I/O₁₅; byte mode data appears on I/O₀–I/O₇. The device is designed to be programmed in-system with the standard 3.0 volt VCC supply, and can also be programmed in standard EPROM programmers.

The device is available with an access time of 70ns. The devices are offered in 69-ball Fine-pitch BGA. Standard control pins—chip enable ($\overline{CE_F}$), write enable (\overline{WE}), and output enable (\overline{OE})—control normal read and write operations, and avoid bus contention issues.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into two banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The A82DL32x4T(U) devices uses multiple bank architectures to provide flexibility for different applications. Three devices are available with these bank sizes:

| Device | Bank 1 | Bank 2 |
|--------|--------|--------|
| DL3224 | 4 Mb | 28 Mb |
| DL3234 | 8 Mb | 24 Mb |
| DL3244 | 16 Mb | 16 Mb |

A82DL32x4T(U) Features

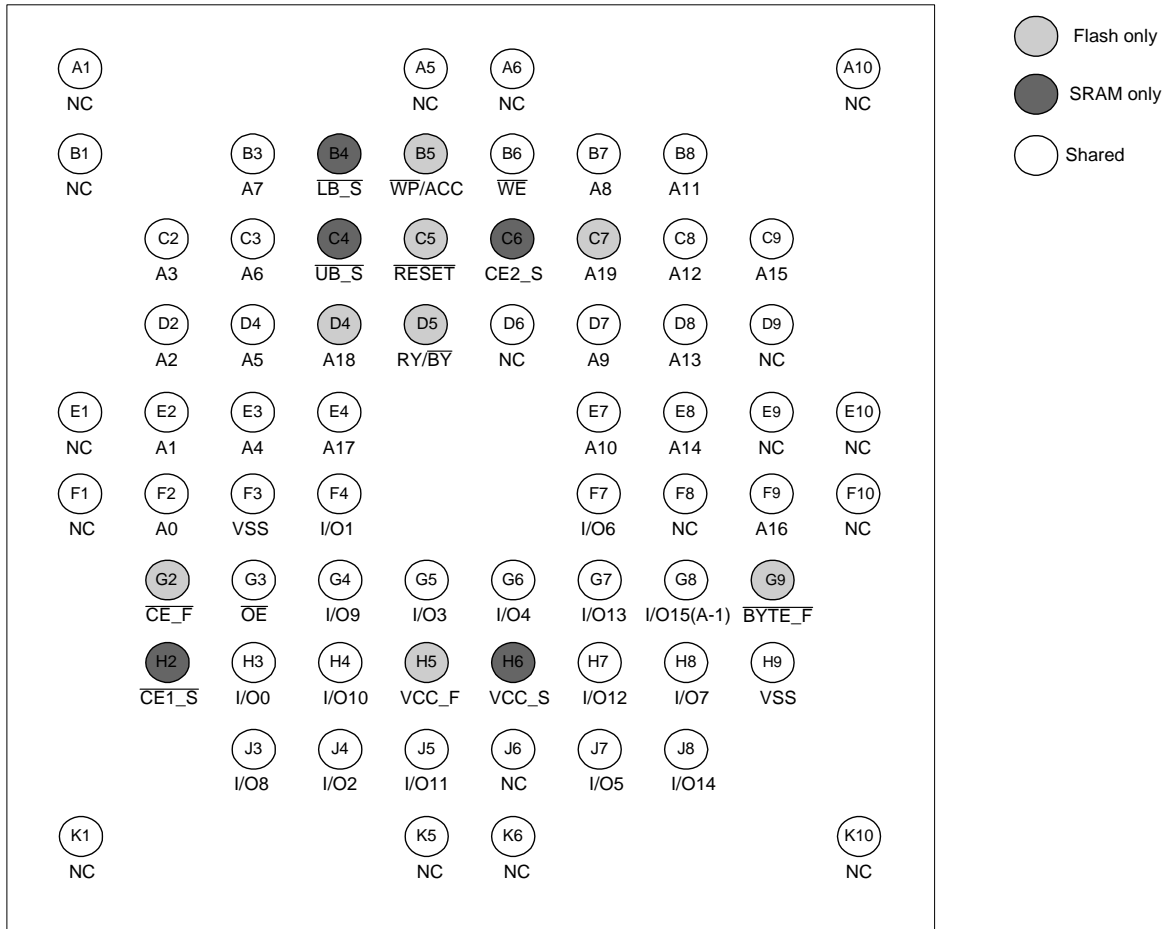
The device offers complete compatibility with the **JEDEC single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bits**: RY/BY pin, I/O₇ (\overline{Data} Polling) and I/O₆/I/O₂ (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low VCC detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-s y s t e m or via programming equipment.

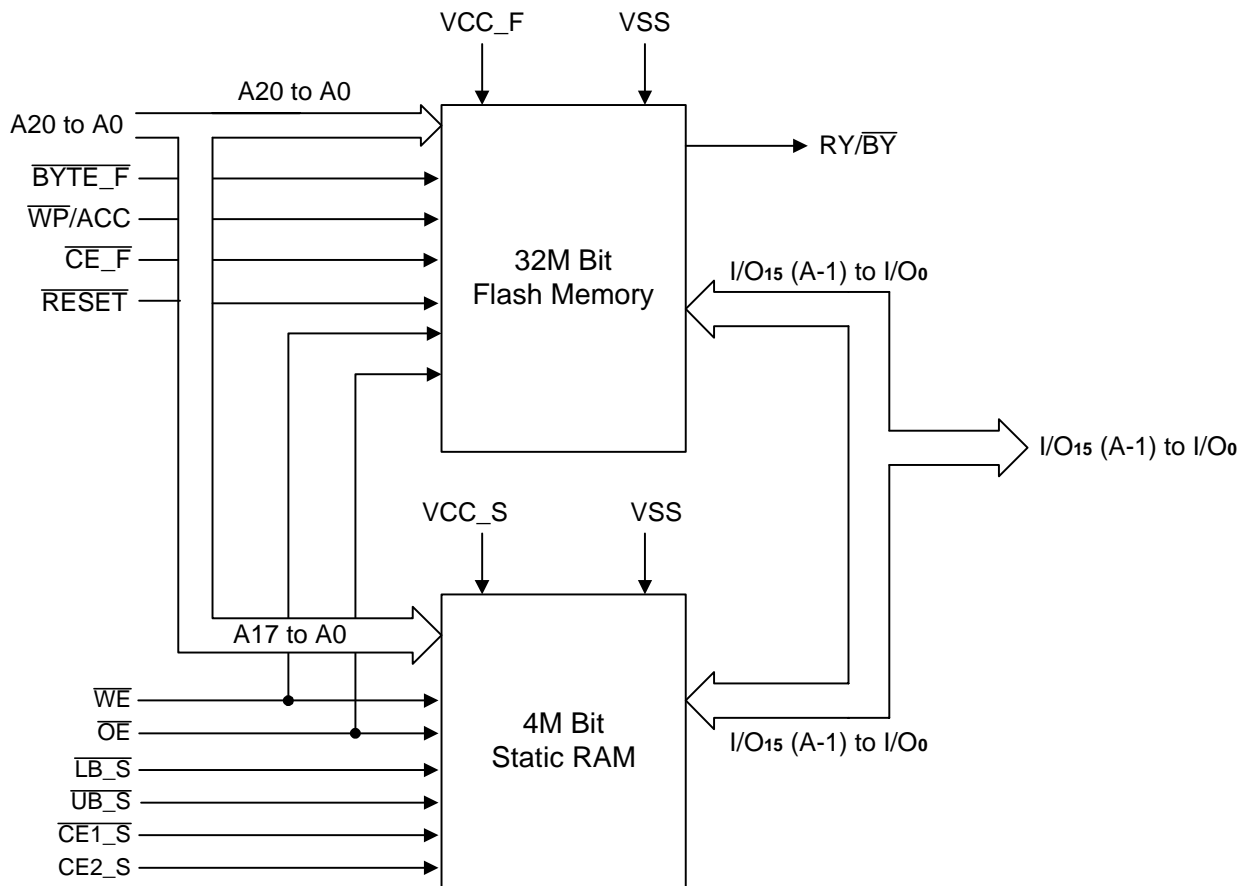
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

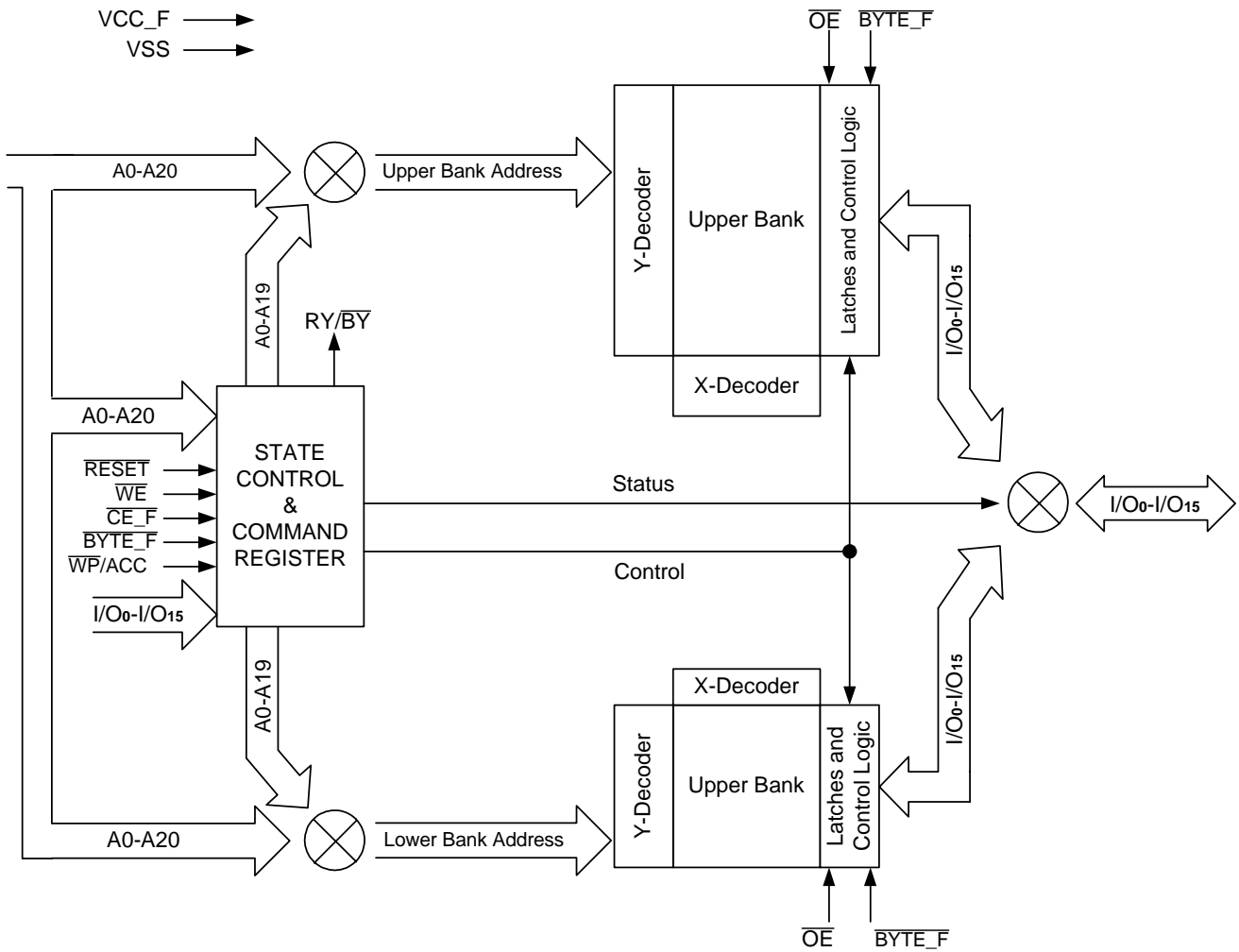
Pin Configurations
**■ 69-Ball TFBGA
Top View**

Special Handling Instructions for TFBGA Package

Special handling is required for Flash Memory products in TFBGA packages. Flash memory devices in TFBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time

Product Information Guide

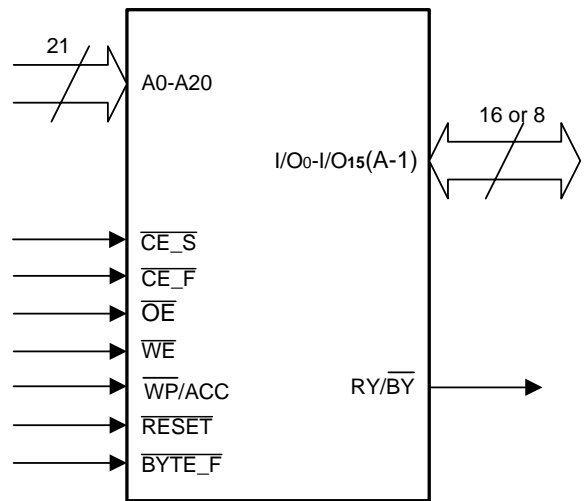
| Part Number | | A82DL32x4T(U) |
|-----------------------|---|---------------|
| Speed Options | Standard Voltage Range: VCC_F/VCC_S=2.7-3.6V | 70 |
| Max Access Time (ns) | | 70 |
| CE_F/CE_S Access (ns) | | 70 |
| OE Access (ns) | | 40 |

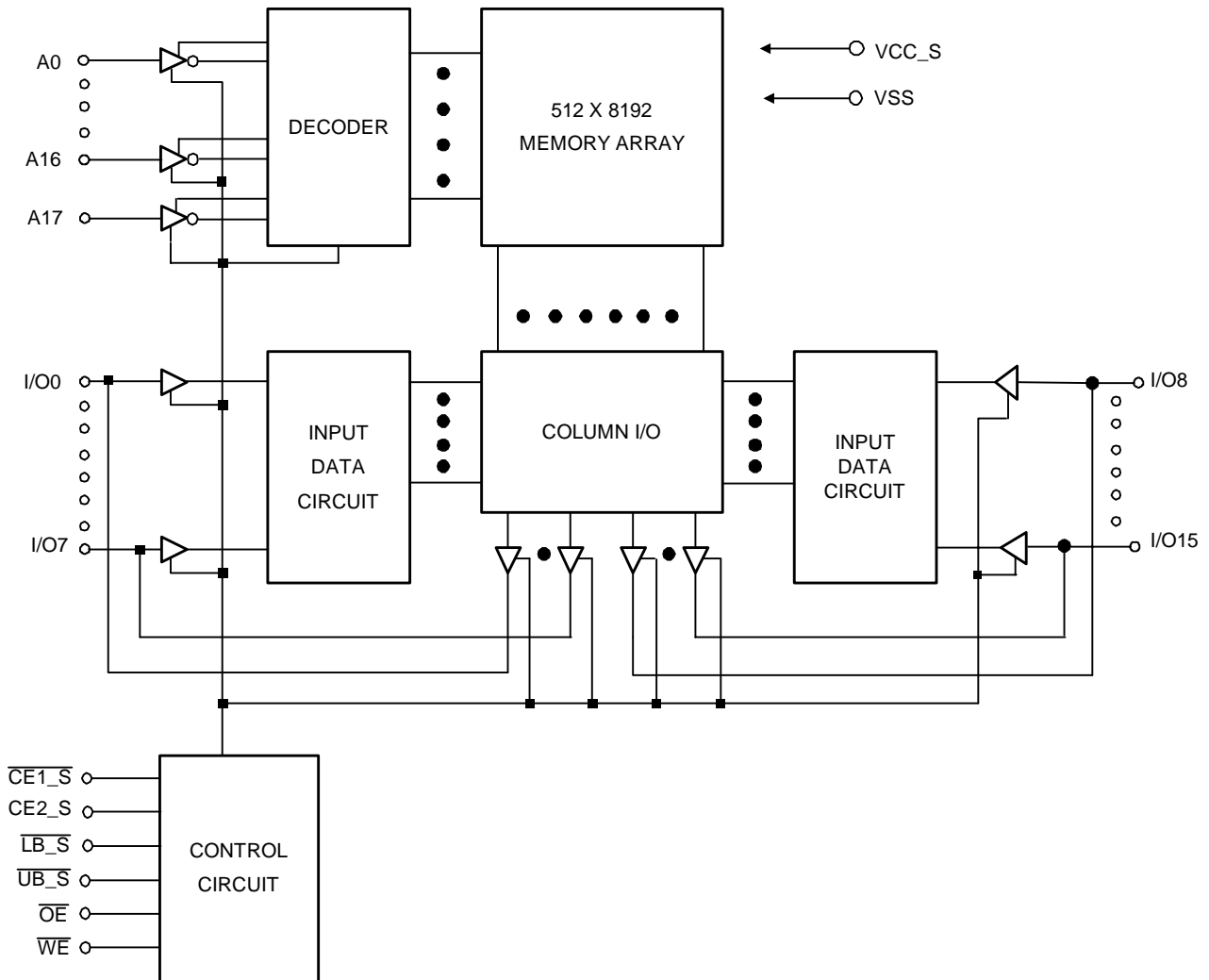
MCP Block Diagram


Flash Block Diagram


Pin Descriptions

| Pin No. | Description | |
|--------------------------------------|---|------------------------------|
| A0 – A20 | Address Inputs | |
| I/O ₀ - I/O ₁₄ | Data Inputs/Outputs | |
| I/O ₁₅ (A-1) | I/O ₁₅ | Data Input/Output, Word Mode |
| | A-1 | LSB Address Input, Byte Mode |
| $\overline{\text{CE}}_F$ | Chip Enable (Flash) | |
| $\overline{\text{CE}}_S$ | Chip Enable (SRAM) | |
| $\overline{\text{WE}}$ | Write Enable | |
| $\overline{\text{OE}}$ | Output Enable | |
| $\overline{\text{WP}}/\text{ACC}$ | Hardware Write Protect/Acceleration Pin | |
| $\overline{\text{RESET}}$ | Hardware Reset Pin, Active Low | |
| $\overline{\text{BYTE}}_F$ | Selects 8-bit or 16-bit Mode | |
| $\text{RY}/\overline{\text{BY}}$ | Ready/ $\overline{\text{BUSY}}$ Output | |
| VSS | Ground | |
| VCC _F | Power Supply (Flash) | |
| VCC _S | Power Supply (SRAM) | |
| NC | Pin Not Connected Internally | |

Logic Symbol


SRAM Block Diagram


DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the

command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1-1. Device Bus Operations – Flash Byte Mode ($\overline{\text{BYTE_F}} = V_{IH}$)

| Operation (Notes 1, 2) | $\overline{\text{CE_F}}$ | $\overline{\text{CE1_S}}$ | CE2_S | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | A0-A20 | $\overline{\text{LB_S}}$ (Note3) | $\overline{\text{UB_S}}$ (Note3) | $\overline{\text{RESET}}$ | $\overline{\text{WP/ACC}}$ (Note 4) | I/O7-I/O0 | I/O15-I/O0 |
|----------------------------|---------------------------|----------------------------|-----------------|------------------------|------------------------|-------------------------------------|-----------------------------------|-----------------------------------|---------------------------|-------------------------------------|------------------|------------------|
| Read from Flash | L | H | X | L | H | A _{IN} | X | X | H | L/H | I _{OUT} | I _{OUT} |
| | | X | L | | | | | | | | | |
| Write to Flash | L | H | X | H | L | A _{IN} | X | X | H | (Note 4) | I _{IN} | I _{IN} |
| | | X | L | | | | | | | | | |
| Standby | $V_{CC} \pm 0.3 V$ | H | X | X | X | X | X | X | $V_{CC} \pm 0.3 V$ | H | High-Z | High-Z |
| | | X | L | | | | | | | | | |
| Output Disable | L | L | H | H | H | X | L | X | H | L/H | High-Z | High-Z |
| | | | | | | | X | L | | | | |
| Flash Hardware Reset | X | H | X | X | X | X | X | X | L | L/H | High-Z | High-Z |
| | | X | L | | | | | | | | | |
| | | H | X | | | | | | | | | |
| Sector Protect (Notes) | L | X | L | H | L | SA, A6 = L, A1 = H, A0 = L | X | X | V _{ID} | L/H | I _{IN} | X |
| | | H | X | | | | | | | | | |
| Sector Unprotect (Note 5) | L | X | L | H | L | SA, A6 = H, A1 = H, A0 = L | X | X | V _{ID} | (Note 6) | I _{IN} | X |
| Temporary Sector Unprotect | X | H | X | X | X | A _{IN} | X | X | V _{ID} | (Note 6) | I _{IN} | High-Z |
| | | X | L | | | | | | | | I _{OUT} | I _{OUT} |
| Read from SRAM | H | L | H | L | H | A _{IN} | H | L | H | X | High-Z | I _{OUT} |
| | | | | | | | L | H | | | I _{OUT} | High-Z |
| | | | | | | | L | L | | | I _{IN} | I _{IN} |
| Write to SRAM | H | L | H | X | L | A _{IN} | H | L | H | X | High-Z | I _{IN} |
| | | | | | | | L | H | | | I _{IN} | High-Z |

Legend: L = Logic Low = V_{IL} , H = Logic High = V_{IH} , $V_{ID} = 8.5-12.5 V$, $V_{HH} = 9.0 \pm 0.5 V$, X = Don't Care, SA = Sector Address, A_{IN} = Address In, I_{IN} = Data In, I_{OUT} = Data Out

Notes:

1. Other operations except for those indicated in this column are inhibited.
2. Do not apply $\overline{\text{CE_F}} = V_{IL}$, $\overline{\text{CE1_S}} = V_{IL}$ and $\text{CE2_S} = V_{IH}$ at the same time.
3. Don't care or open $\overline{\text{LB_S}}$ or $\overline{\text{UB_S}}$.
4. The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.
5. If $\overline{\text{WP/ACC}} = V_{IL}$, the two outermost boot sectors remain protected. If $\overline{\text{WP/ACC}} = V_{IH}$, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If $\overline{\text{WP/ACC}} = V_{HH}$, all sectors will be unprotected.

Table 1-2. Device Bus Operations – Flash Byte Mode ($\overline{\text{BYTE_F}} = V_{IL}$)

| Operation (Notes 1, 2) | $\overline{\text{CE_F}}$ | $\overline{\text{CE1_S}}$ | $\overline{\text{CE2_S}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | A0-A20 | $\overline{\text{LB_S}}$ (Note3) | $\overline{\text{UB_S}}$ (Note3) | RESET | $\overline{\text{WP/ACC}}$ (Note 4) | I/O7– I/O0 | I/O15– I/O8 |
|------------------------------|---------------------------|----------------------------|----------------------------|------------------------|------------------------|-------------------------------------|--------------------------------------|--------------------------------------|-----------------------|--|------------------|--------------------------------|
| Read from Flash | L | H | X | L | H | A _{IN} | X | X | H | L/H | I _{OUT} | High-Z |
| | | X | L | | | | | | | | | |
| Write to Flash | L | H | X | H | L | A _{IN} | X | X | H | (Note 3) | I _{IN} | I/O14–8 =Hi-Z; I/O15=A-1 |
| | | X | L | | | | | | | | | |
| Standby | $V_{CC} \pm 0.3 V$ | H | X | X | X | X | X | X | $V_{CC_F} \pm 0.3 V$ | H | High-Z | High-Z |
| | | X | L | | | | | | | | | |
| Output Disable | L | L | H | H | H | X | L | X | H | L/H | High-Z | High-Z |
| | | | | H | X | X | X | L | | | | |
| Flash Hardware Reset | X | H | X | X | X | X | X | X | L | L/H | High-Z | High-Z |
| | | X | L | | | | | | | | | |
| Sector Protect (Notes) | L | H | X | H | L | SA, A6 = L, A1 = H, A0 = L | X | X | V _{ID} | L/H | I _{IN} | X |
| | | X | L | | | | | | | | | |
| Sector Unprotect (Note 5) | L | H | X | H | L | SA, A6 = H, A1 = H, A0 = L | X | X | V _{ID} | (Note 6) | I _{IN} | X |
| | | X | L | | | | | | | | | |
| Temporary Sector Unprotect | X | H | X | X | X | A _{IN} | X | X | V _{ID} | (Note 6) | I _{IN} | High-Z |
| | | X | L | | | | | | | | | |
| Read from SRAM | H | L | H | L | H | A _{IN} | H | L | H | X | I _{OUT} | I _{OUT} |
| | | | | | | | H | L | | | High-Z | I _{OUT} |
| | | | | | | | L | H | | | I _{OUT} | High-Z |
| Write to SRAM | H | L | H | X | L | A _{IN} | H | L | H | X | I _{IN} | I _{IN} |
| | | | | | | | L | H | | | High-Z | I _{IN} |
| | | | | | | | L | H | | | I _{IN} | High-Z |

Legend: L = Logic Low = V_{IL} , H = Logic High = V_{IH} , $V_{ID} = 8.5\text{--}12.5 V$, $V_{HH} = 9.0 \pm 0.5 V$, X = Don't Care, SA = Sector Address, A_{IN} = Address In (for Flash Byte Mode, I/O15=A-1), I_{IN} = Data In, I_{OUT} = Data Out

Notes:

- Other operations except for those indicated in this column are inhibited.
- Do not apply $\overline{\text{CE_F}} = V_{IL}$, $\overline{\text{CE1_S}} = V_{IL}$ and $\overline{\text{CE2_S}} = V_{IH}$ at the same time.
- Don't care or open $\overline{\text{LB_S}}$ or $\overline{\text{UB_S}}$.
- The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.
- If $\overline{\text{WP/ACC}} = V_{IL}$, the two outermost boot sectors remain protected. If $\overline{\text{WP/ACC}} = V_{IH}$, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If $\overline{\text{WP/ACC}} = V_{HH}$, all sectors will be unprotected.

Word/Byte Configuration

The $\overline{\text{BYTE_F}}$ pin determines whether the I/O pins I/O₁₅-I/O₀ operate in the byte or word configuration. If the $\overline{\text{BYTE_F}}$ pin is set at logic "1", the device is in word configuration, I/O₁₅-I/O₀ are active and controlled by $\overline{\text{CE_F}}$ and $\overline{\text{OE}}$.

If the $\overline{\text{BYTE_F}}$ pin is set at logic "0", the device is in byte configuration, and only I/O₆-I/O₇ are active and controlled by $\overline{\text{CE_F}}$ and $\overline{\text{OE}}$. I/O₈-I/O₁₄ are tri-stated, and I/O₁₅ pin is used as an input for the LSB(A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the $\overline{\text{CE_F}}$ and $\overline{\text{OE}}$ pins to V_{IL} . $\overline{\text{CE_F}}$ is the power control and selects the device. $\overline{\text{OE}}$ is the output control and gates array data to the output pins. $\overline{\text{WE}}$ should remain at V_{H} . The $\overline{\text{BYTE_F}}$ pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

See "Requirements for Reading Array Data" for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 11 for the timing waveform, lcc1_F in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive $\overline{\text{WE}}$ and $\overline{\text{CE_F}}$ to V_{IL} , and $\overline{\text{OE}}$ to V_{H} .

For program operations, the $\overline{\text{BYTE_F}}$ pin determines whether the device accepts program data in bytes or words. Refer to "Word/Byte Configuration" for more information.

The device features an Unlock Bypass mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The "Word / Byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequence.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables 3-4 indicate the address range that each sector occupies. The device address space is divided into two banks: Bank 1 contains the boot/parameter sectors, and Bank 2 contains the larger, code sectors of uniform size. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "sector address" is the address bits required to uniquely select a sector.

lcc2_F in the DC Characteristics table represents the active current specification for the write mode. The "AC

Characteristics" section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the $\overline{\text{WP_ACC}}$ pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{H} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{H} from the $\overline{\text{WP_ACC}}$ pin returns the device to normal operation. Note that the $\overline{\text{WP_ACC}}$ pin must not be at V_{H} for operations other than accelerated programming, or device damage may result. In addition, the $\overline{\text{WP_ACC}}$ pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on I/O₇-I/O₀. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in the other bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 18 shows how read and write cycles may be initiated for simultaneous operation with zero latency. lcc6_F and lcc7_F in the DC Characteristics table represent the current specifications for read-while-program and read-while-erase, respectively.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the $\overline{\text{OE}}$ input.

The device enters the CMOS standby mode when the $\overline{\text{CE_F}}$ & $\overline{\text{RESET}}$ pins are both held at $V_{\text{CC_F}} \pm 0.3\text{V}$. (Note that this is a more restricted voltage range than V_{H} .) If $\overline{\text{CE_F}}$ and $\overline{\text{RESET}}$ are held at V_{H} , but not within $V_{\text{CC_F}} \pm 0.3\text{V}$, the device will be in the standby mode, but the standby current will be greater. The device requires the standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

lcc3_F in the DC Characteristics tables represent the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{acc} + 30ns$. The automatic sleep mode is independent of the \overline{CE}_F , \overline{WE} and \overline{OE} control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{cc4_F} in the DC Characteristics table represents the automatic sleep mode current specification.

\overline{RESET} : Hardware Reset Pin

The \overline{RESET} pin provides a hardware method of resetting the device to reading array data. When the system drives the \overline{RESET} pin low for at least a period of t_{RP} , the device immediately terminates any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the \overline{RESET} pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the \overline{RESET} pulse. When \overline{RESET} is held at $V_{SS} \pm 0.3V$, the device draws CMOS standby current (I_{cc4_F}). If \overline{RESET} is held at V_{IL} but not within $V_{SS} \pm 0.3V$, the standby current will be greater.

The \overline{RESET} pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If \overline{RESET} is asserted during a program or erase operation, the $\overline{RY}/\overline{BY}$ pin remains a "0" (busy) until the internal reset operation is complete, which requires a time t_{READY} (during Embedded Algorithms). The system can thus monitor $\overline{RY}/\overline{BY}$ to determine whether the reset operation is complete. If \overline{RESET} is asserted when a program or erase operation is not executing ($\overline{RY}/\overline{BY}$ pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the \overline{RESET} pin return to V_{IH} .

Refer to the AC Characteristics tables for \overline{RESET} parameters and diagram.

Output Disable Mode

When the \overline{OE} input is at V_{IH} , output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. A82DL32x4T(U) Device Bank Divisions

| Device Part Number | Bank 1 | | Bank 2 | |
|--------------------|----------|--|----------|-------------------------------|
| | Megabits | Sector Sizes | Megabits | Sector Sizes |
| A82DL3224 | 4 Mbit | Eight 8 Kbyte/4 Kword, three 64 Kbyte/32 Kword | 28 Mbit | Fifty-six 64 Kbyte/32 Kword |
| A82DL3234 | 8 Mbit | Eight 8 Kbyte/4 Kword, seven 64 Kbyte/32 Kword | 24 Mbit | Forty-eight 64 Kbyte/32 Kword |
| A82DL3244 | 16 Mbit | Eight 8 Kbyte/4 Kword, fifteen 64 Kbyte/32 Kword | 16 Mbit | Thirty-two 64 Kbyte/32 Kword |

Table 3. Sector Addresses for Top Boot Sector Devices

| A29DL324T | A29DL323T | A29DL322T | Sector | Sector Address A20–A12 | Sector Size (Kbytes/Kwords) | (x8) Address Range | (x16) Address Range | | | |
|-----------|-----------|-----------|--------|---------------------------|--------------------------------|-----------------------|------------------------|-------|-----------------|-----------------|
| Bank 2 | Bank 2 | Bank 2 | SA0 | 00000xxx | 64/32 | 000000h-00FFFFh | 000000h-007FFFh | | | |
| | | | SA1 | 000001xxx | 64/32 | 010000h-01FFFFh | 008000h-00FFFFh | | | |
| | | | SA2 | 000010xxx | 64/32 | 020000h-02FFFFh | 010000h-017FFFh | | | |
| | | | SA3 | 000011xxx | 64/32 | 030000h-03FFFFh | 018000h-1FFFFFh | | | |
| | | | SA4 | 000100xxx | 64/32 | 040000h-04FFFFh | 020000h-027FFFh | | | |
| | | | SA5 | 000101xxx | 64/32 | 050000h-05FFFFh | 028000h-02FFFFh | | | |
| | | | SA6 | 000110xxx | 64/32 | 060000h-06FFFFh | 030000h-037FFFh | | | |
| | | | SA7 | 000111xxx | 64/32 | 070000h-07FFFFh | 038000h-03FFFFh | | | |
| | | | SA8 | 001000xxx | 64/32 | 080000h-08FFFFh | 040000h-047FFFh | | | |
| | | | SA9 | 001001xxx | 64/32 | 090000h-09FFFFh | 048000h-04FFFFh | | | |
| | | | SA10 | 001010xxx | 64/32 | 0A0000h-0AFFFFh | 050000h-057FFFh | | | |
| | | | SA11 | 001011xxx | 64/32 | 0B0000h-0BFFFFh | 058000h-05FFFFh | | | |
| | | | SA12 | 001100xxx | 64/32 | 0C0000h-0CFFFFh | 060000h-067FFFh | | | |
| | | | SA13 | 001101xxx | 64/32 | 0D0000h-0DFFFFh | 068000h-06FFFFh | | | |
| | | | SA14 | 001110xxx | 64/32 | 0E0000h-0EFFFFh | 070000h-077FFFh | | | |
| | | | SA15 | 001111xxx | 64/32 | 0F0000h-0FFFFFh | 078000h-07FFFFh | | | |
| | | | SA16 | 010000xxx | 64/32 | 100000h-10FFFFh | 080000h-087FFFh | | | |
| | | | SA17 | 010001xxx | 64/32 | 110000h-11FFFFh | 088000h-08FFFFh | | | |
| | | | SA18 | 010010xxx | 64/32 | 120000h-12FFFFh | 090000h-097FFFh | | | |
| | | | SA19 | 010011xxx | 64/32 | 130000h-13FFFFh | 098000h-09FFFFh | | | |
| | | | SA20 | 010100xxx | 64/32 | 140000h-14FFFFh | 0A0000h-0A7FFFh | | | |
| | | | SA21 | 010101xxx | 64/32 | 150000h-15FFFFh | 0A8000h-0AFFFFh | | | |
| | | | SA22 | 010110xxx | 64/32 | 160000h-16FFFFh | 0B0000h-0B7FFFh | | | |
| | | | SA23 | 010111xxx | 64/32 | 170000h-17FFFFh | 0B8000h-0BFFFFh | | | |
| | | | SA24 | 011000xxx | 64/32 | 180000h-18FFFFh | 0C0000h-0C7FFFh | | | |
| | | | SA25 | 011001xxx | 64/32 | 190000h-19FFFFh | 0C8000h-0CFFFFh | | | |
| | | | SA26 | 011010xxx | 64/32 | 1A0000h-1AFFFFh | 0D0000h-0D7FFFh | | | |
| | | | SA27 | 011011xxx | 64/32 | 1B0000h-1BFFFFh | 0D8000h-0DFFFFh | | | |
| | | | SA28 | 011100xxx | 64/32 | 1C0000h-1CFFFFh | 0E0000h-0E7FFFh | | | |
| | | | SA29 | 011101xxx | 64/32 | 1D0000h-1DFFFFh | 0E8000h-0EFFFFh | | | |
| | | | SA30 | 011110xxx | 64/32 | 1E0000h-1EFFFFh | 0F0000h-0F7FFFh | | | |
| | | | SA31 | 011111xxx | 64/32 | 1F0000h-1FFFFFh | 0F8000h-0FFFFFh | | | |
| | | | Bank 1 | Bank 2 | Bank 2 | SA32 | 10000xxx | 64/32 | 200000h-20FFFFh | 100000h-107FFFh |
| | | | | | | SA33 | 100001xxx | 64/32 | 210000h-21FFFFh | 108000h-10FFFFh |
| | | | | | | SA34 | 100010xxx | 64/32 | 220000h-22FFFFh | 110000h-117FFFh |
| | | | | | | SA35 | 100011xxx | 64/32 | 230000h-23FFFFh | 118000h-11FFFFh |
| | | | | | | SA36 | 100100xxx | 64/32 | 240000h-24FFFFh | 120000h-127FFFh |
| | | | | | | SA37 | 100101xxx | 64/32 | 250000h-25FFFFh | 128000h-12FFFFh |
| | | | | | | SA38 | 100110xxx | 64/32 | 260000h-26FFFFh | 130000h-137FFFh |
| | | | | | | SA39 | 100111xxx | 64/32 | 270000h-27FFFFh | 138000h-13FFFFh |
| | | | | | | SA40 | 101000xxx | 64/32 | 280000h-28FFFFh | 140000h-147FFFh |
| | | | | | | SA41 | 101001xxx | 64/32 | 290000h-29FFFFh | 148000h-14FFFFh |
| | | | | | | SA42 | 101010xxx | 64/32 | 2A0000h-2AFFFFh | 150000h-157FFFh |
| | | | | | | SA43 | 101011xxx | 64/32 | 2B0000h-2BFFFFh | 158000h-15FFFFh |
| | | | | | | SA44 | 101100xxx | 64/32 | 2C0000h-2CFFFFh | 160000h-167FFFh |
| | | | | | | SA45 | 101101xxx | 64/32 | 2D0000h-2DFFFFh | 168000h-16FFFFh |
| | | | | | | SA46 | 101110xxx | 64/32 | 2E0000h-2EFFFFh | 170000h-177FFFh |
| SA47 | 101111xxx | 64/32 | | | | 2F0000h-2FFFFFh | 178000h-17FFFFh | | | |

Table 3 Sector Addresses for Top Boot Sector Devices

| A29DL324T | A29DL323T | A29DL322T | Sector | Sector Address A20–A12 | Sector Size (Kbytes/Kwords) | (x8) Address Range | (x16) Address Range |
|-----------|-----------|-----------|------------------|---------------------------|--------------------------------|-----------------------|------------------------|
| Bank 1 | Bank 1 | Bank 2 | SA48 | 000000xxx | 64/32 | 300000h-30FFFFh | 180000h–187FFFh |
| | | | SA49 | 000001xxx | 64/32 | 310000h-31FFFFh | 188000h–18FFFFh |
| | | | SA50 | 000010xxx | 64/32 | 320000h-32FFFFh | 190000h–197FFFh |
| | | | SA51 | 000011xxx | 64/32 | 330000h-33FFFFh | 198000h–19FFFFh |
| | | | SA52 | 000100xxx | 64/32 | 340000h-34FFFFh | 1A0000h–1A7FFFh |
| | | | SA53 | 000101xxx | 64/32 | 350000h-35FFFFh | 1A8000h–1AFFFFh |
| | | | SA54 | 000110xxx | 64/32 | 360000h-36FFFFh | 1B0000h–1B7FFFh |
| | | SA55 | 000111xxx | 64/32 | 370000h-37FFFFh | 1B8000h–1BFFFFh | |
| | | Bank 1 | SA56 | 001000xxx | 64/32 | 380000h-38FFFFh | 1C0000h–1C7FFFh |
| | | | SA57 | 001001xxx | 64/32 | 390000h-39FFFFh | 1C8000h–1CFFFFh |
| | | | SA58 | 001010xxx | 64/32 | 3A0000h-3AFFFFh | 1D0000h–1D7FFFh |
| | | | SA59 | 001011xxx | 64/32 | 3B0000h-3BFFFFh | 1D8000h–1DFFFFh |
| | | | SA60 | 001100xxx | 64/32 | 3C0000h-3CFFFFh | 1E0000h–1E7FFFh |
| | | | SA61 | 001101xxx | 64/32 | 3D0000h-3DFFFFh | 1E8000h–1EFFFFh |
| | | | SA62 | 001110xxx | 64/32 | 3E0000h-3EFFFFh | 1F0000h–1F7FFFh |
| | | | SA63 | 001111xxx | 8/4 | 3F0000h-3FFFFFFh | 1F8000h–1F8FFFh |
| | | | SA64 | 010000xxx | 8/4 | 3F2000h-3F3FFFh | 1F9000h–1F9FFFh |
| | | | SA65 | 010001xxx | 8/4 | 3F4000h-3F5FFFh | 1FA000h–1FAFFFh |
| | | | SA66 | 010010xxx | 8/4 | 3F6000h-3F7FFFh | 1FB000h–1FBFFFh |
| | | | SA67 | 010011xxx | 8/4 | 3F8000h-3F9FFFh | 1FC000h–1FCFFFh |
| SA68 | 010100xxx | | 8/4 | 3FA000h-3FBFFFh | 1FD000h–1FDFFFh | | |
| SA69 | 010101xxx | 8/4 | 3FC000h-3FDFFFh | 1FE000h–1FEFFFh | | | |
| SA70 | 010110xxx | 8/4 | 3FE000h-3FFFFFFh | 1FF000h–1FFFFFFh | | | |

Note:

The address range is A20: A-1 in byte mode ($\overline{\text{BYTE_F}} = \text{VIL}$) or A20:A0 in word mode ($\overline{\text{BYTE_F}} = \text{VIH}$). The bank address bits are A20-A18 for A29DL3224T, A20 and A19 for A29DL3234T, and A20 for A29DL3244T.

Table 4. Sector Addresses for Bottom Boot Sector Devices

| A29DL324U | A29DL323U | A29DL322U | Sector | Sector Address A20–A12 | Sector Size (Kbytes/Kwords) | (x8) Address Range | (x16) Address Range |
|-----------|-----------|-----------|-----------------|---------------------------|--------------------------------|-----------------------|------------------------|
| Bank 2 | Bank 1 | Bank 1 | SA0 | 00000000 | 8/4 | 000000h-001FFFh | 000000h-000FFFh |
| | | | SA1 | 00000001 | 8/4 | 002000h-003FFFh | 001000h-001FFFh |
| | | | SA2 | 00000010 | 8/4 | 004000h-005FFFh | 002000h-002FFFh |
| | | | SA3 | 00000011 | 8/4 | 006000h-007FFFh | 003000h-003FFFh |
| | | | SA4 | 00000100 | 8/4 | 008000h-009FFFh | 004000h-004FFFh |
| | | | SA5 | 00000101 | 8/4 | 00A000h-00BFFFh | 005000h-005FFFh |
| | | | SA6 | 00000110 | 8/4 | 00C000h-00DFFFh | 006000h-006FFFh |
| | | | SA7 | 00000111 | 8/4 | 00E000h-00FFFFh | 007000h-007FFFh |
| | | | SA8 | 000001XXX | 64/32 | 010000h-01FFFFh | 008000h-00FFFFh |
| | | | SA9 | 000010XXX | 64/32 | 020000h-02FFFFh | 010000h-017FFFh |
| | | | SA10 | 000011XXX | 64/32 | 030000h-03FFFFh | 018000h-01FFFFh |
| | | | SA11 | 000100XXX | 64/32 | 040000h-04FFFFh | 020000h-027FFFh |
| | | | SA12 | 000101XXX | 64/32 | 050000h-05FFFFh | 028000h-02FFFFh |
| | | | SA13 | 000110XXX | 64/32 | 060000h-06FFFFh | 030000h-037FFFh |
| | | SA14 | 000111XXX | 64/32 | 070000h-07FFFFh | 038000h-03FFFFh | |
| | | SA15 | 001000XXX | 64/32 | 080000h-08FFFFh | 040000h-047FFFh | |
| | | SA16 | 001001XXX | 64/32 | 090000h-09FFFFh | 048000h-04FFFFh | |
| | | SA17 | 001010XXX | 64/32 | 0A0000h-0AFFFFh | 050000h-057FFFh | |
| | | SA18 | 001011XXX | 64/32 | 0B0000h-0BFFFFh | 058000h-05FFFFh | |
| | | SA19 | 001100XXX | 64/32 | 0C0000h-0CFFFFh | 060000h-067FFFh | |
| | | SA20 | 001101XXX | 64/32 | 0D0000h-0DFFFFh | 068000h-06FFFFh | |
| | SA21 | 001110XXX | 64/32 | 0E0000h-0EFFFFh | 070000h-077FFFh | | |
| | SA22 | 001111XXX | 64/32 | 0F0000h-0FFFFFh | 078000h-07FFFFh | | |
| | SA23 | 010000XXX | 64/32 | 100000h-10FFFFh | 080000h-087FFFh | | |
| | SA24 | 010001XXX | 64/32 | 110000h-11FFFFh | 088000h-08FFFFh | | |
| | SA25 | 010010XXX | 64/32 | 120000h-12FFFFh | 090000h-097FFFh | | |
| | SA26 | 010011XXX | 64/32 | 130000h-13FFFFh | 098000h-09FFFFh | | |
| | SA27 | 010100XXX | 64/32 | 140000h-14FFFFh | 0A0000h-0A7FFFh | | |
| | SA28 | 010101XXX | 64/32 | 150000h-15FFFFh | 0A8000h-0AFFFFh | | |
| | SA29 | 010110XXX | 64/32 | 160000h-16FFFFh | 0B0000h-0B7FFFh | | |
| | SA30 | 010111XXX | 64/32 | 170000h-17FFFFh | 0B8000h-0BFFFFh | | |
| | SA31 | 011000XXX | 64/32 | 180000h-18FFFFh | 0C0000h-0C7FFFh | | |
| | SA32 | 011001XXX | 64/32 | 190000h-19FFFFh | 0C8000h-0CFFFFh | | |
| | SA33 | 011010XXX | 64/32 | 1A0000h-1AFFFFh | 0D0000h-0D7FFFh | | |
| | SA34 | 011011XXX | 64/32 | 1B0000h-1BFFFFh | 0D8000h-0DFFFFh | | |
| | SA35 | 011100XXX | 64/32 | 1C0000h-1CFFFFh | 0E0000h-0E7FFFh | | |
| | SA36 | 011101XXX | 64/32 | 1D0000h-1DFFFFh | 0E8000h-0EFFFFh | | |
| | SA37 | 011110XXX | 64/32 | 1E0000h-1EFFFFh | 0F0000h-0F7FFFh | | |
| | SA38 | 011111XXX | 64/32 | 1F0000h-1FFFFFh | 0F8000h-0FFFFFh | | |
| | SA39 | 100000XXX | 64/32 | 200000h-20FFFFh | 100000h-107FFFh | | |
| | SA40 | 100001XXX | 64/32 | 210000h-21FFFFh | 108000h-10FFFFh | | |
| | SA41 | 100010XXX | 64/32 | 220000h-22FFFFh | 110000h-117FFFh | | |
| | SA42 | 100011XXX | 64/32 | 230000h-23FFFFh | 118000h-11FFFFh | | |
| | SA43 | 100100XXX | 64/32 | 240000h-24FFFFh | 120000h-127FFFh | | |
| | SA44 | 100101XXX | 64/32 | 250000h-25FFFFh | 128000h-12FFFFh | | |
| | SA45 | 100110XXX | 64/32 | 260000h-26FFFFh | 130000h-137FFFh | | |
| | SA46 | 100111XXX | 64/32 | 270000h-27FFFFh | 138000h-13FFFFh | | |
| SA47 | 101000XXX | 64/32 | 280000h-28FFFFh | 140000h-147FFFh | | | |
| Bank 2 | Bank 2 | Bank 2 | | | | | |

| A29DL324U | A29DL323U | A29DL322U | Sector | Sector Address A20–A12 | Sector Size (Kbytes/Kwords) | (x8) Address Range | (x16) Address Range |
|-----------|-----------|-----------|------------------|---------------------------|--------------------------------|-----------------------|------------------------|
| Bank 2 | Bank 2 | Bank 2 | SA48 | 101001XXX | 64/32 | 290000h-29FFFFh | 148000h-14FFFFh |
| | | | SA49 | 101010XXX | 64/32 | 2A0000h-2AFFFFh | 150000h-157FFFh |
| | | | SA50 | 101011XXX | 64/32 | 2B0000h-2BFFFFh | 158000h-15FFFFh |
| | | | SA51 | 101100XXX | 64/32 | 2C0000h-2CFFFFh | 160000h-167FFFh |
| | | | SA52 | 101101XXX | 64/32 | 2D0000h-2DFFFFh | 168000h-16FFFFh |
| | | | SA53 | 101110XXX | 64/32 | 2E0000h-2EFFFFh | 170000h-177FFFh |
| | | | SA54 | 101111XXX | 64/32 | 2F0000h-2FFFFFFh | 178000h-17FFFFh |
| | | | SA55 | 111000XXX | 64/32 | 300000h-30FFFFh | 180000h-187FFFh |
| | | | SA56 | 111001XXX | 64/32 | 310000h-31FFFFh | 188000h-18FFFFh |
| | | | SA57 | 110010XXX | 64/32 | 320000h-32FFFFh | 190000h-197FFFh |
| | | | SA58 | 110011XXX | 64/32 | 330000h-33FFFFh | 198000h-19FFFFh |
| | | | SA59 | 110100XXX | 64/32 | 340000h-34FFFFh | 1A0000h-1A7FFFh |
| | | | SA60 | 110101XXX | 64/32 | 350000h-35FFFFh | 1A8000h-1AFFFFh |
| | | | SA61 | 110110XXX | 64/32 | 360000h-36FFFFh | 1B0000h-1B7FFFh |
| | | | SA62 | 110111XXX | 64/32 | 370000h-37FFFFh | 1B8000h-1BFFFFh |
| | | | SA63 | 111000XXX | 64/32 | 380000h-38FFFFh | 1C0000h-1C7FFFh |
| | | | SA64 | 111001XXX | 64/32 | 390000h-39FFFFh | 1C8000h-1CFFFFh |
| | | | SA65 | 111010XXX | 64/32 | 3A0000h-3AFFFFh | 1D0000h-1D7FFFh |
| | | | SA66 | 111011XXX | 64/32 | 3B0000h-3BFFFFh | 1D8000h-1DFFFFh |
| | | | SA67 | 111100XXX | 64/32 | 3C0000h-3CFFFFh | 1E0000h-1E7FFFh |
| SA68 | 111101XXX | 64/32 | 3D0000h-3DFFFFh | 1E8000h-1EFFFFh | | | |
| SA69 | 111110XXX | 64/32 | 3E0000h-3EFFFFh | 1F0000h-1F7FFFh | | | |
| SA70 | 111111XXX | 64/32 | 3F0000h-3FFFFFFh | 1F8000h-1FFFFFFh | | | |

Note:

The address range is A20: A-1in byte mode ($\overline{\text{BYTE_F}} = V_{IL}$) or A20:A0 in word mode ($\overline{\text{BYTE_F}} = V_{IH}$). The bank address bits are A20-A18 for A29DL3224U, A20 and A19 for A29DL3234U, and A20 for A29DL3244U.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on I/O₇ - I/O₀. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register. When using programming equipment, the autoselect mode requires V_{DD} (8.5V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 5. In addition, when verifying sector protection, the sector address

must appear on the appropriate highest order address bits. (see Table 3-4). Table 5 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on I/O₇ - I/O₀.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 12. This method does not require V_{DD}. Refer to the Autoselect Command Sequence section for more information.

Table 5. A82DL32x4T(U) Autoselect Codes (High Voltage Method)

| Description | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | A20 to A12 | A11 to A10 | A9 | A8 to A7 | A6 | A5 to A4 | A3 | A2 | A1 | A0 | I/O ₈ to I/O ₁₅ | | I/O ₇ to I/O ₀ |
|-----------------------|------------------------|------------------------|------------------------|------------|------------|-----------------|----------|----|----------|----|----|----|----|---|---|--------------------------------------|
| | | | | | | | | | | | | | | $\overline{\text{BYTE}} = \text{V}_{\text{IH}}$ | $\overline{\text{BYTE}} = \text{V}_{\text{IL}}$ | |
| Manufacturer ID: AMIC | L | L | H | BA | X | V _{DD} | X | L | X | L | L | L | L | X | X | 37h |
| Device ID: A29DL8224 | L | L | H | BA | X | V _{DD} | X | L | X | X | X | L | H | 22h | X | 55h (T), 56h (U) |
| Device ID: A29DL8234 | L | L | H | BA | X | V _{DD} | X | L | X | X | X | L | H | 22h | X | 50h (T), 53h (U) |
| Device ID: A29DL8244 | L | L | H | BA | X | V _{DD} | X | L | X | X | X | L | H | 22h | X | 5Ch (T), 5Fh (U) |
| Continuation ID | L | L | H | X | X | V _{DD} | X | L | X | X | X | H | H | X | X | 7Fh |
| Read Sector Status | L | L | H | SA | X | V _{DD} | X | L | X | L | L | H | L | X | X | 01h (protected), 00h (unprotected) |

L=Logic Low= V_{IL}, H=Logic High=V_{IH}, SA=Sector Address, X=Don't Care, BA=Bank Address

Note: The autoselect codes may also be accessed in-system via command sequences.

Sector/Sector Block Protection and Unprotection

(Note: For the following discussion, the term “sector” applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Tables 6 and 7).

Table 6. Top Boot Sector/Sector Block Addresses for Protection/Unprotection
Table 6. Top Boot Sector/Sector Block Addresses for Protection/Unprotection

| Sector / Sector Block | A20–A12 | Sector / Sector Block Size |
|-----------------------|--|----------------------------|
| SA0 | 000000XXXX | 64 Kbytes |
| SA1-SA3 | 000001XXXX, 000010XXXX, 000011XXXX | 192 (3x64) Kbytes |
| SA4-SA7 | 0001XXXXXX | 256 (4x64) Kbytes |
| SA8-SA11 | 0010XXXXXX | 256 (4x64) Kbytes |
| SA12-SA15 | 0011XXXXXX | 256 (4x64) Kbytes |
| SA16-SA19 | 0100XXXXXX | 256 (4x64) Kbytes |
| SA20-SA23 | 0101XXXXXX | 256 (4x64) Kbytes |
| SA24-SA27 | 0110XXXXXX | 256 (4x64) Kbytes |
| SA28-SA31 | 0111XXXXXX | 256 (4x64) Kbytes |
| SA32-SA35 | 1000XXXXXX | 256 (4x64) Kbytes |
| SA36-SA39 | 1001XXXXXX | 256 (4x64) Kbytes |
| SA40-SA43 | 1010XXXXXX | 256 (4x64) Kbytes |
| SA44-SA47 | 1011XXXXXX | 256 (4x64) Kbytes |
| SA48-SA51 | 1100XXXXXX | 256 (4x64) Kbytes |
| SA52-SA55 | 1101XXXXXX | 256 (4x64) Kbytes |
| SA56-SA59 | 1110XXXXXX | 256 (4x64) Kbytes |
| SA60-SA62 | 111100XXX, 111101XXX, 111110XXX | 192 (3x64) Kbytes |
| SA63 | 111111000 | 8 Kbytes |
| SA64 | 111111001 | 8 Kbytes |
| SA65 | 111111010 | 8 Kbytes |
| SA66 | 111111011 | 8 Kbytes |
| SA67 | 111111100 | 8 Kbytes |
| SA68 | 111111101 | 8 Kbytes |
| SA69 | 111111110 | 8 Kbytes |
| SA70 | 111111111 | 8 Kbytes |

Table 7. Bottom Boot Sector/Sector Block Addresses for Protection/Unprotection

| Sector / Sector Block | A20–A12 | Sector / Sector Block Size |
|-----------------------|---------------------------------------|----------------------------|
| SA70 | 111111XXXX | 64 Kbytes |
| SA69- SA67 | 111110XXX, 111101XXX, 111100XXX | 192 (3x64) Kbytes |
| SA66- SA63 | 1110XXXXXX | 256 (4x64) Kbytes |
| SA62- SA59 | 1101XXXXXX | 256 (4x64) Kbytes |
| SA58- SA55 | 1100XXXXXX | 256 (4x64) Kbytes |
| SA54- SA51 | 1011XXXXXX | 256 (4x64) Kbytes |
| SA50- SA47 | 1010XXXXXX | 256 (4x64) Kbytes |
| SA46-SA43 | 1001XXXXXX | 256 (4x64) Kbytes |
| SA42-SA39 | 1000XXXXXX | 256 (4x64) Kbytes |
| SA38-SA35 | 0111XXXXXX | 256 (4x64) Kbytes |
| SA34-SA31 | 0110XXXXXX | 256 (4x64) Kbytes |
| SA30-SA27 | 0101XXXXXX | 256 (4x64) Kbytes |
| SA26-SA23 | 0100XXXXXX | 256 (4x64) Kbytes |
| SA22-SA19 | 0011XXXXXX | 256 (4x64) Kbytes |
| SA18-SA15 | 0010XXXXXX | 256 (4x64) Kbytes |
| SA14-SA11 | 0001XXXXXX | 256 (4x64) Kbytes |
| SA10-SA8 | 000001XXX, 000010XXX, 000011XXX | 192 (3x64) Kbytes |
| SA7 | 000000111 | 8 Kbytes |
| SA6 | 000000110 | 8 Kbytes |
| SA5 | 000000101 | 8 Kbytes |
| SA4 | 000000100 | 8 Kbytes |
| SA3 | 000000011 | 8 Kbytes |
| SA2 | 000000010 | 8 Kbytes |
| SA1 | 000000001 | 8 Kbytes |
| SA0 | 000000000 | 8 Kbytes |

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection and unprotection can be implemented via two methods.

The primary method requires V_{DD} on the $\overline{\text{RESET}}$ pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 23 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The sector unprotect algorithm unprotects all sectors in parallel. All previously protected sectors must be individually re-protected. To change data in protected sectors efficiently, the temporary sector unprotect function is available. See "Temporary Sector/Sector Block Unprotect".

The alternate method for protection and unprotection is by software temporary sector /sector block unprotect command. See Figure 2 for Command Flow.

The device is shipped with all sectors unprotected.

It is possible to determine whether a sector is protected or unprotected. See the Autoselect Mode section for details.

Write Protect ($\overline{\text{WP}}/\text{ACC}$)

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{DD} . This function is one of two provided by the $\overline{\text{WP}}/\text{ACC}$ pin.

If the system asserts V_{IL} on the $\overline{\text{WP}}/\text{ACC}$ pin, the device disables program and erase functions in the two "outermost" 8 Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

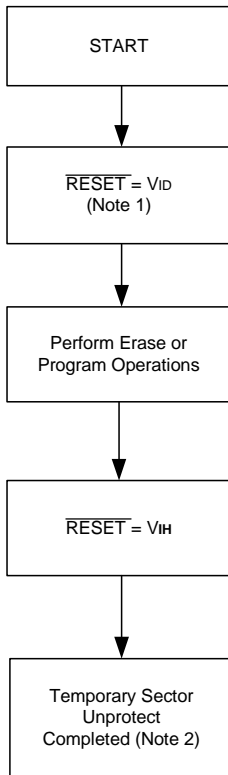
If the system asserts V_{IH} on the $\overline{\text{WP}}/\text{ACC}$ pin, the device reverts to whether the two outermost 8 Kbyte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection".

Note that the $\overline{\text{WP}}/\text{ACC}$ pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Temporary Sector/Sector Block Unprotect

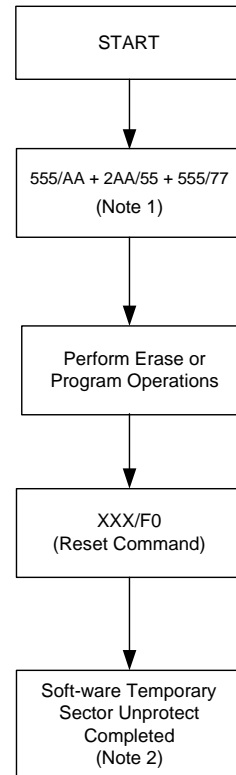
(Note: For the following discussion, the term "sector" applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Tables 6 and 7).)

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the $\overline{\text{RESET}}$ pin to V_{DD} (8.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{DD} is removed from the $\overline{\text{RESET}}$ pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and Figure 22 shows the timing diagrams, for this feature.



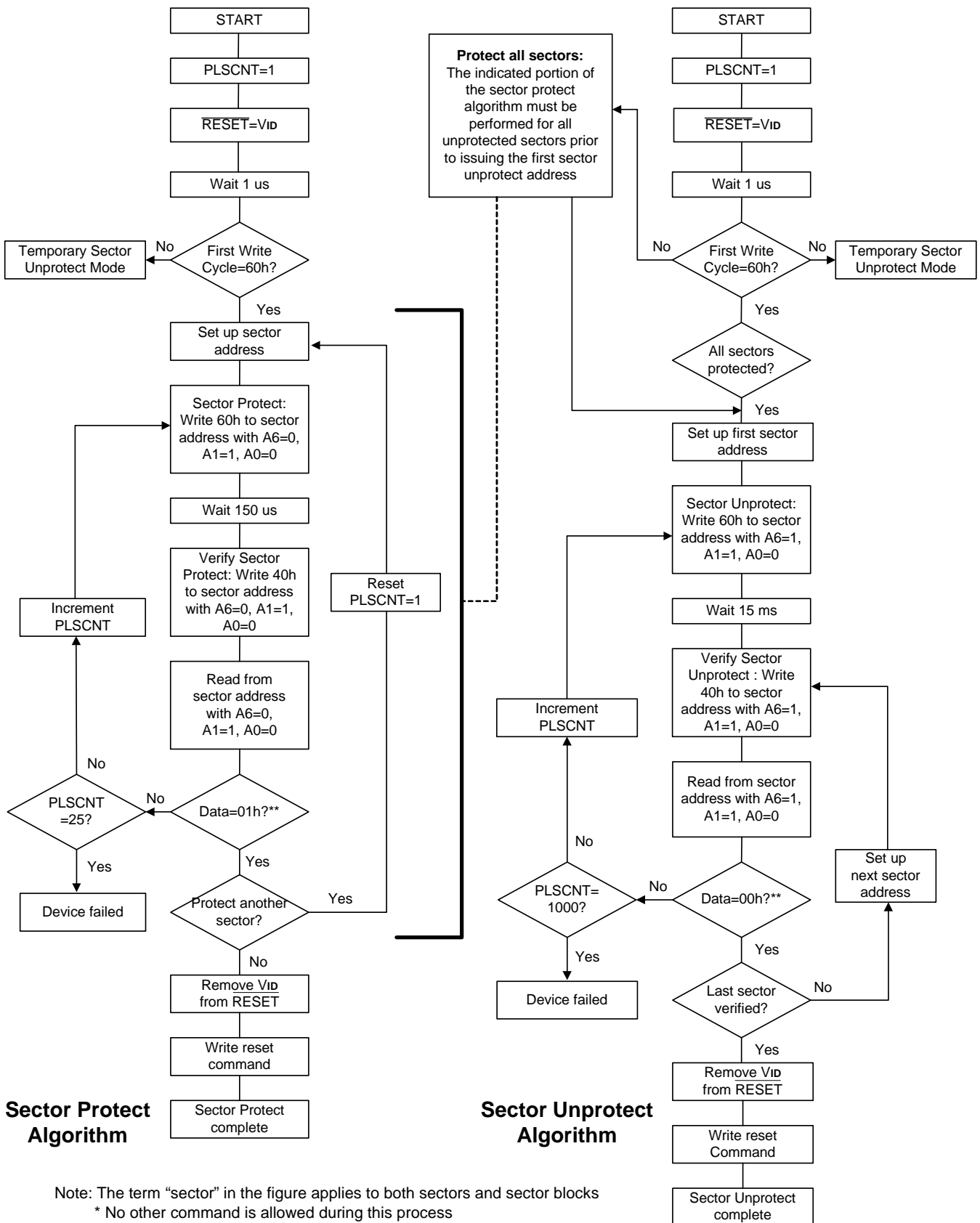
- Notes:
1. All protected sectors unprotected (If $\overline{WP}/ACC=V_{IL}$, outermost boot sectors will remain protected).
 2. All previously protected sectors are protected once again.

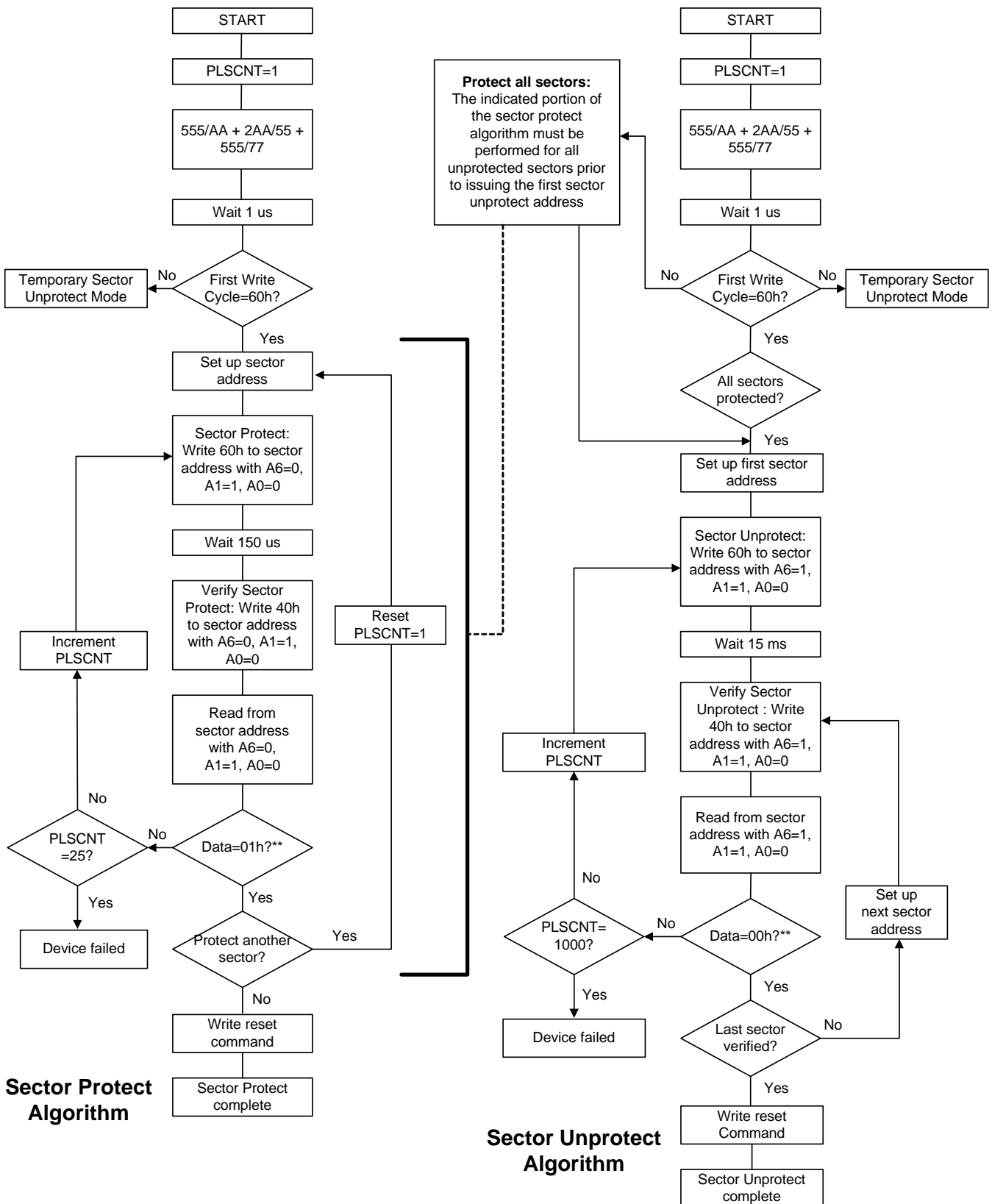
Figure 1-1. Temporary Sector Unprotect Operation by \overline{RESET} Mode



- Notes:
1. All protected sectors unprotected (If $\overline{WP}/ACC=V_{IL}$, outermost boot sectors will remain protected).
 2. All previously protected sectors are protected once again.

Figure 1-2. Temporary Sector Unprotect Operation by Software Mode


Figure 2-1. High Voltage Sector/Sector Block Protection and Unprotection Algorithms



Note: The term "sector" in the figure applies to both sectors and sector blocks
 * No other command is allowed during this process
 ** Access time is 200ns-300ns

Figure 2-2. Software Sector/Sector Block Protection and Unprotection Algorithms

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 12 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during VCC_F power-up and power-down transitions, or from system noise.

Low VCC Write Inhibit

When VCC_F is less than V_{Lko}, the device does not accept any write cycles. This protects data during VCC_F power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until VCC_F is greater than V_{Lko}. The system must provide the proper signals to the control pins to prevent unintentional writes when VCC_F is greater than V_{Lko}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5ns (typical) on \overline{OE} , $\overline{CE_F}$ or \overline{WE} do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE_F} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle, $\overline{CE_F}$ and \overline{WE} must be a logical zero while \overline{OE} is a logical one.

Power-Up Write Inhibit

If $\overline{WE} = \overline{CE_F} = V_{IL}$ and $\overline{OE} = V_{IH}$ during power up, the device does not accept commands on the rising edge of \overline{WE} . The internal state machine is automatically reset to reading array data on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 8-11. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 8-11. The system must write the reset command to return the device to the autoselect mode.

Table 8. CFI Query Identification String

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|--------------------------|--------------------------|-------------------------|--|
| 10h 11h 12h | 20h 22h 24h | 0051h 0052h 0059h | Query Unique ASCII string “QRY” |
| 13h 14h | 26h 28h | 0002h 0000h | Primary OEM Command Set |
| 15h 16h | 2Ah 2Ch | 0040h 0000h | Address for Primary Extended Table |
| 17h 18h | 2Eh 30h | 0000h 0000h | Alternate OEM Command Set (00h = none exists) |
| 19h 1Ah | 32h 34h | 0000h 0000h | Address for Alternate OEM Extended Table (00h = none exists) |

Table 9. System Interface String

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|--------------------------|--------------------------|-------|---|
| 1Bh | 36h | 0027h | VCC Min. (write/erase) I/O ₇ - I/O ₄ : volt, I/O ₃ - I/O ₀ : 100 millivolt |
| 1Ch | 38h | 0036h | VCC Max. (write/erase) I/O ₇ - I/O ₄ : volt, I/O ₃ - I/O ₀ : 100 millivolt |
| 1Dh | 3Ah | 0000h | Vpp Min. voltage (00h = no Vpp pin present) |
| 1Eh | 3Ch | 0000h | Vpp Max. voltage (00h = no Vpp pin present) |
| 1Fh | 3Eh | 0004h | Typical timeout per single byte/word write 2 ^N μs |
| 20h | 40h | 0000h | Typical timeout for Min. size buffer write 2 ^N μs (00h = not supported) |
| 21h | 42h | 000Ah | Typical timeout per individual block erase 2 ^N ms |
| 22h | 44h | 0000h | Typical timeout for full chip erase 2 ^N ms (00h = not supported) |
| 23h | 46h | 0005h | Max. timeout for byte/word write 2 ^N times typical |
| 24h | 48h | 0000h | Max. timeout for buffer write 2 ^N times typical |
| 25h | 4Ah | 0004h | Max. timeout per individual block erase 2 ^N times typical |
| 26h | 4Ch | 0000h | Max. timeout for full chip erase 2 ^N times typical (00h = not supported) |

Table 10 Device Geometry Definition

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|--------------------------|--------------------------|-------|---|
| 27h | 4Eh | 0015h | Device Size = 2 ^N byte |
| 28h | 50h | 0002h | Flash Device Interface description |
| 29h | 52h | 0000h | |
| 2Ah | 54h | 0000h | Max. number of byte in multi-byte write = 2 ^N (00h = not supported) |
| 2Bh | 56h | 0000h | |
| 2Ch | 58h | 0002h | Number of Erase Block Regions within device |
| 2Dh | 5Ah | 0007h | Erase Block Region 1 Information (refer to the CFI specification) |
| 2Eh | 5Ch | 0000h | |
| 2Fh | 5Eh | 0020h | |
| 30h | 60h | 0000h | |
| 31h | 62h | 001Eh | Erase Block Region 2 Information |
| 32h | 64h | 0000h | |
| 33h | 66h | 0000h | |
| 34h | 68h | 0001h | |
| 35h | 6Ah | 0000h | Erase Block Region 3 Information |
| 36h | 6Ch | 0000h | |
| 37h | 6Eh | 0000h | |
| 38h | 40h | 0000h | |
| 39h | 72h | 0000h | Erase Block Region 4 Information |
| 3Ah | 74h | 0000h | |
| 3Bh | 76h | 0000h | |
| 3Ch | 78h | 0000h | |

Table 11. Primary Vendor-Specific Extended Query

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|--------------------------|--------------------------|-------------------------|---|
| 40h 41h 42h | 80h 82h 84h | 0050h 0052h 0049h | Query-unique ASCII string "PRI" |
| 43h | 86h | 0031h | Major version number, ASCII |
| 44h | 88h | 0032h | Minor version number, ASCII |
| 45h | 8Ah | 0000h | Address Sensitive Unlock 0 = Required, 1 = Not Required |
| 46h | 8Ch | 0002h | Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write |
| 47h | 8Eh | 0001h | Sector Protect 0 = Not Supported, X = Number of sectors in per group |
| 48h | 90h | 0001h | Sector Temporary Unprotect 00 = Not Supported, 01 = Supported |
| 49h | 92h | 0004h | Sector Protect/Unprotect scheme 04 = A29L800 mode |
| 4Ah | 94h | 00XXh | Simultaneous Operation XX = 38 (A29DL8224) XX = 30 (A29DL8234) XX = 20 (A29DL8244) |
| 4Bh | 96h | 0000h | Burst Mode Type 00 = Not Supported, 01 = Supported |
| 4Ch | 98h | 0000h | Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page |
| 4Dh | 9Ah | 0085h | ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV |
| 4Eh | 9Ch | 0095h | ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV |
| 4Fh | 9Eh | 000Xh | Top/Bottom Boot Sector Flag 02h = Bottom Boot Device, 03h = Top Boot Device |
| 58h | B0h | 00XXh | Bank 1 Region Information – Number of Sectors on Bank 1 XX = 0F (A29DL322) XX = 17 (A29DL323) XX = 27 (A29DL324) |
| 59h | B2h | 00XXh | Bank 2 Region Information – Number of Sectors in Bank 2 XX = 38 (A29DL322) XX = 30 (A29DL323) XX = 20 (A29DL324) |
| 5Ah | B4h | 0000 | Bank 3 Region Information – Number of Sector in Bank 3 |
| 5Bh | B6h | 0000 | Bank 4 Region Information – Number of Sector in Bank 4 |

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 12 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of \overline{WE} or $\overline{CE_F}$, whichever happens later. All data is latched on the rising edge of \overline{WE} or $\overline{CE_F}$, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if I/O_s goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Figure 11 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to reading array data. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. If I/O_s goes high during a program or erase operation, writing the reset command returns the banks to reading array data

(or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 12 shows the address and data requirements. This method is an alternative to that shown in Table 5, which is intended for PROM programmers and requires V_{DD} on address pin A9. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence:

- A read cycle at address (BA)XX00h (where BA is the bank address) returns the manufacturer code.
- A read cycle at address (BA)XX01h in word mode (or (BA)XX02h in byte mode) returns the device code.
- A read cycle to an address containing a sector address (SA) within the same bank, and the address 02h on A7-A0 in word mode (or the address 04h on A6-A-1 in byte mode) returns 01h if the sector is protected, or 00h if it is unprotected. (Refer to Tables 3-4 for valid sector addresses).

The system must write the reset command to return to reading array data (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Byte/Word Program Command Sequence

The system may program the device by word or byte, depending on the state of the $\overline{BYTE_F}$ pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 12 shows the address and data requirements for the byte program command sequence. When the Embedded Program algorithm is complete, that bank then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using I/O₇, I/O₆, or RY/ \overline{BY} . Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from "0" back to a "1." Attempting to do so may cause that bank to set I/O_s = 1, or cause the I/O₇ and I/O₆ status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

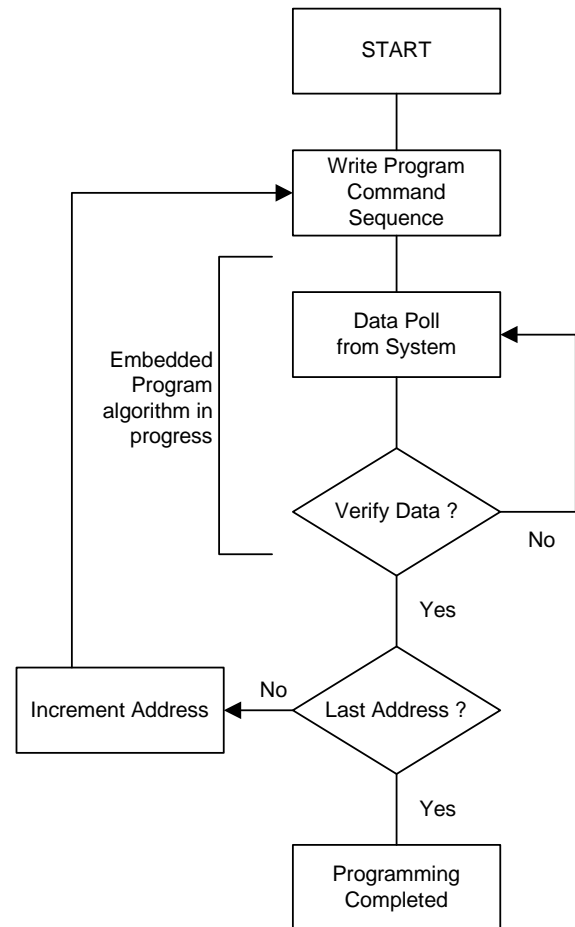
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 12 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The device then returns to reading array data.

The device offers accelerated program operations through the \overline{WP}/ACC pin. When the system asserts V_{HH} on the \overline{WP}/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the \overline{WP}/ACC pin to accelerate the operation. Note that the \overline{WP}/ACC pin must not be at V_{HH} any operation other than accelerated programming, or device damage may result. In addition, the \overline{WP}/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Figure 3 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 15 for timing diagrams.



Note : See Table 14 for program command sequence.

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 12 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using I/O₇, I/O₆, I/O₂, or RY/ $\overline{\text{BY}}$. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 17 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 12 shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 μs occurs. During the time-out period, additional sector addresses and sector erase commands within the bank may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 μs , otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to reading array data. The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor I/O₃ to determine if the sector erase timer has timed out (See the section on I/O₃: Sector Erase Timer.). The time-out begins from the rising edge of the final $\overline{\text{WE}}$ pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading I/O₇, I/O₆, I/O₂, or RY/ $\overline{\text{BY}}$ in the erasing bank.

Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 17 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 μs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

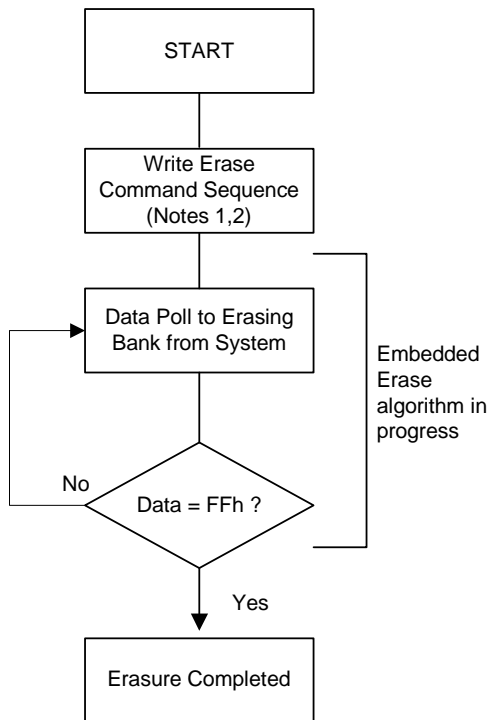
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 μs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on I/O₇–I/O₀. The system can use I/O₇, or I/O₆ and I/O₂ together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the I/O₇ or I/O₆ status bits, just as in the standard Byte Program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is ignored when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Note :

1. See Table 14 for erase command sequence.
2. See the section on I/O₃ for information on the sector erase timer.

Figure 4. Erase Operation

Command Definitions
Table 12. A82DL32x4T(U) Command Definitions

| Command Sequence (Note 1) | | Cycle | Bus Cycles (Notes 2-5) | | | | | | | | | | | | | |
|---------------------------------|--|-------|------------------------|------|--------|------|-------|---------|--------|---------|---------------|------|-------|------|----|--|
| | | | First | | Second | | Third | | Fourth | | Fifth | | Sixth | | | |
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | | |
| Read (Note 6) | | 1 | RA | RD | | | | | | | | | | | | |
| Reset (Note 7) | | 1 | XXX | F0 | | | | | | | | | | | | |
| Autoselect (Note 8) | Manufacturer ID | Word | 4 | 555 | AA | 2AA | 55 | (BA)555 | 90 | (BA)X00 | 37 | | | | | |
| | | Byte | 4 | AAA | AA | 555 | 55 | (BA)AAA | 90 | (BA)X01 | (see Table 5) | | | | | |
| | Device ID | Word | 4 | 555 | AA | 2AA | 55 | (BA)555 | 90 | (BA)X01 | (see Table 5) | | | | | |
| | | Byte | 4 | AAA | AA | 555 | 55 | (BA)AAA | 90 | (BA)X02 | (see Table 5) | | | | | |
| | Continuation ID | Word | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X03 | 7F | | | | | |
| | | Byte | 4 | AAA | AA | 555 | 55 | AAA | 90 | X06 | 7F | | | | | |
| | Sector Protect Verify (Note 9) | Word | 4 | 555 | AA | 2AA | 55 | (BA)555 | 90 | (SA) | 00/01 | | | | | |
| | | Byte | 4 | AAA | AA | 555 | 55 | (BA)AAA | 90 | (SA)X04 | 00/01 | | | | | |
| | Command Temporary Sector Unprotect (Note 15) | | Word | 3 | 555 | AA | 2AA | 55 | 555 | 77 | | | | | | |
| | | | Byte | 3 | AAA | AA | 555 | 55 | AAA | 77 | | | | | | |
| Program | | Word | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | | |
| | | Byte | 4 | AAA | AA | 555 | 55 | AAA | A0 | PA | PD | | | | | |
| Unlock Bypass | | Word | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | | |
| | | Byte | 3 | AAA | AA | 555 | 55 | AAA | 20 | | | | | | | |
| Unlock Bypass Program (Note 10) | | 2 | XXX | A0 | PA | PD | | | | | | | | | | |
| Unlock Bypass Reset (Note 11) | | 2 | XXX | 90 | XXX | 00 | | | | | | | | | | |
| Chip Erase | | Word | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 | |
| | | Byte | 6 | AAA | AA | 555 | 55 | AAA | 80 | AA A | AA | 555 | 55 | AAA | 10 | |
| Sector Erase | | Word | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 | |
| | | Byte | 6 | AAA | AA | 555 | 55 | AAA | 80 | AAA | AA | 555 | 55 | SA | 30 | |
| Erase Suspend (Note 12) | | 1 | XXX | B0 | | | | | | | | | | | | |
| Erase Resume (Note 13) | | 1 | XXX | 30 | | | | | | | | | | | | |
| CFI Query (Note 14) | | Word | 1 | 55 | 98 | | | | | | | | | | | |
| | | Byte | 1 | AA | 98 | | | | | | | | | | | |

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

 PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the \overline{WE} or $\overline{CE_F}$ pulse, whichever happens later.

 PD = Data to be programmed at location PA. Data latches on the rising edge of \overline{WE} or $\overline{CE_F}$ pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A20 - A12 select a unique sector.

BA = Address of the bank that is being switched to autoselect mode, is in bypass mode, or is being erased.

Note:

- See Table 1 for description of bus operations.
- All values are in hexadecimal.
- Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.
- Data bits I/O₁₅-I/O₈ are don't care in command sequences. Except for RD and PD.
- Unless otherwise noted, address bits A20-A11 are don't cares.
- No unlock or command cycles required when bank is reading array data.
- The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if I/O₅ goes high (while the bank is providing status information).
- The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacture ID, or device ID information. Data bits I/O₁₅-I/O₈ are don't care. See the Autoselect Command Sequence section for more information.
- The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.
- The Unlock Bypass command is required prior to the Unlock Bypass Program Command.
- The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.
- The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and require the bank address.
- The Erase Resume command is valid only during the Erase.
- Command is valid when device is ready to read array data or when device is in autoselect mode.
- Once reset command is applied, software temporary unprotect is exit to return read array data. But under erase suspend condition, this command is still effective even a reset command has been applied. The reset command which can deactivate the software temporary unprotect command is useful only after the erase command is complete.

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: I/O_2 , I/O_3 , I/O_5 , I/O_6 , and I/O_7 . Table 13 and the following subsections describe the function of these bits. I/O_7 and I/O_6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, $\overline{RY/BY}$, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

I/O_7 : Data Polling

The $\overline{\text{Data}}$ Polling bit, I/O_7 , indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. $\overline{\text{Data}}$ Polling is valid after the rising edge of the final \overline{WE} pulse in the program or erase command sequence.

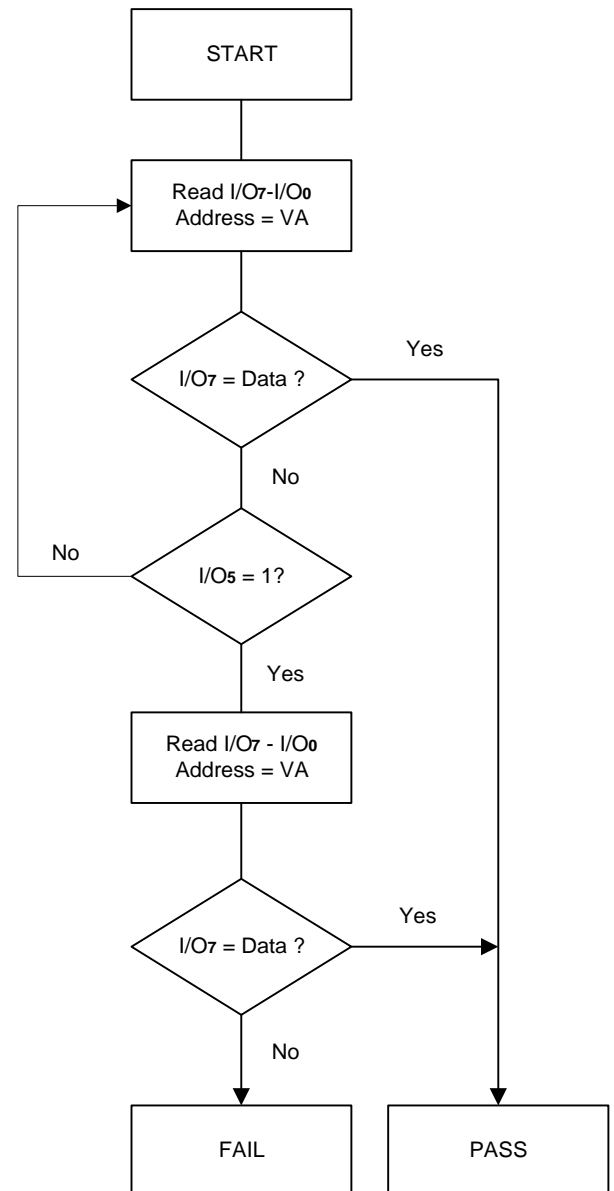
During the Embedded Program algorithm, the device outputs on I/O_7 the complement of the datum programmed to I/O_7 . This I/O_7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to I/O_7 . The system must provide the program address to read valid status information on I/O_7 . If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on I/O_7 is active for approximately $1\mu\text{s}$, then the device returns to reading array data.

During the Embedded Erase algorithm, $\overline{\text{Data}}$ Polling produces a "0" on I/O_7 . When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, $\overline{\text{Data}}$ Polling produces a "1" on I/O_7 . The system must provide an address within any of the sectors selected for erasure to read valid status information on I/O_7 .

After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on I/O_7 is active for approximately $100\mu\text{s}$, then the bank returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads I/O_7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, I/O_7 may change asynchronously with I/O_6 – I/O_5 while Output Enable (\overline{OE}) is asserted low. That is, the device may change from providing status information to valid data on I/O_7 . Depending on when the system samples the I/O_7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and I/O_7 has valid data, the data outputs on I/O_6 – I/O_5 may be still invalid. Valid data on I/O_6 – I/O_7 will appear on successive read cycles.

Table 13 shows the outputs for $\overline{\text{Data}}$ Polling on I/O_7 . Figure 5 shows the $\overline{\text{Data}}$ Polling algorithm. Figure 19 in the AC Characteristics section shows the $\overline{\text{Data}}$ Polling timing diagram.



Note :

1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
2. I/O_7 should be rechecked even if $I/O_5 = "1"$ because I/O_7 may change simultaneously with I/O_5 .

Figure 5. $\overline{\text{Data}}$ Polling Algorithm

R \overline{Y} /B \overline{Y} : Ready/Busy

The R \overline{Y} /B \overline{Y} is a dedicated, open-drain output pin that indicates whether an Embedded algorithm is in progress or complete. The R \overline{Y} /B \overline{Y} status is valid after the rising edge of the final \overline{WE} pulse in the command sequence. Since R \overline{Y} /B \overline{Y} is an open-drain output, several R \overline{Y} /B \overline{Y} pins can be tied together in parallel with a pull-up resistor to VCC_F.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 13 shows the outputs for R \overline{Y} /B \overline{Y} .

I/O₆: Toggle Bit I

Toggle Bit I on I/O₆ indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final \overline{WE} pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause I/O₆ to toggle.

The system may use either \overline{OE} or \overline{CE}_F to control the read cycles. When the operation is complete, I/O₆ stops toggling.

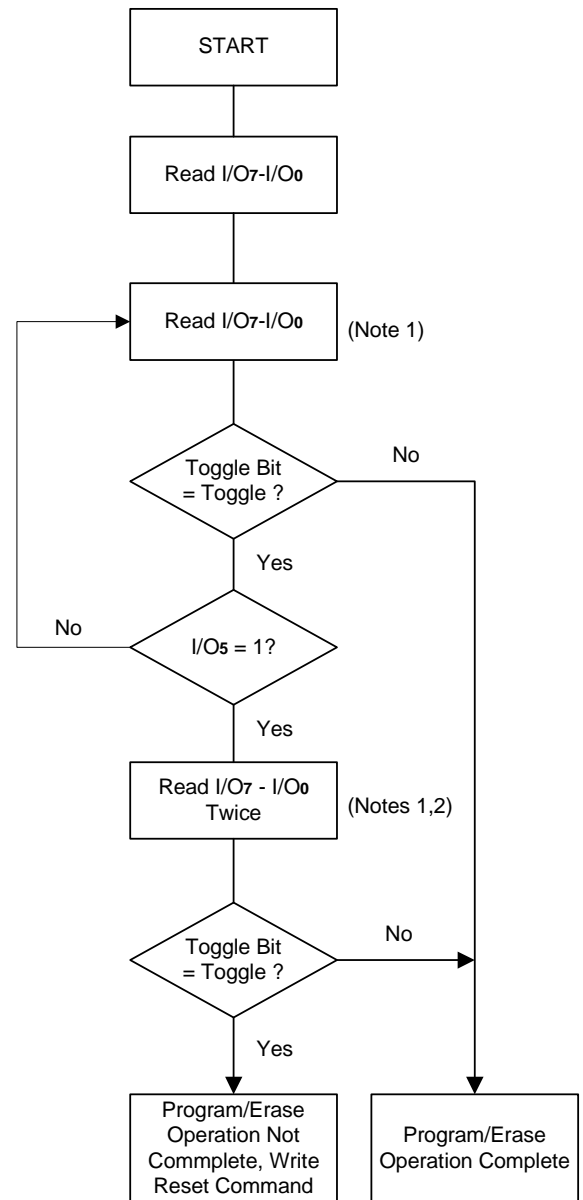
After an erase command sequence is written, if all sectors selected for erasing are protected, I/O₆ toggles for approximately 100 μ s, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use I/O₆ and I/O₂ together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), I/O₆ toggles. When the device enters the Erase Suspend mode, I/O₆ stops toggling. However, the system must also use I/O₂ to determine which sectors are erasing or erase-suspended. Alternatively, the system can use I/O₇ (see the subsection on "I/O₇: Data Polling").

If a program address falls within a protected sector, I/O₆ toggles for approximately 1 μ s after the program command sequence is written, then returns to reading array data.

I/O₆ also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 13 shows the outputs for Toggle Bit I on I/O₆. Figure 6 shows the toggle bit algorithm. Figure 20 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 23 shows the differences between I/O₂ and I/O₆ in graphical form. See also the subsection on I/O₂: Toggle Bit II.



Note:
The system should recheck the toggle bit even if I/O₅="1" because the toggle bit may stop toggling as I/O₅ changes to "1". See the subsections on I/O₆ and I/O₂ for more information.

Figure 6. Toggle Bit Algorithm

I/O₂: Toggle Bit II

The "Toggle Bit II" on I/O₂, when used with I/O₆, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final \overline{WE} pulse in the command sequence. I/O₂ toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either \overline{OE} or \overline{CE}_F to control the read cycles.) But I/O₂ cannot distinguish whether the sector is actively erasing or is erase-suspended. I/O₆, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 8 to compare outputs for I/O₂ and I/O₆.

Figure 6 shows the toggle bit algorithm in flowchart form, and the section "I/O₂: Toggle Bit II" explains the algorithm. See also the "I/O₆: Toggle Bit I" subsection. Figure 20 shows the toggle bit timing diagram. Figure 21 shows the differences between I/O₂ and I/O₆ in graphical form.

Reading Toggle Bits I/O₆, I/O₂

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read I/O₇-I/O₀ at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on I/O₇-I/O₀ on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of I/O₅ is high (see the section on I/O₅). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as I/O₅ went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data. The remaining scenario is that the system initially determines that the toggle bit is toggling and I/O₅ has not gone high. The system may continue to monitor the toggle bit and I/O₅ through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

I/O₅: Exceeded Timing Limits

I/O₅ indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions I/O₅ produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.

The device may output a "1" on I/O₅ if the system tries to program a "1" to a location that was previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the timing limit has been exceeded, I/O₅ produces a "1."

Under both these conditions, the system must write the reset command to return to reading array data (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

I/O₃: Sector Erase Timer

After writing a sector erase command sequence, the system may read I/O₃ to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, I/O₃ switches from "0" to "1." The system may ignore I/O₃ if the system can guarantee that the time between additional sector erase commands will always be less than 50 μ s. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on I/O₇ (Data Polling) or I/O₆ (Toggle Bit 1) to ensure the device has accepted the command sequence, and then read I/O₃. If I/O₃ is "1", the internally controlled erase cycle has begun; all further commands (Except Erase Suspend) are ignored until the erase operation is complete. If I/O₃ is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of I/O₃ prior to and following each subsequent sector erase command. If I/O₃ is high on the second status check, the last command might not have been accepted.

Table 13 shows the status of I/O₃ relative to the other status bits.

Table 13. Write Operation Status

| Status | | I/O ₇ (Note 2) | I/O ₆ | I/O ₅ (Note 1) | I/O ₃ | I/O ₂ (Note 2) | R _Y /B _Y | |
|--------------------|----------------------------|------------------------------|------------------|------------------------------|------------------|------------------------------|--------------------------------|---|
| Standard Mode | Embedded Program Algorithm | $\overline{\text{I/O}}_7$ | Toggle | 0 | N/A | No toggle | 0 | |
| | Embedded Erase Algorithm | 0 | Toggle | 0 | 1 | Toggle | 0 | |
| Erase Suspend Mode | Erase-Suspend-Read | Erase Suspended Sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| | | Non-Erase Suspend Sector | Data | Data | Data | Data | Data | 1 |
| | Erase-Suspend-Program | $\overline{\text{I/O}}_7$ | Toggle | 0 | N/A | N/A | 0 | |

Notes:

1. I/O₅ switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on I/O₅ for more information.
2. I/O₇ and I/O₂ require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.

ABSOLUTE MAXIMUM RATINGS*

| | |
|---|-----------------------------|
| Storage Temperature Plastic Packages. . . | -65°C to + 150°C |
| Ambient Temperature with Power Applied. -65°C to + 125°C | |
| Voltage with Respect to Ground | |
| VCC_F/VCC_S (Note 1) | -0.5V to +4.0V |
| A9, \overline{OE} & \overline{RESET} (Note 2) | -0.5V to +12.5V |
| \overline{WP} /ACC | -0.5V to +10.5V |
| All other pins (Note 1) | -0.5V to VCC_F/VCC_S + 0.5V |
| Output Short Circuit Current (Note 3) | 200mA |

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot VSS to -2.0V for periods of up to 20ns. Maximum DC voltage on input and I/O pins is VCC_F/VCC_S + 0.5V. See Figure 7. During voltage transitions, input or I/O pins may overshoot to VCC_F/VCC_S + 2.0V for periods up to 20ns. See Figure 8.
2. Minimum DC input voltage on A9, \overline{OE} , \overline{RESET} and \overline{WP} /ACC is -0.5V. During voltage transitions, A9, \overline{OE} , \overline{WP} /ACC and \overline{RESET} may overshoot VSS to -2.0V for periods of up to 20ns. See Figure 7. Maximum DC input voltage on A9 is +12.5V which may overshoot to 14.0V for periods up to 20ns. Maximum DC input voltage on \overline{WP} /ACC is +9.5V which may overshoot to +12.0V for period up to 20ns.
3. No more than one output is shorted to ground at a time. Duration of the short circuit should not be greater than one second.

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

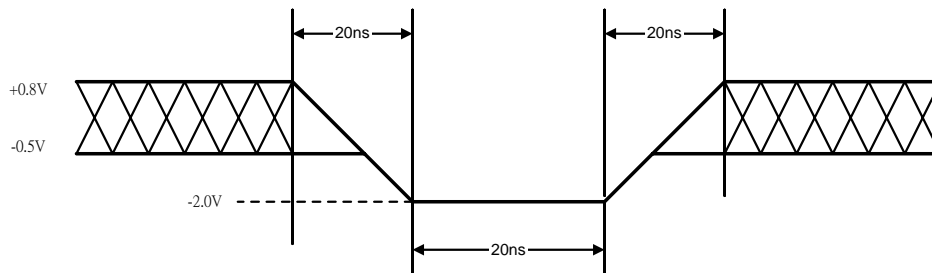
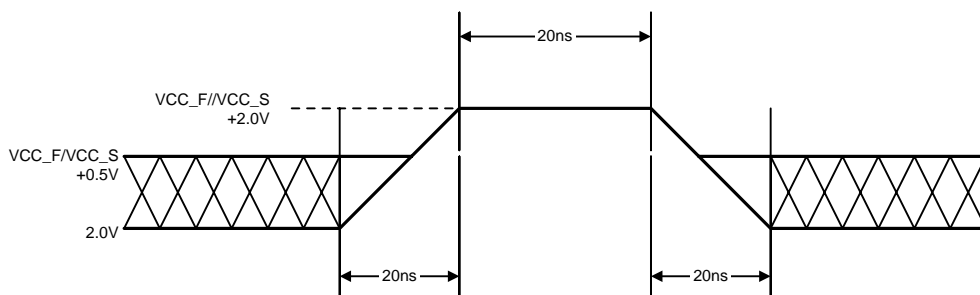
OPERATING RANGES
Industrial (I) Devices

Ambient Temperature (T_A) -40°C to +85°C

VCC Supply Voltages

VCC_F/VCC_S for all devices +2.7V to +3.6V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Figure 7. Maximum Negative Overshoot Waveform

Figure 8. Maximum Positive Overshoot Waveform


DC CHARACTERISTICS
CMOS Compatible

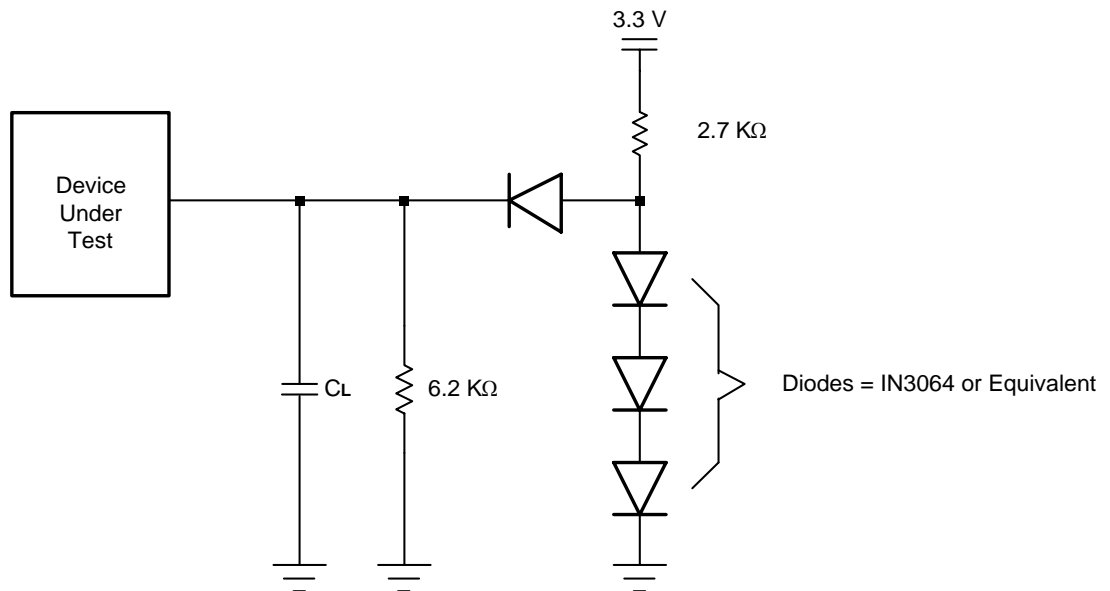
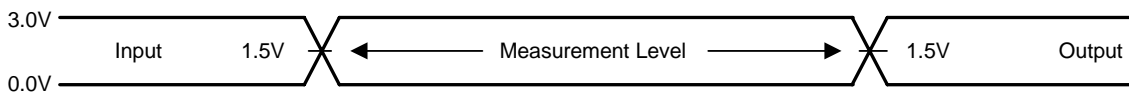
| Parameter Symbol | Parameter Description | Test Description | Min. | Typ. | Max. | Unit | |
|--------------------|--|--|-------------------------|------|-------------------------|------|----|
| I _{LI} | Input Load Current | V _{IN} = V _{SS} to V _{CC_F} . V _{CC_F} = V _{CC_F} Max | | | ±1.0 | μA | |
| I _{LIT} | A9 Input Load Current | V _{CC} = V _{CC} Max, A9 = 12.5V | | | 35 | μA | |
| I _{LO} | Output Leakage Current | V _{OUT} = V _{SS} to V _{CC_F} . V _{CC} = V _{CC_F} Max | | | ±1.0 | μA | |
| I _{CC1_F} | V _{CC_F} Active Read Current (Notes 1, 2) | Byte Mode $\overline{CE}_F = V_{IL}, \overline{OE} = V_{IH}$ | 5 MHz | 10 | 16 | mA | |
| | | | 1 MHz | 2 | 4 | | |
| | | Word Mode $\overline{CE}_F = V_{IL}, \overline{OE} = V_{IH}$ | 5 MHz | 10 | 16 | | |
| | | | 1 MHz | 2 | 4 | | |
| I _{CC2_F} | V _{CC_F} Active Write Current (Notes 2, 3) | $\overline{CE}_F = V_{IL}, \overline{OE} = V_{IH}$ | | 20 | 30 | mA | |
| I _{CC3_F} | V _{CC_F} Standby Current (Note 2) | $\overline{CE}_F = V_{IH}, \overline{RESET} = V_{CC_F} \pm 0.3V$ | | 0.2 | 5 | μA | |
| I _{CC4_F} | V _{CC_F} Reset Current (Note 2) | $\overline{RESET} = V_{SS} \pm 0.3V$ | | 0.2 | 5 | μA | |
| I _{CC5_F} | Automatic Sleep Mode (Note 2, 4) | V _{IH} = V _{CC_F} ± 0.3V; V _{IL} = V _{SS} ± 0.3V | | 0.2 | 5 | μA | |
| I _{CC6_F} | V _{CC_F} Active Read-While-Program Current (Notes 1, 2) | $\overline{CE}_F = V_{IL}, \overline{OE} = V_{IH}$ | Byte | | 21 | 45 | mA |
| | | | Word | | 21 | 45 | |
| I _{CC7_F} | V _{CC_F} Active Read-While-Erase Current (Notes 1, 2) | $\overline{CE}_F = V_{IL}, \overline{OE} = V_{IH}$ | Byte | | 21 | 45 | mA |
| | | | Word | | 21 | 45 | |
| I _{CC8_F} | V _{CC_F} Active Program-While-Erase-Suspended Current (Notes 2, 5) | $\overline{CE}_F = V_{IL}, \overline{OE} = V_{IH}$ | | 17 | 35 | mA | |
| I _{ACC} | ACC Accelerated Program Current, Word or Byte | $\overline{CE}_F = V_{IL}, \overline{OE} = V_{IH}$ | ACC pin | | 5 | 10 | mA |
| | | | V _{CC_F} pin | | 15 | 30 | |
| V _{IL} | Input Low Level | | -0.5 | | 0.8 | V | |
| V _{IH} | Input High Level | | 0.7 x V _{CC_F} | | V _{CC_F} + 0.3 | V | |
| V _{HH} | Voltage for \overline{WP} /ACC Sector Protect/Unprotect and Program Acceleration | V _{CC_F} = 3.0 V ± 10% | 8.5 | | 9.5 | V | |
| V _{ID} | Voltage for Autoselect and Temporary Unprotect Sector | V _{CC_F} = 3.0 V ± 10% | 8.5 | | 12.5 | V | |
| V _{oL} | Output Low Voltage | I _{oL} = 4.0mA, V _{CC_F} = V _{CC_F} Min | | | 0.45 | V | |
| V _{oH1} | Output High Voltage | I _{oH} = -2.0 mA, V _{CC_F} = V _{CC_F} Min | 0.85x V _{CC_F} | | | V | |
| V _{oH2} | | I _{oH} = -100 μA, V _{CC_F} = V _{CC} Min | V _{CC_F} - 0.4 | | | V | |
| V _{LKO} | Low V _{CC_F} Lock-Out Voltage (Note 5) | | 2.3 | | 2.5 | V | |

Notes:

1. The I_{CC} current listed is typically less than 2 mA/MHz, with \overline{OE} at V_{IH}.
2. Maximum I_{CC} specifications are tested with V_{CC_F} = V_{CC_F} max.
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{acc_F} + 30ns. Typical sleep mode current is 200nA.
5. Not 100% tested.

TEST CONDITIONS
Table 14. Test Specifications

| Test Condition | -70 | Unit |
|--|------------|------|
| Output Load | 1 TTL gate | |
| Output Load Capacitance, C_L (including jig capacitance) | 30 | pF |
| Input Rise and Fall Times | 5 | ns |
| Input Pulse Levels | 0.0 - 3.0 | V |
| Input timing measurement reference levels | 1.5 | V |
| Output timing measurement reference levels | 1.5 | V |

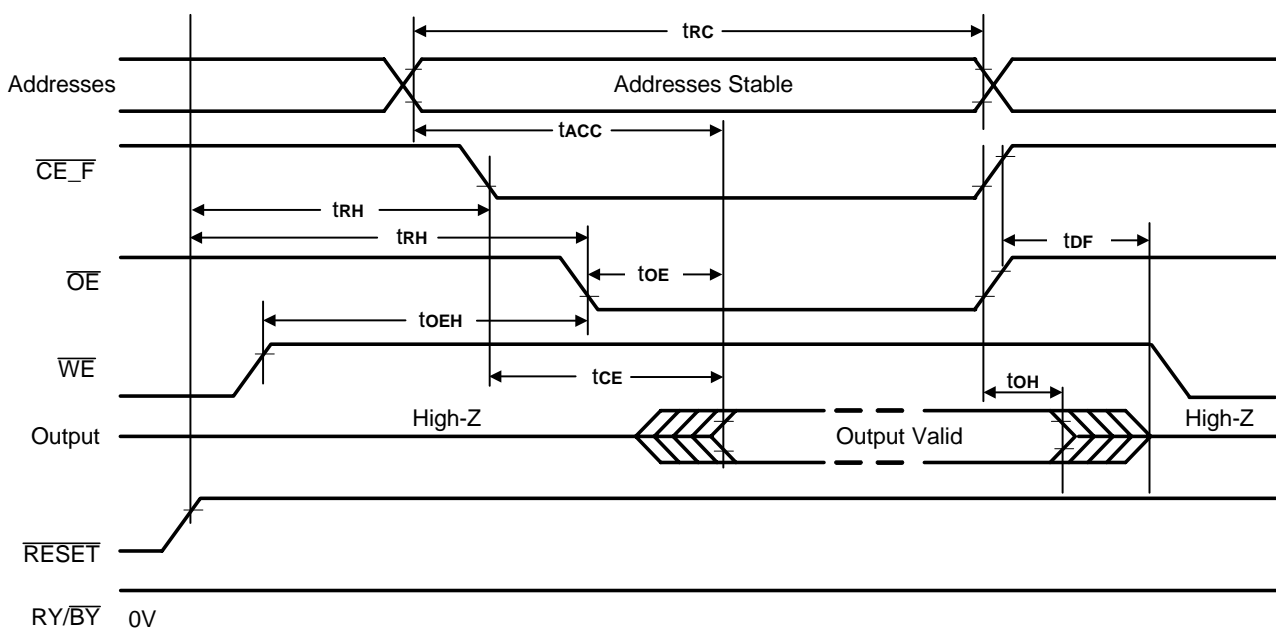
Figure 9. Test Setup

Figure 10. Input Waveforms and Measurement Levels


AC CHARACTERISTICS
Read Only Operations

| Parameter | | Description | Test Setup | | Speed | Unit |
|-----------|------|--|---|------|-------|------|
| JEDEC | Std | | | | -70 | |
| tAVAV | trc | Read Cycle Time (Note 1) | | Min. | 70 | ns |
| tAVQV | tACC | Address to Output Delay | $\overline{CE_F} = V_{IL}$ $\overline{OE} = V_{IL}$ | Max. | 70 | ns |
| tELQV | tCE | Chip Enable to Output Delay | $\overline{OE} = V_{IL}$ | Max. | 70 | ns |
| tGLQV | toE | Output Enable to Output Delay | | Max. | 30 | ns |
| tEHQZ | tdF | Chip Enable to Output High Z (Notes 1,3) | | Max. | 16 | ns |
| tGHQZ | tdF | Output Enable to Output High Z (Notes 1,3) | | Max. | 16 | ns |
| tAXQX | toH | Output Hold Time from Addresses, \overline{CE} or \overline{OE} , Whichever Occurs First | | Min. | 0 | ns |
| | toEH | Output Enable Hold Time (Note 1) | Read | Min. | 0 | ns |
| | | | Toggle and Data Polling | Min. | 10 | ns |

Notes:

1. Not 100% tested.
2. See Figure 9 and Table 14 for test specifications.
3. Measurements performed by placing a 50-ohm termination on the data pin with a bias of $(V_{CC_F})/2$. The time from \overline{OE} high to the data bus driven to $(V_{CC_F})/2$ is taken as t_{dF} .

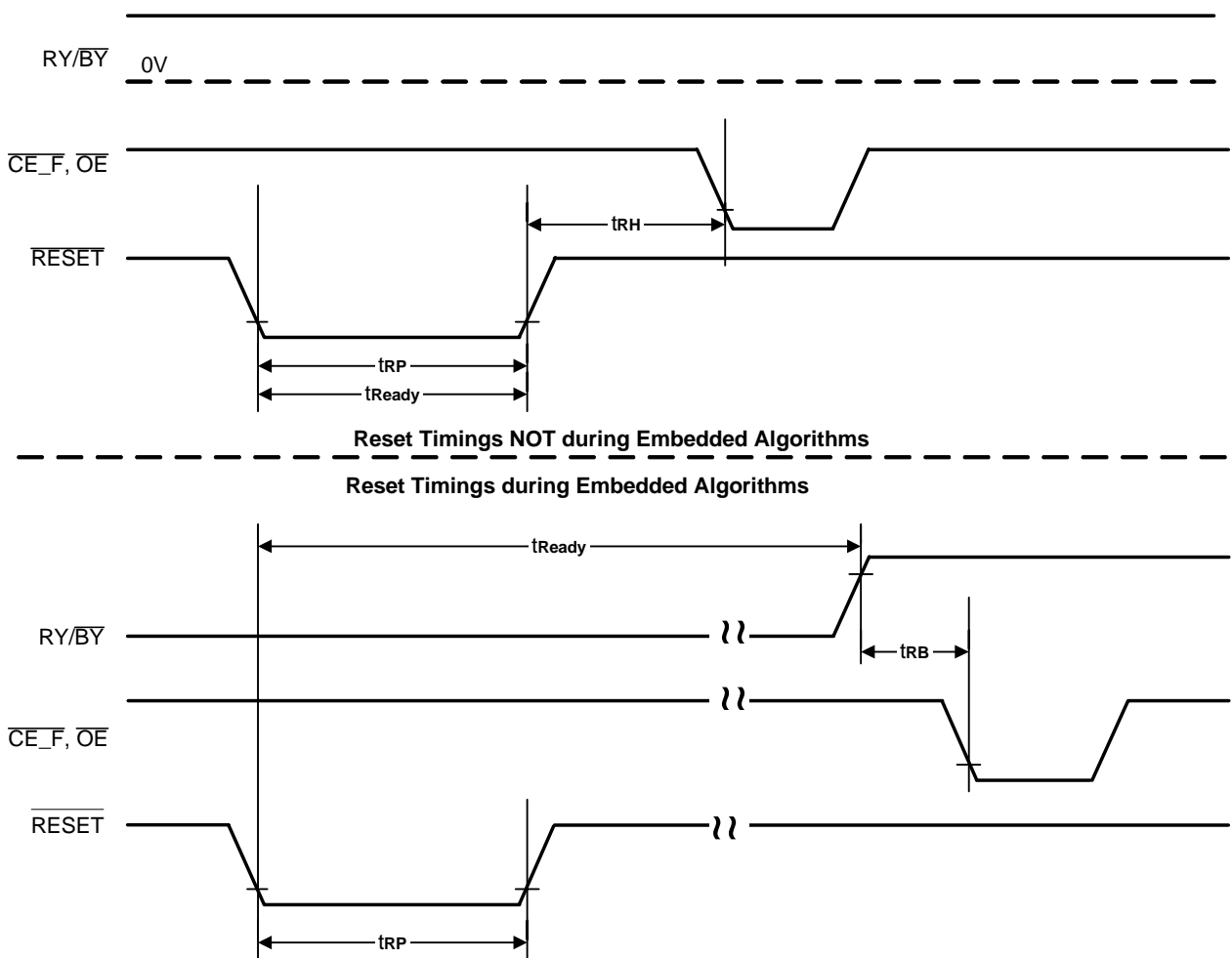
Figure 11. Read Operation Timings


AC CHARACTERISTICS
Hardware Reset ($\overline{\text{RESET}}$)

| Parameter | | Description | Test Setup | | All Speed Options | Unit |
|-----------|--------------------|--|------------|-----|-------------------|---------------|
| JEDEC | Std | | | | | |
| | t_{READY} | $\overline{\text{RESET}}$ Pin Low (During Embedded Algorithms) to Read or Write (See Note) | | Max | 20 | μs |
| | t_{READY} | $\overline{\text{RESET}}$ Pin Low (Not During Embedded Algorithms) to Read or Write (See Note) | | Max | 500 | ns |
| | t_{RP} | $\overline{\text{RESET}}$ Pulse Width | | Min | 500 | ns |
| | t_{RH} | $\overline{\text{RESET}}$ High Time Before Read (See Note) | | Min | 50 | ns |
| | t_{RB} | $\text{RY}/\overline{\text{BY}}$ Recovery Time | | Min | 0 | ns |
| | t_{RPD} | $\overline{\text{RESET}}$ Low to Standby Mode | | Min | 20 | μs |

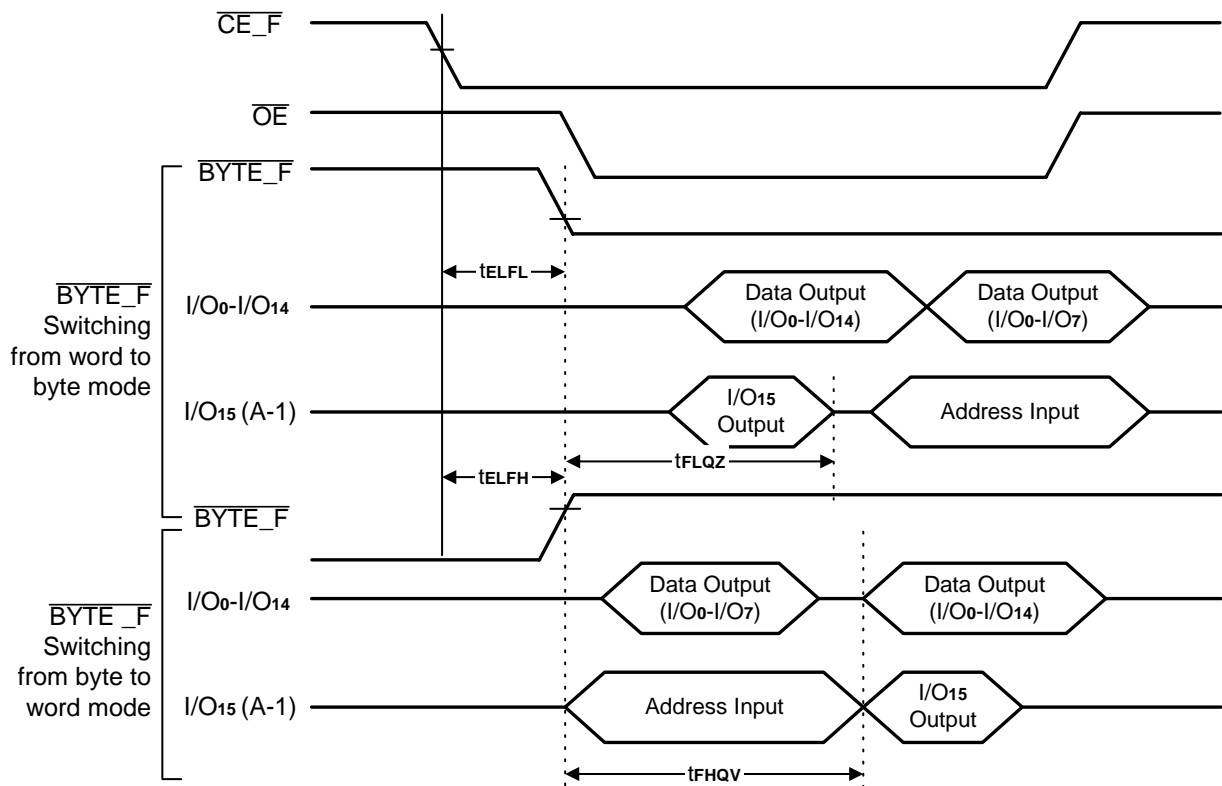
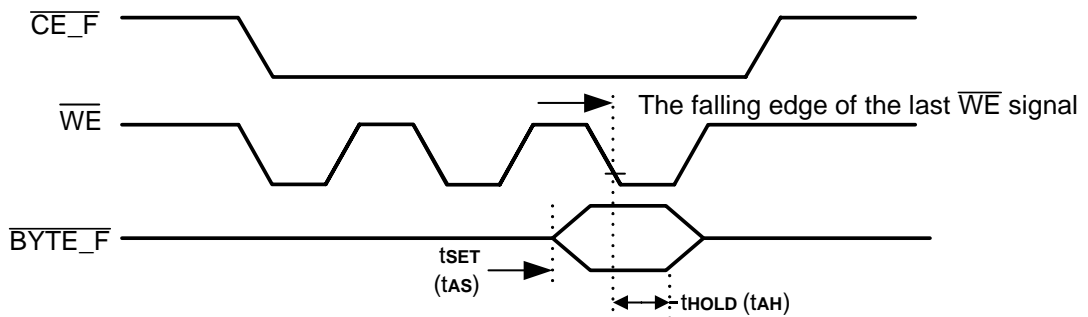
Note: Not 100% tested.

Figure 12. $\overline{\text{RESET}}$ Timings



AC CHARACTERISTICS
Word/Byte Configuration ($\overline{\text{BYTE_F}}$)

| Parameter | | Description | | Speed Option | Unit |
|-----------|-----------------------------------|--|-----|--------------|------|
| JEDEC | Std | | | -70 | |
| | $t_{\text{ELFL}}/t_{\text{ELFH}}$ | $\overline{\text{CE_F}}$ to $\overline{\text{BYTE_F}}$ Switching Low or High | Max | 5 | ns |
| | t_{FLQZ} | $\overline{\text{BYTE_F}}$ Switching Low to Output High-Z | Max | 25 | ns |
| | t_{HqV} | $\overline{\text{BYTE_F}}$ Switching High to Output Active | Min | 70 | ns |

Figure 13. $\overline{\text{BYTE_F}}$ Timings for Read Operations

Figure 14. $\overline{\text{BYTE_F}}$ Timings for Write Operations


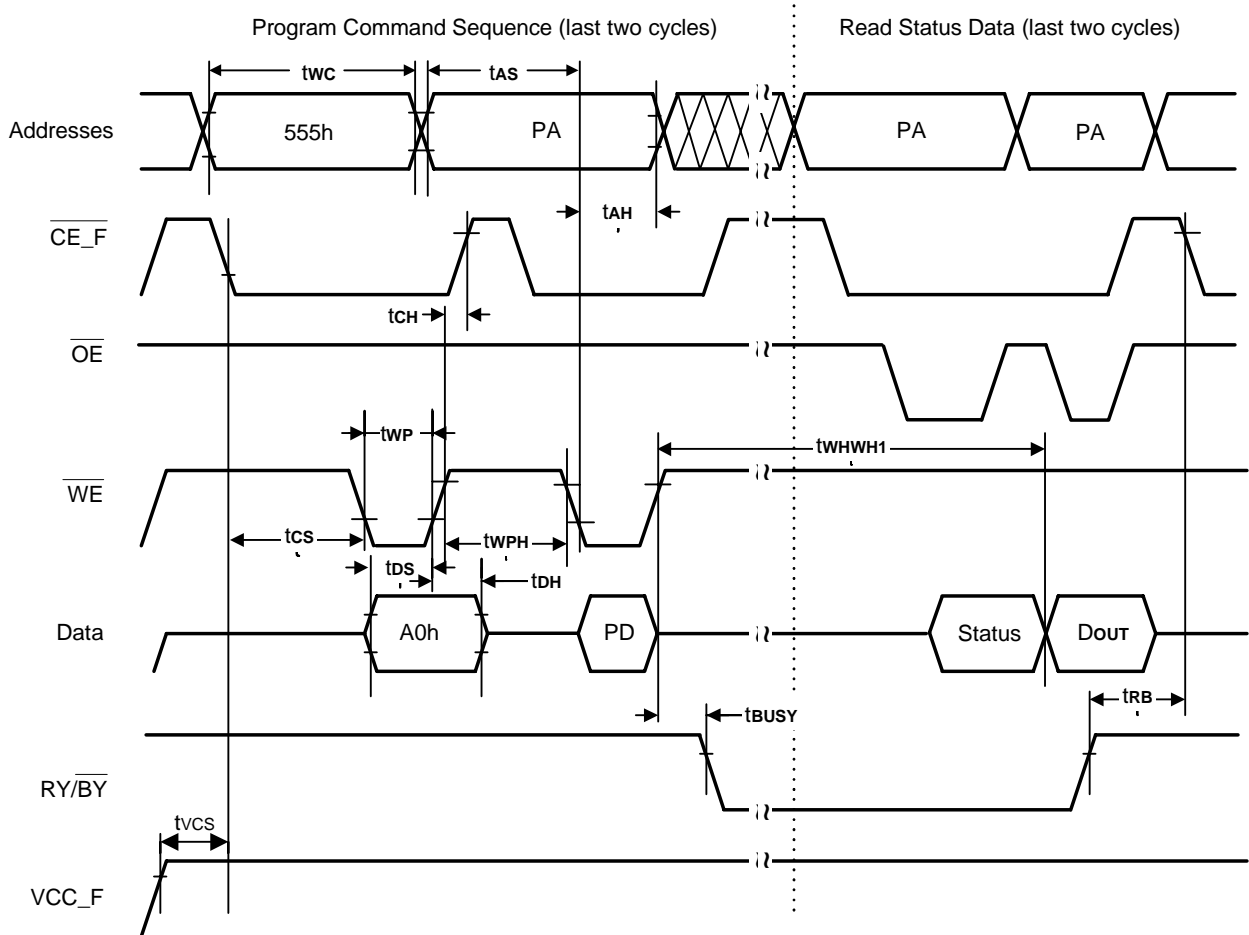
Note:
Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.

AC CHARACTERISTICS
Erase and Program Operations

| Parameter | | Description | | Speed | Unit | |
|-----------|--------|---|------|-------|---------|---------|
| JEDEC | Std | | | -70 | | |
| tAVAV | tWC | Write Cycle Time (Note 1) | Min. | 70 | ns | |
| tAVWL | tAS | Address Setup Time | Min. | 0 | ns | |
| | tASO | Address Setup Time to \overline{OE} low during toggle bit polling | | 15 | ns | |
| tWLAX | tAH | Address Hold Time | Min. | 45 | ns | |
| | tAHT | Address Hold Time From $\overline{CE_F}$ or \overline{OE} high during toggle bit polling | | 0 | ns | |
| tdVWH | tdS | Data Setup Time | Min. | 35 | ns | |
| tWHDX | tdH | Data Hold Time | Min. | 0 | ns | |
| | toEPH | Output Enable High during toggle bit polling | Min. | 20 | ns | |
| tGHWL | tGHWL | Read Recover Time Before Write (\overline{OE} high to \overline{WE} low) | Min. | 0 | ns | |
| tELWL | tCS | $\overline{CE_F}$ Setup Time | Min. | 0 | ns | |
| tWHEH | tCH | $\overline{CE_F}$ Hold Time | Min. | 0 | ns | |
| tWLWH | tWP | Write Pulse Width | Min. | 30 | ns | |
| tWHDL | tWPH | Write Pulse Width High | Min. | 30 | ns | |
| | tSR/W | Latency Between Read and Write Operations | Min. | 0 | | |
| tWHWH1 | tWHWH1 | Byte Programming Operation (Note 2) | Byte | Typ. | 5 | μ s |
| | | | Word | Typ. | 7 | |
| tWHWH1 | tWHWH1 | Accelerated Programming Operation, Word or Byte (Note 2) | Typ. | 4 | sec | |
| tWHWH2 | tWHWH2 | Sector Erase Operation (Note 2) | Typ. | 0.7 | sec | |
| | tVCS | VCC_F Set Up Time (Note 1) | Min. | 50 | μ s | |
| | tRB | Recovery Time from RY/ \overline{BY} | Min | 0 | ns | |
| | tBUSY | Program/Erase Valid to RY/ \overline{BY} Delay | Min | 90 | ns | |

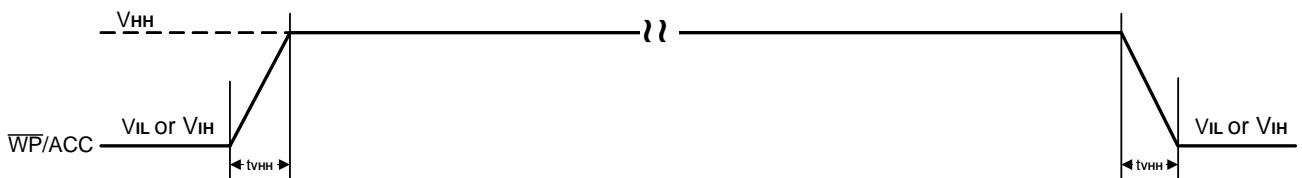
Notes:

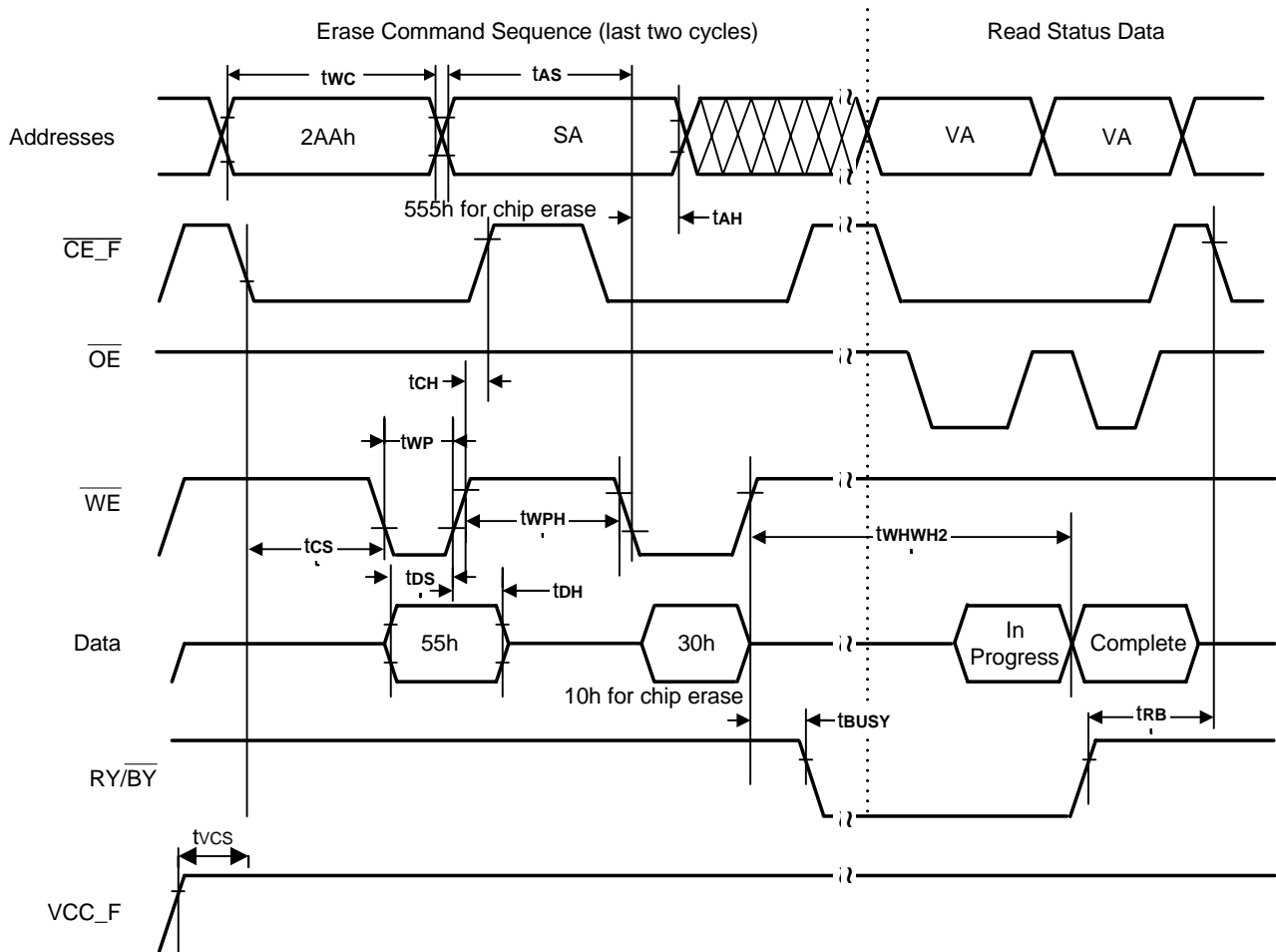
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

AC CHARACTERISTICS
Figure 15. Program Operation Timings


Note :

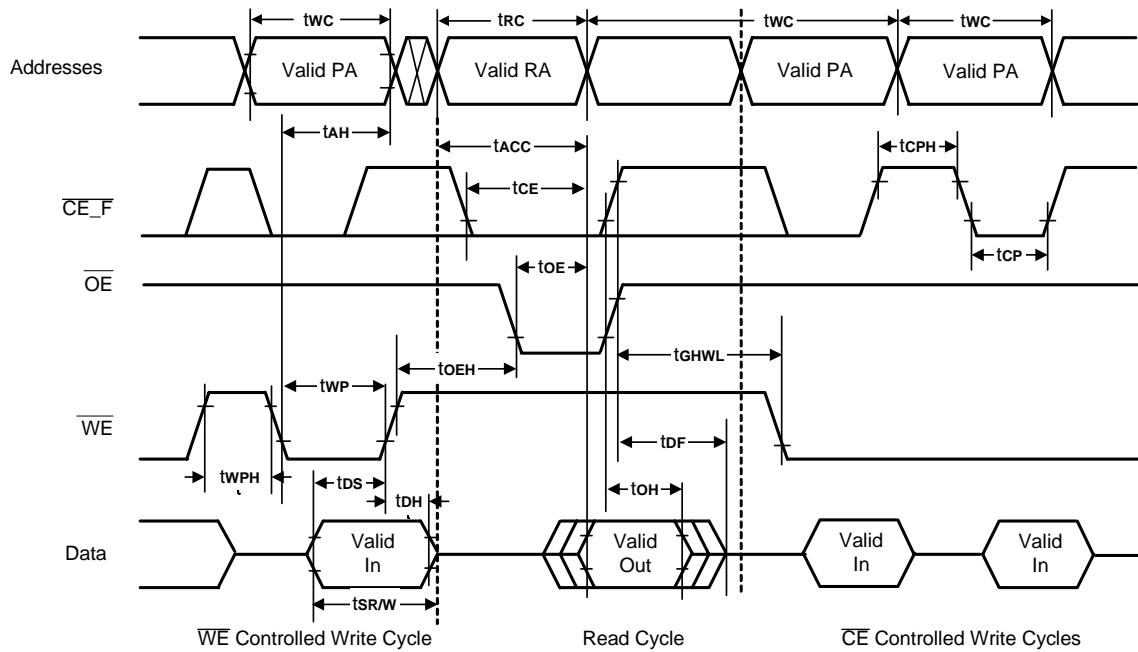
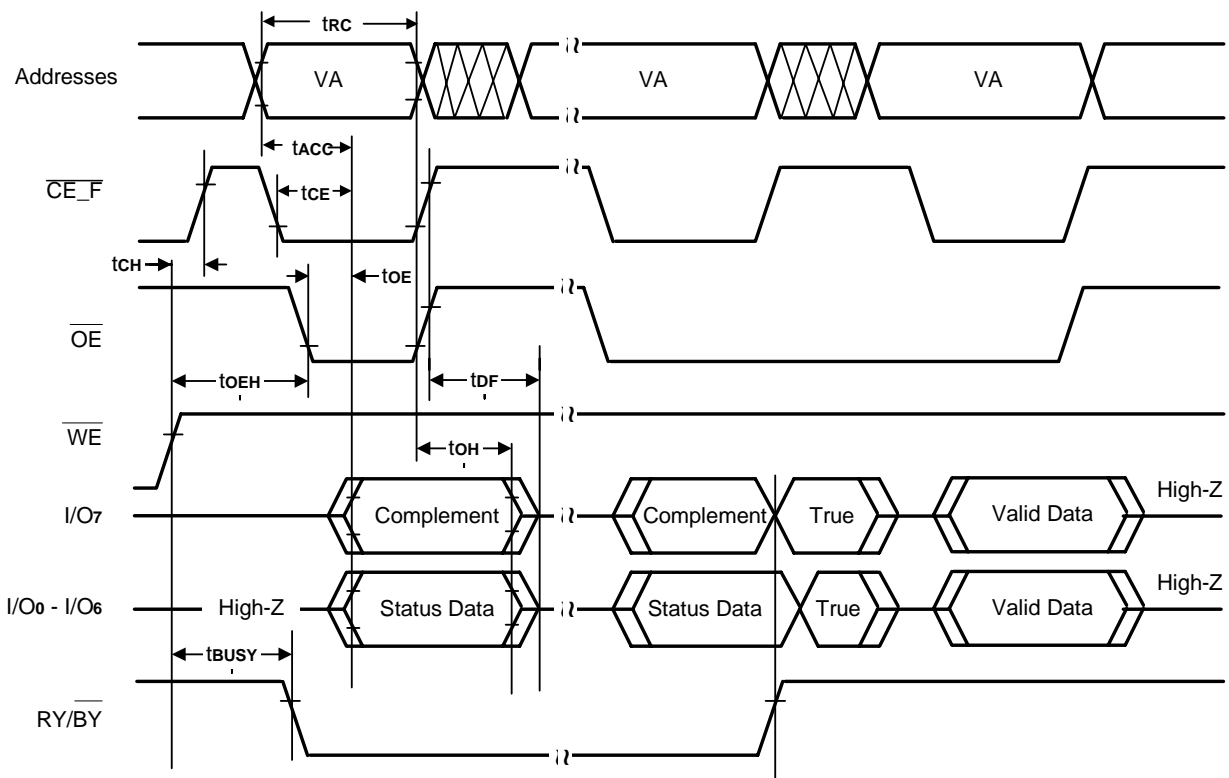
1. PA = program address, PD = program data, Dout is the true data at the program address.
2. Illustration shows device in word mode.

Figure 16. Accelerated Program Timing Diagram


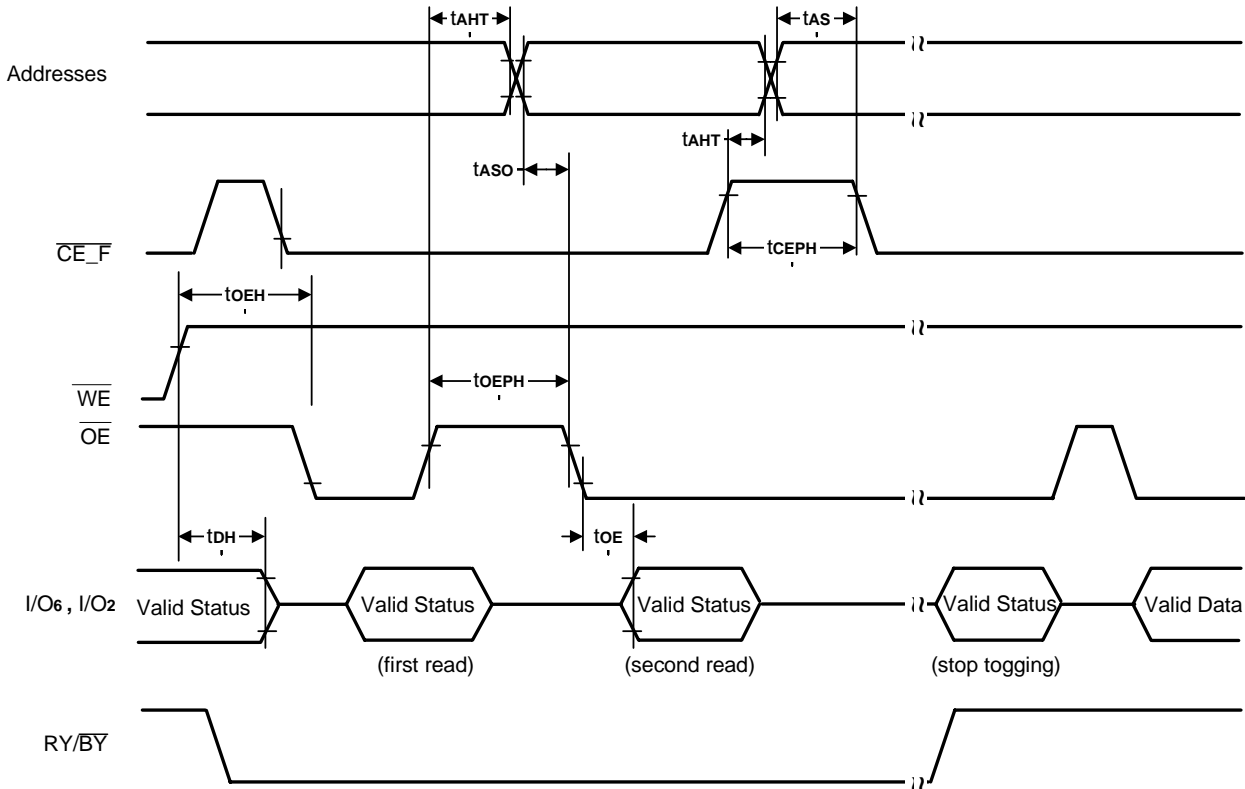
AC CHARACTERISTICS
Figure 17. Chip/Sector Erase Operation Timings


Note :

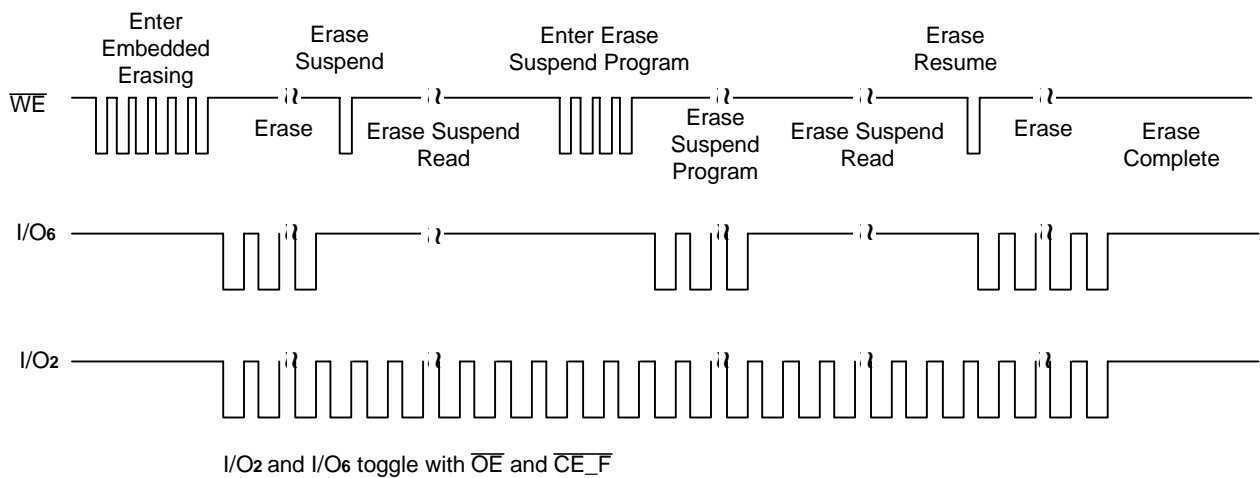
1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").
2. Illustration shows device in word mode.

AC CHARACTERISTICS
Figure 18. Back-to-back Read/Write Cycle Timings

Figure 19. Data Polling Timings (During Embedded Algorithms)


Note : VA = Valid Address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

AC CHARACTERISTICS
Figure 20. Toggle Bit Timings (During Embedded Algorithms)


Note: VA = Valid Address; not required for I/O₆. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 21. I/O₂ vs. I/O₆


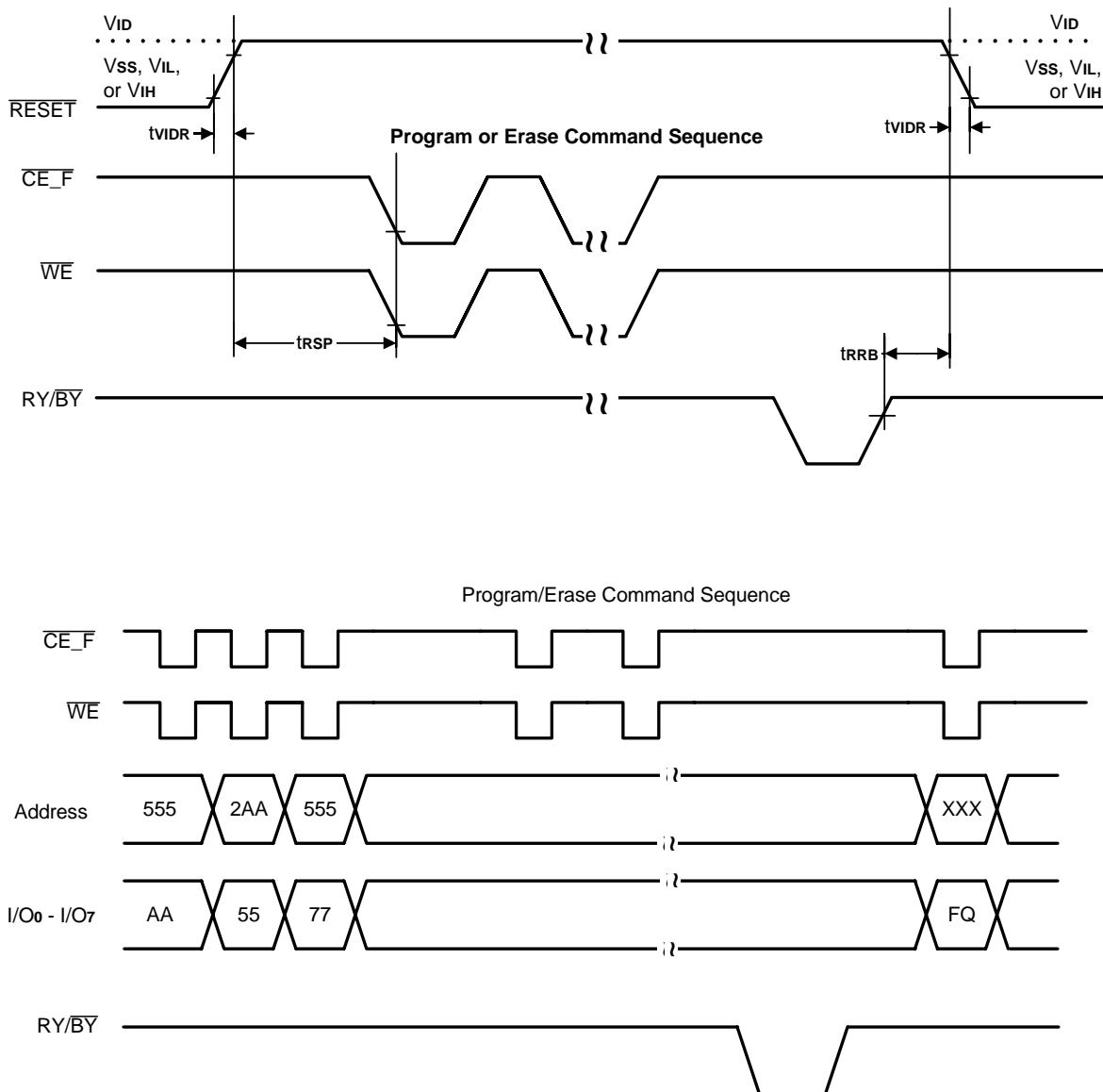
Note : Both I/O₆ and I/O₂ toggle with \overline{OE} or $\overline{CE_F}$. See the text on I/O₆ and I/O₂ in the section "Write Operation Status" for more information.

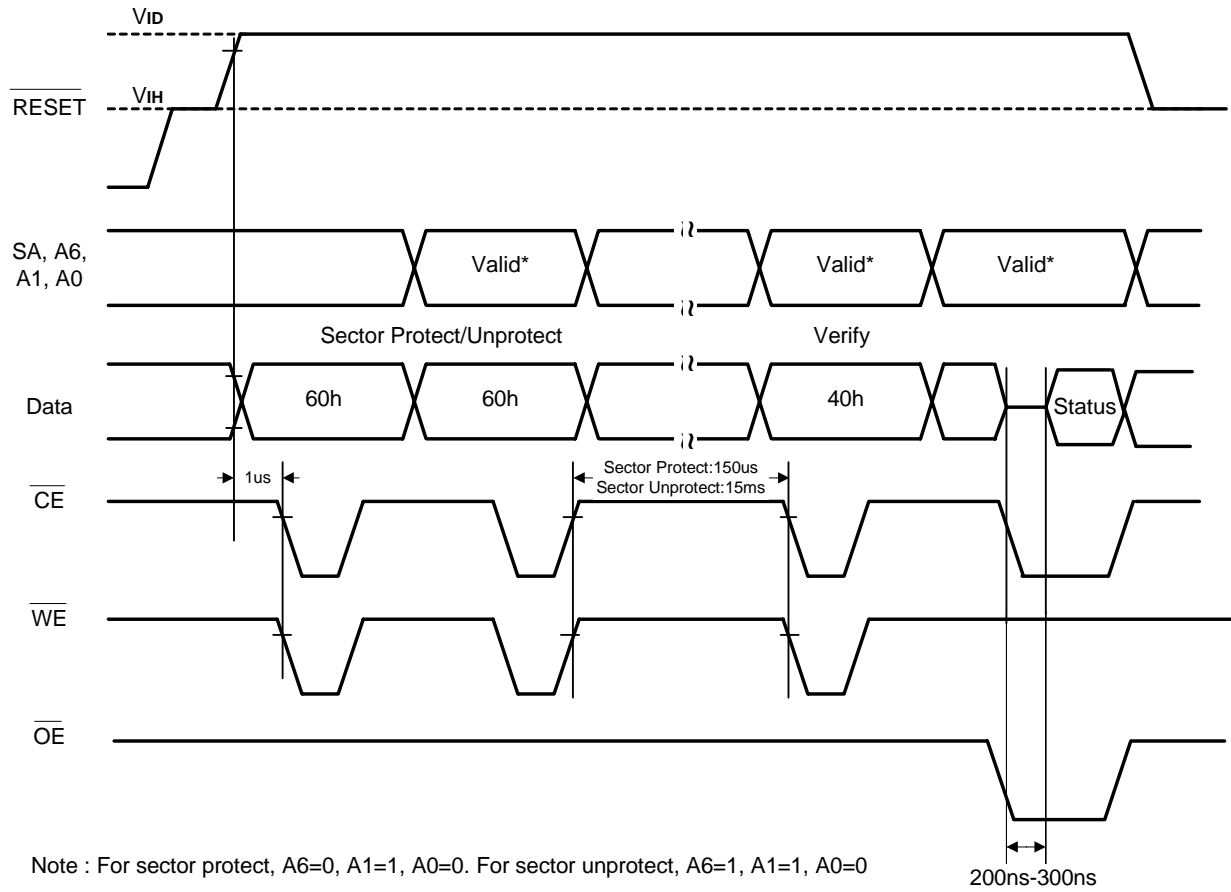
AC CHARACTERISTICS
Temporary Sector/Sector Block Unprotect

| Parameter | | Description | | All Speed Options | Unit |
|-----------|-------|---|-----|-------------------|------|
| JEDEC | Std | | | | |
| | tVIDR | V _{ID} Rise and Fall Time (See Note) | Min | 500 | ns |
| | tVHH | V _{HH} Rise and Fall Time (See Note) | Min | 250 | μs |
| | tRSP | RESET Setup Time for Temporary Sector/Sector Block Unprotect | Min | 4 | μs |
| | tRRB | RESET Hold Time from RY/BY High for Temporary Sector/Sector Block Unprotect | Min | 4 | μs |

Note: Not 100% tested.

Figure 22. Temporary Sector/Sector Block Unprotect Timing Diagram



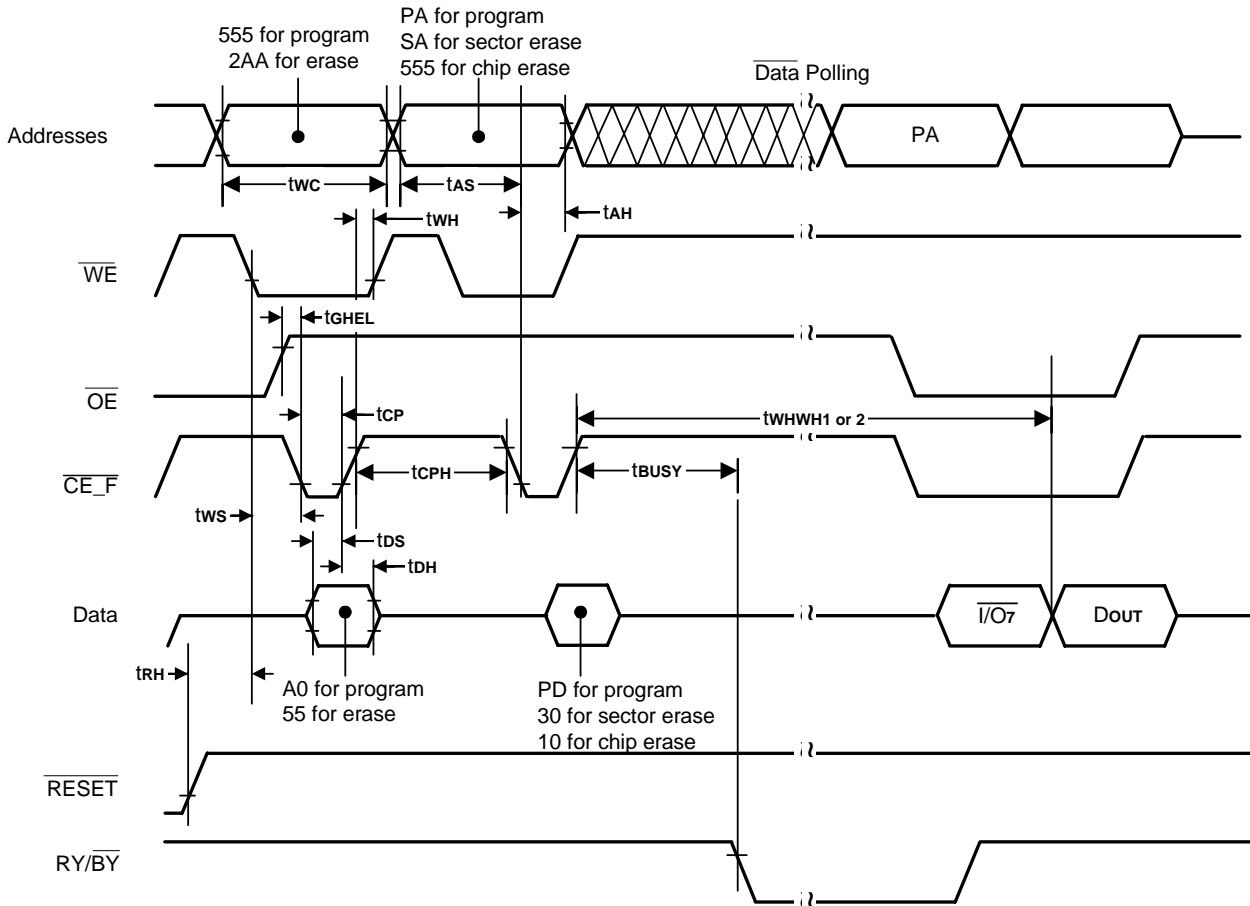
AC CHARACTERISTICS
Figure 23. Sector/Sector Block Protect and Unprotect Timing Diagram


AC CHARACTERISTICS
Alternate $\overline{CE_F}$ Controlled Erase and Program Operations

| Parameter | | Description | | Speed | Unit | |
|-----------|--------|--|------|-------|---------|---------|
| JEDEC | Std | | | -70 | | |
| tAVAV | tWC | Write Cycle Time (Note 1) | Min. | 70 | ns | |
| tAVEL | tAS | Address Setup Time | Min. | 0 | ns | |
| tELAX | tAH | Address Hold Time | Min. | 45 | ns | |
| tDVEH | tDS | Data Setup Time | Min. | 35 | ns | |
| tHDX | tDH | Data Hold Time | Min. | 0 | ns | |
| tGHEL | tGHEL | Read Recover Time Before Write (\overline{OE} High to \overline{WE} Low) | Min. | 0 | ns | |
| tWLEL | tWS | \overline{WE} Setup Time | Min. | 0 | ns | |
| tEWHH | tWH | \overline{WE} Hold Time | Min. | 0 | ns | |
| tELEH | tCP | $\overline{CE_F}$ Pulse Width | Min. | 30 | ns | |
| tEHEL | tCPH | $\overline{CE_F}$ Pulse Width High | Min. | 30 | ns | |
| tWHWH1 | tWHWH1 | Programming Operation (Note 2) | Byte | Typ. | 5 | μ s |
| | | | Word | Typ. | 7 | |
| tWHWH1 | tWHWH1 | Accelerated Programming Operation, Word or Byte (Note 2) | Typ. | 4 | μ s | |
| tWHWH2 | tWHWH2 | Sector Erase Operation (Note 2) | Typ. | 0.7 | sec | |

Notes:

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

AC CHARACTERISTICS
Figure 24. Alternate $\overline{\text{CE}}_F$ Controlled Write (Erase/Program) Operation Timings

Notes:

1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data.
3. $\overline{\text{I/O}}_7$ is the complement of the data written to the device. DOUT is the data written to the device.
4. Waveforms are for the word mode.

SRAM
DC Electrical Characteristics ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC_S} = 2.7\text{V}$ to 3.6V , $\text{GND} = 0\text{V}$)

| Symbol | Parameter | - 70 ns | | Unit | Conditions |
|--------------|------------------------------|---------|------|---------------|---|
| | | Min. | Max. | | |
| $ I_{LI} $ | Input Leakage Current | - | 1 | μA | $V_{IN} = \text{GND to } V_{CC_S}$ |
| $ I_{LO} $ | Output Leakage Current | - | 1 | μA | $\overline{\text{CE1_S}} = V_{IH}$ or $\text{CE2_S} = V_{IL}$ or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$ $V_{I/O} = \text{GND to } V_{CC}$ |
| I_{CC_S} | Active Power Supply Current | - | 3 | mA | $\overline{\text{CE1_S}} = V_{IL}$, $\text{CE2_S} = V_{IH}$ $I_{I/O} = 0\text{mA}$ |
| I_{CC1_S} | Dynamic Operating Current | - | 30 | mA | Min. Cycle, Duty = 100% $\overline{\text{CE1_S}} = V_{IL}$, $\text{CE2_S} = V_{IH}$ $I_{I/O} = 0\text{mA}$ |
| I_{CC2_S} | | - | 3 | mA | $\overline{\text{CE1_S}} = V_{IL}$, $\text{CE2_S} = V_{IH}$ $V_{IH} = V_{CC_S}$, $V_{IL} = 0\text{V}$ $f = 1\text{ MHz}$, $I_{I/O} = 0\text{mA}$ |
| I_{SB_S} | Standby Power Supply Current | - | 0.5 | mA | $V_{CC_S} \leq 3.3\text{V}$, $\overline{\text{CE1_S}} = V_{IH}$ or $\text{CE2_S} = V_{IL}$ |
| I_{SB1_S} | | - | 5 | μA | $V_{CC} \leq 3.3\text{V}$, $\overline{\text{CE1_S}} \geq V_{CC} - 0.2\text{V}$ or $\text{CE2_S} \leq 0.2\text{V}$, $V_{IN} \geq 0\text{V}$ |
| V_{OL} | Output Low Voltage | - | 0.4 | V | $I_{OL} = 2.1\text{mA}$ |
| V_{OH} | Output High Voltage | 2.2 | - | V | $I_{OH} = -1.0\text{mA}$ |

Truth Table

| Mode | $\overline{\text{CE1_S}}$ | CE2_S | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | I/O Operation | Supply Current |
|----------------|----------------------------|-----------------|------------------------|------------------------|------------------|----------------------------------|
| Standby | H | X | X | X | High Z | I_{SB} , I_{SB1} |
| | X | L | X | X | High Z | I_{SB} , I_{SB1} |
| Output Disable | L | H | H | H | High Z | I_{CC} , I_{CC1} , I_{CC2} |
| Read | L | H | L | H | D _{OUT} | I_{CC} , I_{CC1} , I_{CC2} |
| Write | L | H | X | L | D _{IN} | I_{CC} , I_{CC1} , I_{CC2} |

Note: X = H or L

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

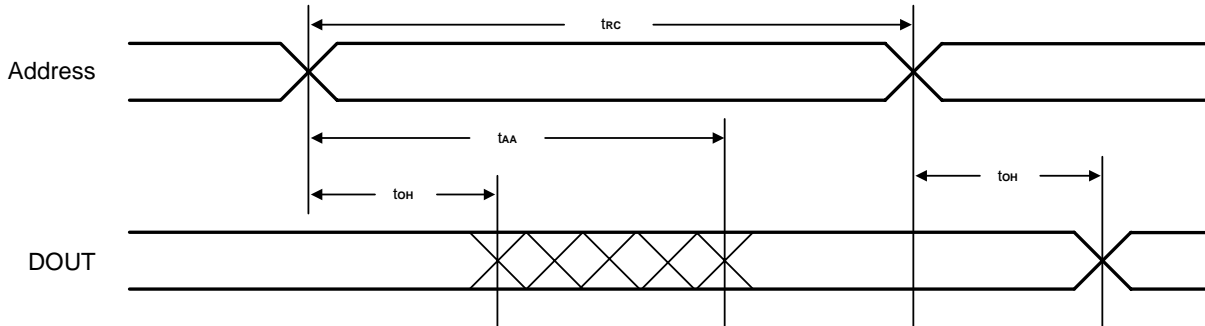
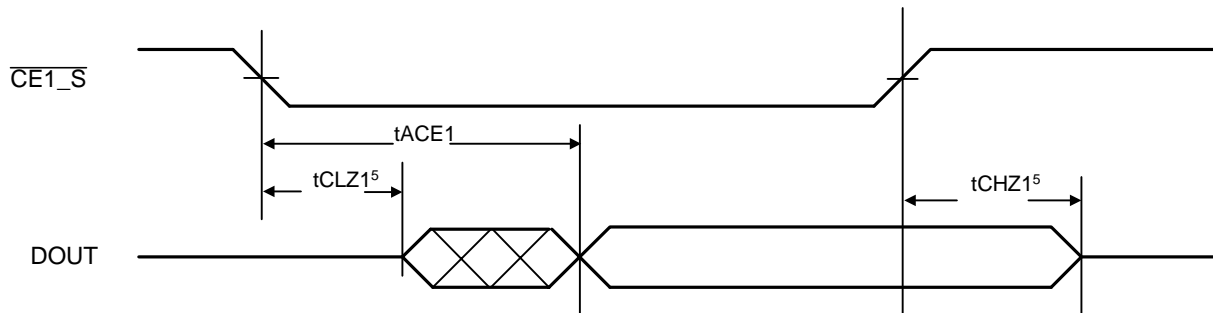
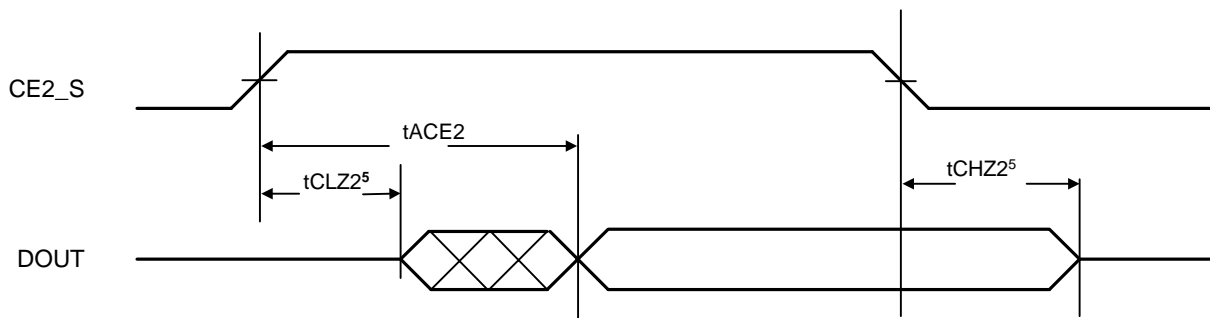
| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|------------|--------------------------|------|------|------|---------------|
| C_{IN}^* | Input Capacitance | | 6 | pF | $V_{IN} = 0V$ |
| C_{IO}^* | Input/Output Capacitance | | 8 | pF | $V_{IO} = 0V$ |

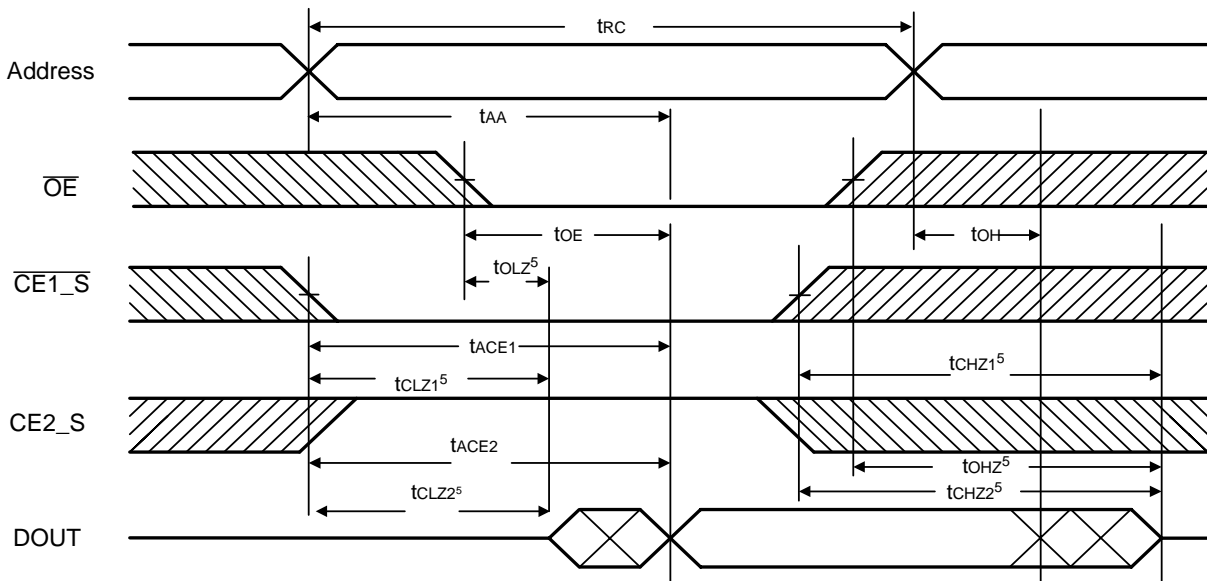
* These parameters are sampled and not 100% tested.

AC Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC_S} = 2.7\text{V}$ to 3.6V)

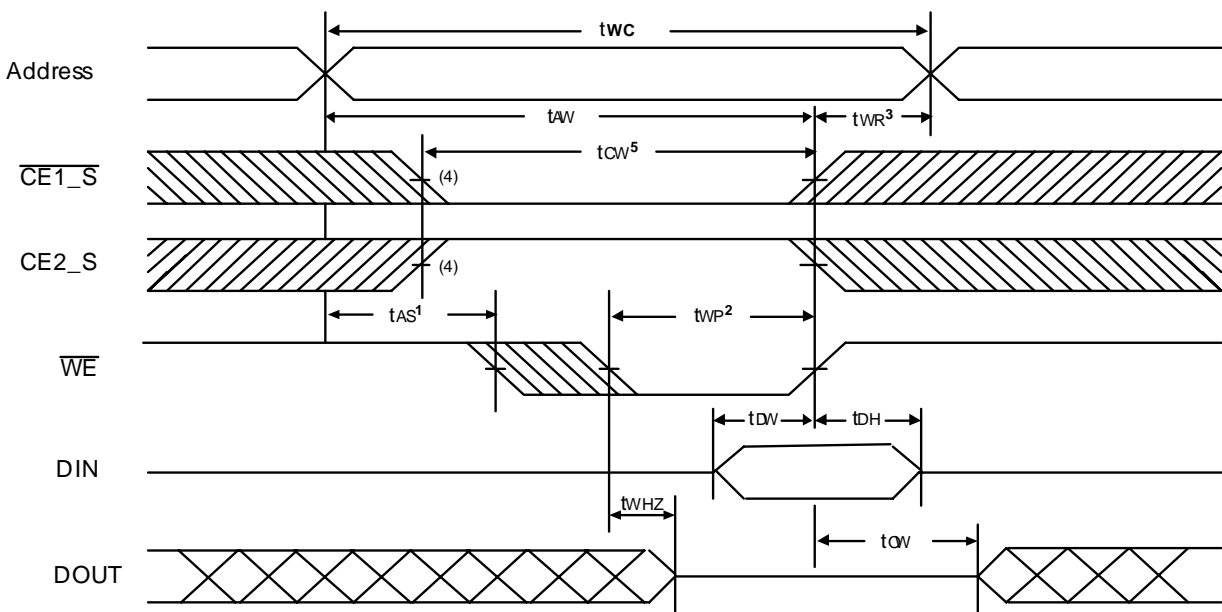
| Symbol | Parameter | -70 ns | | Unit | |
|-------------------|------------------------------------|----------------------------|------|------|----|
| | | Min. | Max. | | |
| Read Cycle | | | | | |
| t _{RC} | Read Cycle Time | 70 | - | ns | |
| t _{AA} | Address Access Time | - | 70 | ns | |
| t _{ACE1} | Chip Enable Access Time | $\overline{\text{CE1_S}}$ | - | 70 | ns |
| t _{ACE2} | | CE2_S | - | 70 | ns |
| t _{OE} | Output Enable to Output Valid | - | 35 | ns | |
| t _{CLZ1} | Chip Enable to Output in Low Z | $\overline{\text{CE1_S}}$ | 10 | - | ns |
| t _{CLZ2} | | CE2_S | 10 | - | ns |
| t _{OLZ} | Output Enable to Output in Low Z | 5 | - | ns | |
| t _{CHZ1} | Chip Disable to Output in High Z | $\overline{\text{CE1_S}}$ | 0 | 25 | ns |
| t _{CHZ2} | | CE2_S | 0 | 25 | ns |
| t _{OHZ} | Output Disable to Output in High Z | 0 | 25 | ns | |
| t _{OH} | Output Hold from Address Change | 10 | - | ns | |
| Write Cycle | | | | | |
| t _{WC} | Write Cycle Time | 70 | - | ns | |
| t _{CW} | Chip Enable to End of Write | 60 | - | ns | |
| t _{AS} | Address Setup Time | 0 | - | ns | |
| t _{AW} | Address Valid to End of Write | 60 | - | ns | |
| t _{WP} | Write Pulse Width | 50 | - | ns | |
| t _{WR} | Write Recovery Time | 0 | - | ns | |
| t _{WHZ} | Write to Output in High Z | 0 | 25 | ns | |
| t _{DW} | Data to Write Time Overlap | 30 | - | ns | |
| t _{DH} | Data Hold from Write Time | 0 | - | ns | |
| t _{OW} | Output Active from End of Write | 5 | - | ns | |

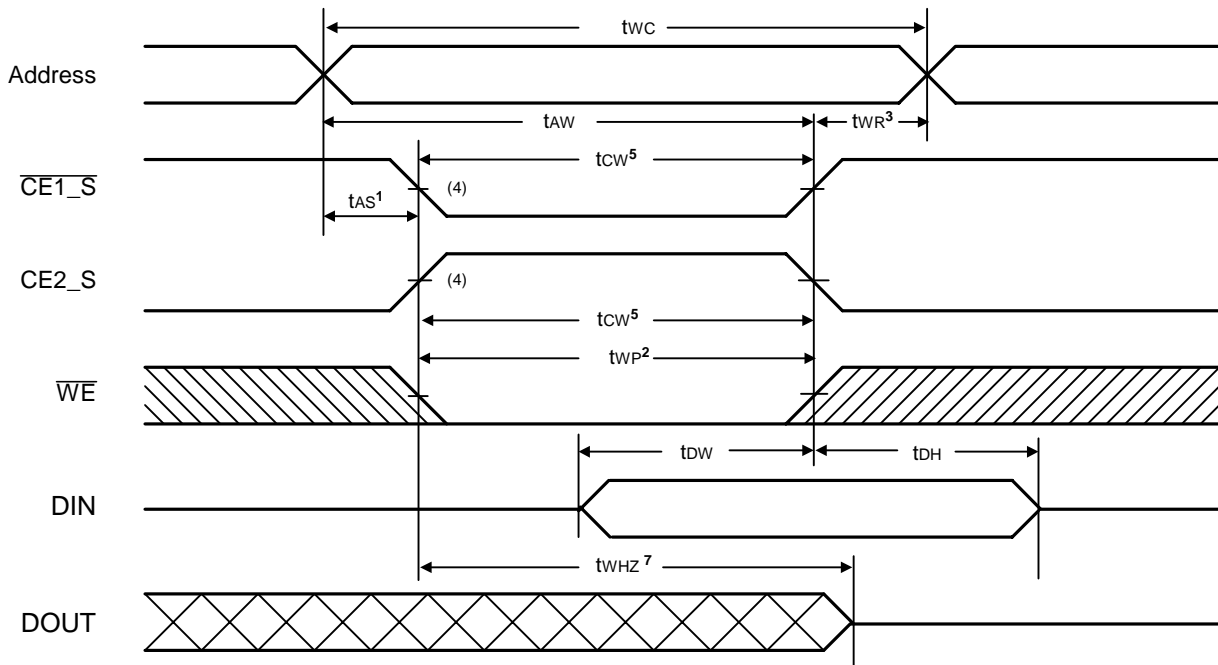
Notes: t_{CHZ1}, t_{CHZ2}, t_{OHZ}, and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms
Read Cycle 1^(1, 2, 4)

Read Cycle 2^(1, 3, 4, 6)

Read Cycle 3^(1, 4, 7, 8)


Timing Waveforms (continued)
Read Cycle 4 ⁽¹⁾


- Notes:
1. \overline{WE} is high for Read Cycle.
 2. Device is continuously enabled $\overline{CE1_S} = V_{IL}$ and $CE2_S = V_{IH}$.
 3. Address valid prior to or coincident with $\overline{CE1_S}$ transition low.
 4. $\overline{OE} = V_{IL}$.
 5. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.
 6. $CE2_S$ is high.
 7. $CE1_S$ is low.
 8. Address valid prior to or coincident with $CE2_S$ transition high.

Write Cycle 1 ⁽⁶⁾
(Write Enable Controlled)


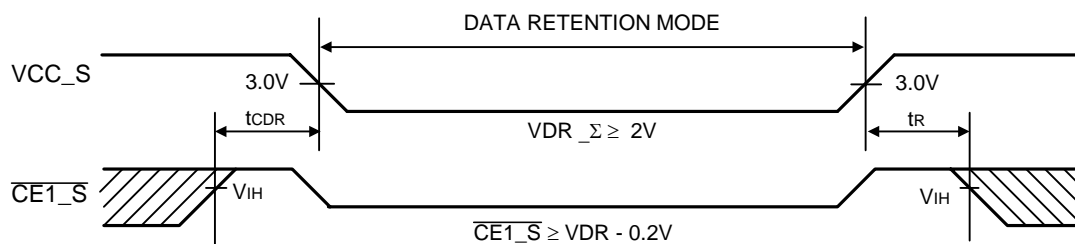
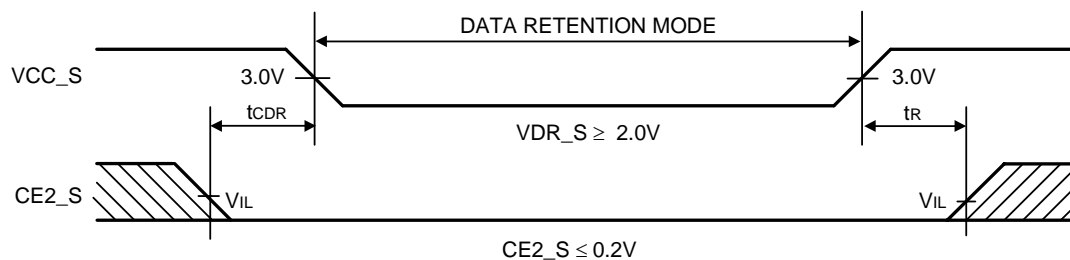
Timing Waveforms (continued)
**Write Cycle 2
(Chip Enable Controlled)**


- Notes:
1. t_{AS1} is measured from the address valid to the beginning of Write.
 2. A Write occurs during the overlap (t_{WP}^2) of a low $\overline{CE1_S}$, a high $CE2_S$ and a low \overline{WE} .
 3. t_{WR}^3 is measured from the earliest of $\overline{CE1_S}$ or \overline{WE} going high or $CE2_S$ going low to the end of the Write cycle.
 4. If the $\overline{CE1_S}$ low transition or the $CE2_S$ high transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, outputs remain in a high impedance state.
 5. t_{CW}^5 is measured from the later of $\overline{CE1_S}$ going low or $CE2_S$ going high to the end of Write.
 6. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
 7. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

SRAM
Data Retention Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|----------------|-------------------------------------|------|------|---------------|---|
| V_{DR1} | VCC for Data Retention | 2.0 | 3.6 | V | $\overline{CE1_S} \geq V_{CC} - 0.2V$ |
| V_{DR2} | | 2.0 | 3.6 | V | $CE2_S \leq 0.2V$, |
| I_{CCDR1_S} | Data Retention Current | - | 1* | μA | $V_{CC_S} = 2V$, $\overline{CE1_S} \geq V_{CC_S} - 0.2V$, $V_{IN} \geq 0V$ |
| I_{CCDR2_S} | | - | 1* | μA | $V_{CC_S} = 2V$, $CE2_S \leq 0.2V$, $V_{IN} \geq 0V$ |
| t_{CDR} | Chip Disable to Data Retention Time | 0 | - | ns | See Retention Waveform |
| t_R | Operation Recovery Time | 5 | - | ms | |

* I_{CCDR_S} : max. $1\mu\text{A}$ at $T_A = 0^{\circ}\text{C}$ to $+40^{\circ}\text{C}$

Low VCC_S Data Retention Waveform (1) ($\overline{CE1_S}$ Controlled)

Low VCC Data Retention Waveform (2) ($CE2_S$ Controlled)


ERASE AND PROGRAMMING PERFORMANCE

| Parameter | | Typ. (Note 1) | Max. (Note 2) | Unit | Comments |
|--|-----------|---------------|---------------|------|--|
| Sector Erase Time | | 0.7 | 15 | sec | Excludes 00h programming prior to erasure (Note 4) |
| Chip Erase Time | | 27 | | sec | |
| Byte Programming Time | | 5 | 150 | μs | Excludes system-level overhead (Note 5) |
| Word Programming Time | | 7 | 210 | μs | |
| Accelerated Word/Byte Programming Time | | 4 | 120 | μs | |
| Chip Programming Time (Note 3) | Byte Mode | 9 | 27 | sec | |
| | Word Mode | 6 | 18 | sec | |

Notes:

1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC_F, 10,000 cycles. Additionally, programming typically assumes checkerboard pattern.
2. Under worst case conditions of 90°C, VCC_F = 2.7V, 100,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum byte program time listed.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the four-bus-cycle command sequence for programming. See Table 12 for further information on command definitions.
6. The device has a minimum erase and program cycle endurance of 10,000 cycles.

FLASH LATCH-UP CHARACTERISTICS

| Description | Min. | Max. |
|--|---------|------------|
| Input Voltage with respect to VSS on all I/O pins | -1.0V | VCC_F+1.0V |
| VCC_F Current | -100 mA | +100 mA |
| Input voltage with respect to VSS on all pins except I/O pins (including A9, \overline{OE} and \overline{RESET}) | -1.0V | 12.5V |

Includes all pins except VCC_F. Test conditions: VCC_F = 3.0V, one pin at time.

DATA RETENTION

| Parameter | Test Conditions | Min | Unit |
|-------------------------------------|-----------------|-----|-------|
| Minimum Pattern Data Retention Time | 150°C | 10 | Years |
| | 125°C | 20 | Years |

Ordering Information
Top Boot Sector Flash & SRAM

| Part No. | Access Time (ns) | Bank 1 | Bank 2 | Package |
|------------------|------------------|--------|--------|-----------------------|
| A82DL3224TG-70 | 70 | 4M | 28M | 69-ball TFBGA |
| A82DL3224TG-70F | | | | 69-ball Pb-Free TFBGA |
| A82DL3224TG-70I | | | | 69-ball TFBGA |
| A82DL3224TG-70IF | | | | 69-ball Pb-Free TFBGA |
| A82DL3224TG-70U | | | | 69-ball TFBGA |
| A82DL3224TG-70UF | | | | 69-ball Pb-Free TFBGA |
| A82DL3234TG-70 | 70 | 8M | 24M | 69-ball TFBGA |
| A82DL3234TG-70F | | | | 69-ball Pb-Free TFBGA |
| A82DL3234TG-70I | | | | 69-ball TFBGA |
| A82DL3234TG-70IF | | | | 69-ball Pb-Free TFBGA |
| A82DL3234TG-70U | | | | 69-ball TFBGA |
| A82DL3234TG-70UF | | | | 69-ball Pb-Free TFBGA |
| A82DL3244TG-70 | 70 | 16M | 16M | 69-ball TFBGA |
| A82DL3244TG-70F | | | | 69-ball Pb-Free TFBGA |
| A82DL3244TG-70I | | | | 69-ball TFBGA |
| A82DL3244TG-70IF | | | | 69-ball Pb-Free TFBGA |
| A82DL3244TG-70U | | | | 69-ball TFBGA |
| A82DL3244TG-70UF | | | | 69-ball Pb-Free TFBGA |

Note: Industrial operating temperature range: -40°C to 85°C for -U; -25°C to 85°C for -I

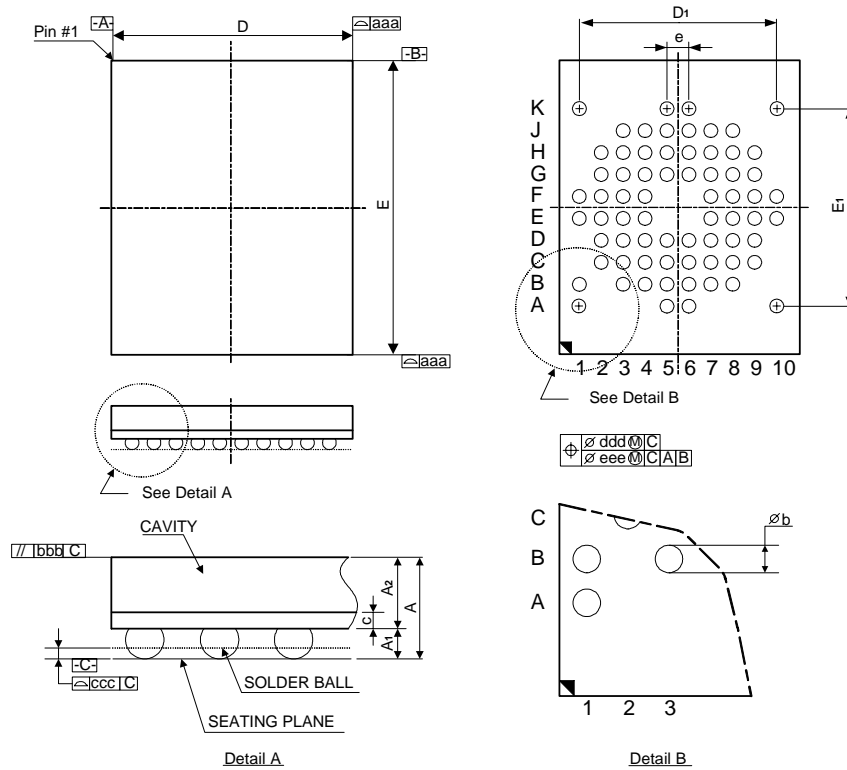
Bottom Boot Sector Flash & SRAM

| Part No. | Access Time (ns) | Bank 1 | Bank 2 | Package |
|------------------|------------------|--------|--------|-----------------------|
| A82DL3224UG-70 | 70 | 4M | 28M | 69-ball TFBGA |
| A82DL3224UG-70F | | | | 69-ball Pb-Free TFBGA |
| A82DL3224UG-70I | | | | 69-ball TFBGA |
| A82DL3224UG-70IF | | | | 69-ball Pb-Free TFBGA |
| A82DL3224UG-70U | | | | 69-ball TFBGA |
| A82DL3224UG-70UF | | | | 69-ball Pb-Free TFBGA |
| A82DL3234UG-70 | 70 | 8M | 24M | 69-ball TFBGA |
| A82DL3234UG-70F | | | | 69-ball Pb-Free TFBGA |
| A82DL3234UG-70I | | | | 69-ball TFBGA |
| A82DL3234UG-70IF | | | | 69-ball Pb-Free TFBGA |
| A82DL3234UG-70U | | | | 69-ball TFBGA |
| A82DL3234UG-70UF | | | | 69-ball Pb-Free TFBGA |
| A82DL3244UG-70 | 70 | 16M | 16M | 69-ball TFBGA |
| A82DL3244UG-70F | | | | 69-ball Pb-Free TFBGA |
| A82DL3244UG-70I | | | | 69-ball TFBGA |
| A82DL3244UG-70IF | | | | 69-ball Pb-Free TFBGA |
| A82DL3244UG-70U | | | | 69-ball TFBGA |
| A82DL3244UG-70UF | | | | 69-ball Pb-Free TFBGA |

Note: Industrial operating temperature range: -40°C to 85°C for -U; -25°C to 85°C for -I

Package Information
69LD STF BGA (8 x 11mm) Outline Dimensions

unit: mm



| Symbol | Dimensions in mm | | | Dimensions in inches | | |
|--------|------------------|-------|-------|----------------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 1.40 | - | - | 0.055 |
| A1 | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| A2 | 0.91 | 0.96 | 1.01 | 0.036 | 0.038 | 0.040 |
| c | 0.22 | 0.26 | 0.30 | 0.009 | 0.010 | 0.012 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| E | 10.90 | 11.00 | 11.10 | 0.429 | 0.433 | 0.437 |
| D1 | - | 7.20 | - | - | 0.283 | - |
| E1 | - | 7.20 | - | - | 0.283 | - |
| e | - | 0.80 | - | - | 0.031 | - |
| b | 0.35 | 0.40 | 0.45 | 0.14 | 0.16 | 0.18 |
| aaa | 0.15 | | | 0.006 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.12 | | | 0.005 | | |
| ddd | 0.15 | | | 0.006 | | |
| eee | 0.08 | | | 0.003 | | |
| MD/ME | 10/10 | | | 10/10 | | |

Notes:

1. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. REFERENCE DOCUMENT: JEDEC MO-219
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.