

## Section 15. Electrical Specifications

### 15.1 Absolute Maximum Ratings

Table 15-1 lists the absolute maximum ratings.

**Table 15-1. Absolute Maximum Ratings**

Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Programming voltage	V <sub>PP</sub>	-0.3 to +14.0	V
Input voltage	V <sub>in</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
Operating temperature	T <sub>opr</sub>	Regular specifications: -20 to +75	°C
		Wide-range specifications: -40 to +85	°C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

**Note:** The input pins have protection circuits that guard against high static voltages and electric fields, but these high input-impedance circuits should never receive overvoltages exceeding the absolute maximum ratings shown in table 15-1.

### 15.2 Electrical Characteristics

#### 15.2.1 DC Characteristics

Table 15-2 lists the DC characteristics of the H8/320 series.

**Table 15-2. DC Characteristics**Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = -20$  to  $75^\circ C$  (regular specifications) $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Item		Symbol				Unit	Measurement
			min	typ	max		conditions
Schmitt trigger input voltage (1)	P66 – P63, P60,	$V_{T^-}$	1.0	–	–	V	
	P70	$V_{T^+}$	–	–	$V_{CC} \times 0.7$	V	
		$V_{T^+} - V_{T^-}$	0.4	–	–	V	
Input high voltage (2)	$\overline{RES}$ , $\overline{STBY}$	$V_{IH}$	$V_{CC} - 0.7$	–	$V_{CC} + 0.3$	V	
	MD1, MD0 EXTAL, $\overline{NMI}$						
Input high voltage	Input pins other than (1) and (2)	$V_{IH}$	2.0	–	$V_{CC} + 0.3$	V	
Input low voltage (3)	$\overline{RES}$ , $\overline{STBY}$	$V_{IL}$	–0.3	–	0.5	V	
	MD1, MD0, EXTAL						
Input low voltage	Input pins other than (1) and (3)	$V_{IL}$	–0.3	–	0.8	V	
Output high voltage	All output pins	$V_{OH}$	$V_{CC} - 0.5$	–	–	V	$I_{OH} = -200 \mu A$
			3.5	–	–	V	$I_{OH} = -1.0 mA$
Output low voltage	All output pins P17 – P10, P27 – P20	$V_{OL}$	–	–	0.4	V	$I_{OL} = 1.6 mA$
			–	–	1.0	V	$I_{OL} = 10.0 mA$
Input leakage current	$\overline{RES}$	$ I_{in} $	–	–	10.0	$\mu A$	$V_{in} = 0.5 V$ to
	$\overline{STBY}$ , $\overline{NMI}$ , MD1, MD0		–	–	1.0	$\mu A$	$V_{CC} - 0.5 V$
Leakage current in 3-state (off state)	Ports 1 to 7	$ I_{TSI} $	–	–	1.0	$\mu A$	$V_{in} = 0.5 V$ to $V_{CC} - 0.5 V$
Input pull-up MOS current	Ports 1 to 7	$-I_p$	30	–	250	$\mu A$	$V_{in} = 0 V$

**Table 15-2. DC Characteristics (cont.)**Conditions:  $V_{CC} = AV_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = -20$  to  $75^\circ C$  (regular specifications) $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement
							conditions
Input capacitance	$\overline{RES}$	$C_{in}$	-	-	60	pF	$V_{in} = 0 V$
	$\overline{NMI}$				30	pF	
	All input pins except $\overline{RES}$ and $\overline{NMI}$		-	-	15	pF	$f = 1 MHz$ $T_a = 25^\circ C$
Current dissipation*	Normal operation	$I_{CC}$	-	12	25	mA	$f = 6 MHz$
				16	30	mA	$f = 8 MHz$
				20	40	mA	$f = 10 MHz$
	Sleep mode			8	15	mA	$f = 6 MHz$
				10	20	mA	$f = 8 MHz$
				12	25	mA	$f = 10 MHz$
	Standby modes			-	0.01	5.0	$\mu A$
RAM standby voltage		$V_{RAM}$	2.0	-	-	V	

\* Current dissipation values assume that  $V_{IH \text{ min.}} = V_{CC} - 0.5V$ ,  $V_{IL \text{ max.}} = 0.5V$ , all output pins are in the no-load state, and all MOS input pull-ups are off.

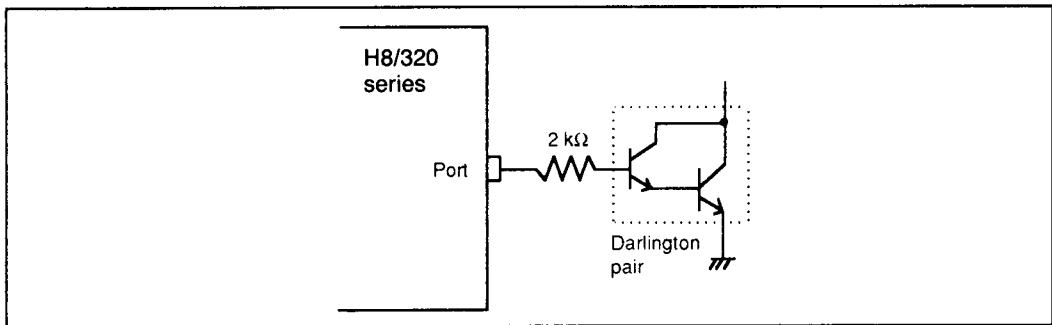
**Table 15-3. Allowable Output Current Sink Values**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = -20$  to  $75^\circ C$  (regular specifications)

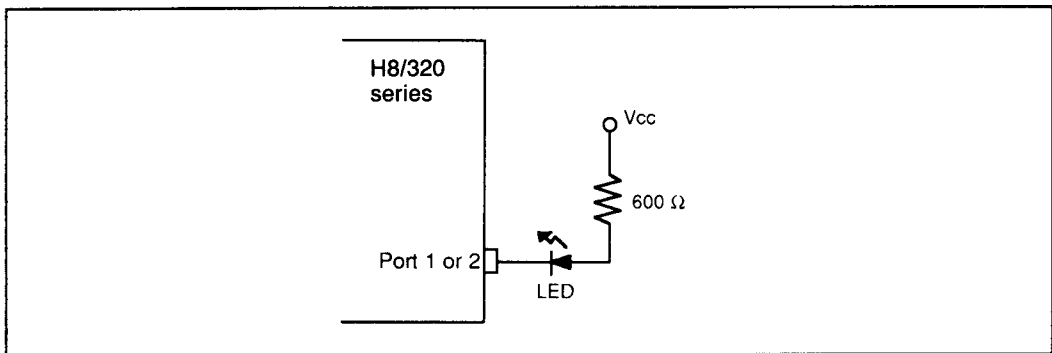
$T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Item		Symbol	min	typ	max	Unit
Allowable output low current sink (per pin)	Ports 1 and 2	$I_{OL}$	—	—	10	mA
	Other output pins		—	—	2.0	mA
Allowable output low current sink (total)	Ports 1 and 2, total	$\Sigma I_{OL}$	—	—	80	mA
	All output pins		—	—	120	mA
Allowable output high current sink (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
	Total of all output	$\Sigma -I_{OH}$	—	—	40	mA

**Note:** To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 15-3. In particular, when driving a Darlington pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 17-1 and 17-2.



**Figure 15-1. Example of Circuit for Driving a Darlington Pair**



**Figure 15-2. Example of Circuit for Driving a LED**

## 15.2.2 AC Characteristics

The AC characteristics for the H8/320 series are listed in three tables. Bus timing parameters are given in table 15-4, control signal timing parameters in table 15-5, and timing parameters of the on-chip supporting modules in table 15-6.

**Table 15-4. Bus Timing**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $\phi = 0.5$  to 10MHz,  $V_{SS} = 0V$ ,

$T_a = -20$  to  $75^\circ C$  (regular specifications),  $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Measurement Item	Symbol	Measurement conditions	6MHz		8MHz		10MHz		Unit
			min	max	min	max	min	max	
Clock cycle time	$t_{cy}$	Fig. 15-4	166.7	2000	125	2000	100	2000	ns
Clock pulse width Low	$t_{CL}$	Fig. 15-4	65	–	45	–	35	–	ns
Clock pulse width High	$t_{CH}$	Fig. 15-4	65	–	45	–	35	–	ns
Clock rise time	$t_{Cr}$	Fig. 15-4	–	15	–	15	–	15	ns
Clock fall time	$t_{Cf}$	Fig. 15-4	–	15	–	15	–	15	ns
Address delay time	$t_{AD}$	Fig. 15-4	–	70	–	60	–	55	ns
Address hold time	$t_{AH}$	Fig. 15-4	30	–	25	–	20	–	ns
Address strobe delay time	$t_{ASD}$	Fig. 15-4	–	70	–	60	–	40	ns
Write strobe delay time	$t_{WSD}$	Fig. 15-4	–	70	–	60	–	50	ns
Strobe delay time	$t_{SD}$	Fig. 15-4	–	70	–	60	–	50	ns
Write strobe pulse width	$t_{WSW}$	Fig. 15-4	200	–	150	–	120	–	ns
Address setup time 1	$t_{AS1}$	Fig. 15-4	25	–	20	–	15	–	ns
Address setup time 2	$t_{AS2}$	Fig. 15-4	105	–	80	–	65	–	ns
Read data setup time	$t_{RDS}$	Fig. 15-4	60	–	50	–	35	–	ns
Read data hold time	$t_{RDH}$	Fig. 15-4	0	–	0	–	0	–	ns
Write data delay time	$t_{WDD}$	Fig. 15-4	–	85	–	75	–	75	ns
Read data access time	$t_{ACC}$	Fig. 15-4	–	280	–	210	–	170	ns
Write data setup time	$t_{WDS}$	Fig. 15-4	30	–	15	–	10	–	ns
Write data hold time	$t_{WDH}$	Fig. 15-4	30	–	25	–	20	–	ns
Wait setup time	$t_{WTS}$	Fig. 15-5	45	–	45	–	45	–	ns
Wait hold time	$t_{WTH}$	Fig. 15-5	10	–	10	–	10	–	ns
E clock delay time	$t_{ED}$	Fig. 15-6	–	25	–	25	–	25	ns
E clock rise time	$t_{Er}$	Fig. 15-6	–	15	–	15	–	15	ns
E clock fall time	$t_{Ef}$	Fig. 15-6	–	15	–	15	–	15	ns
Read data hold time (for E clock)	$t_{RDHE}$	Fig. 15-6	0	–	0	–	0	–	ns
Write data hold time (for E clock)	$t_{WDHE}$	Fig. 15-6	50	–	40	–	30	–	ns

**Table 15-5. Control Signal Timing**Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $\phi = 0.5$  to 10 MHz,  $V_{SS} = 0V$ , $T_a = -20$  to  $75^\circ C$  (regular specifications),  $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Measurement Item	Symbol	Measurement conditions	6MHz		8MHz		10MHz		Unit
			min	max	min	max	min	max	
RES setup time	tRESS	Fig. 15-7	200	–	200	–	200	–	ns
RES pulse width	tRESW	Fig. 15-7	10	–	10	–	10	–	t <sub>eyc</sub>
Mode programming setup time	tMDS	Fig. 15-7	4	–	4	–	4	–	t <sub>eyc</sub>
NMI setup time ( $\overline{NMI}$ , $\overline{IRQ_0}$ to $\overline{IRQ_2}$ )	tNMIS	Fig. 15-8	150	–	150	–	150	–	ns
NMI hold time ( $\overline{NMI}$ , $\overline{IRQ_0}$ to $\overline{IRQ_2}$ )	tNMIH	Fig. 15-8	10	–	10	–	10	–	ns
Interrupt pulse width for recovery from soft- ware standby mode ( $\overline{NMI}$ , $\overline{IRQ_0}$ to $\overline{IRQ_2}$ )	tNMIW	Fig. 15-8	200	–	200	–	200	–	ns
Crystal oscillator settling time (reset)	tOSC1	Fig. 15-9	20	–	20	–	20	–	ms
Crystal oscillator settling time (software standby)	tOSC2	Fig. 15-10	10	–	10	–	10	–	ms

**Table 15-6. Timing Conditions of On-Chip Supporting Modules**Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $\phi = 0.5$  to 10MHz,  $V_{SS} = 0V$ , $T_a = -20$  to  $75^\circ C$  (regular specifications),  $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Item	Symbol	Measurement conditions	6MHz		8MHz		10MHz		Unit
			min	max	min	max	min	max	
FRT Timer output delay time	tFTOD	Fig. 15-11	–	100	–	100	–	100	ns
Timer input setup time	tFTIS	Fig. 15-11	50	–	50	–	50	–	ns
Timer clock input setup time	tFTCS	Fig. 15-12	50	–	50	–	50	–	ns
Timer clock pulse width	tFTCWH tFTCWL	Fig. 15-12	1.5	–	1.5	–	1.5	–	t <sub>eyc</sub>

**Table 15-6. Timing Conditions of On-Chip Supporting Modules (cont.)**Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $\phi = 0.5$  to 10 MHz,  $V_{SS} = 0V$ , $T_a = -20$  to  $75^\circ C$  (regular specifications),  $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Item	Symbol	Measurement conditions	6MHz		8MHz		10MHz		Unit		
			min	max	min	max	min	max			
TMR	Timer output delay time	tTMOD	Fig. 15-13	–	100	–	100	–	100	ns	
	Timer reset input setup time	tTMRS	Fig. 15-15	50	–	50	–	50	–	ns	
	Timer clock input setup time	tTMCS	Fig. 15-14	50	–	50	–	50	–	ns	
	Timer clock pulse width (single edge)	tTMCWH tTMCWL	Fig. 15-14	1.5	–	1.5	–	1.5	–	t <sub>cyc</sub>	
	Timer clock pulse width (both edges)		Fig. 15-14	2.5	–	2.5	–	2.5	–	t <sub>cyc</sub>	
	SCI	Input (Async) clock	tS <sub>cyc</sub>	Fig. 15-16	2	–	2	–	2	–	t <sub>cyc</sub>
		Input clock (Sync)	tS <sub>cyc</sub>	Fig. 15-16	4	–	4	–	4	–	t <sub>cyc</sub>
Transmit data delay time (Sync)		tTXD	Fig. 15-16	–	100	–	100	–	100	ns	
Receive data setup time (Sync)		tRXS	Fig. 15-16	100	–	100	–	100	–	ns	
Receive data hold time (Sync)		tRXH	Fig. 15-16	100	–	100	–	100	–	ns	
Input clock pulse width		tSCKW	Fig. 15-17	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>S<sub>cyc</sub></sub>	
Ports		Output data delay time	tPWD	Fig. 15-18	–	100	–	100	–	100	ns
	Input data setup time	tPRS	Fig. 15-18	50	–	50	–	50	–	ns	
	Input data hold time	tPRH	Fig. 15-18	50	–	50	–	50	–	ns	

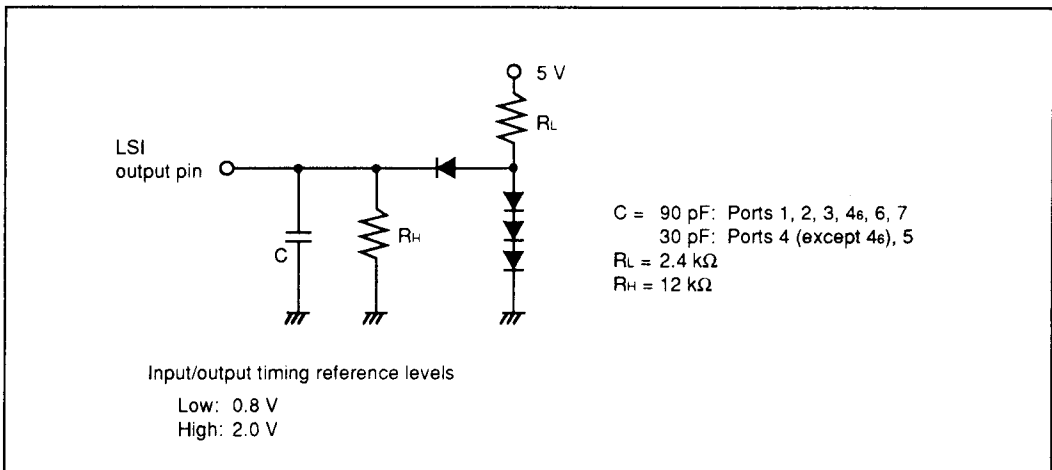
**Table 15-6. Timing Conditions of On-Chip Supporting Modules (cont.)**

Conditions:  $V_{CC} = 5.0V \pm 10\%$ ,  $\phi = 0.5$  to 10 MHz,  $V_{SS} = 0V$ ,

$T_a = -20$  to  $75^\circ C$  (regular specifications),  $T_a = -40$  to  $85^\circ C$  (wide-range specifications)

Item	Symbol	Measurement conditions	6MHz		8MHz		10MHz		Unit	
			min	max	min	max	min	max		
Parallel handshake interface	Handshake input strobe pulse width	tHSW	Fig. 15-19	1.5	–	1.5	–	1.5	–	t <sub>cy</sub>
	Handshake input data setup time	tHIS	Fig. 15-19	10	–	10	–	10	–	ns
	Handshake input data hold time	tHIH	Fig. 15-19	120	–	120	–	120	–	ns
	Handshake output strobe delay time	tHOSD1	Fig. 15-20	–	80	–	80	–	80	ns
		tHOSD2	Fig. 15-20	–	80	–	80	–	80	ns
	Busy output delay time	tHBSOD1	Fig. 15-21	–	150	–	150	–	150	ns
		tHBSOD2	Fig. 15-21	–	150	–	150	–	150	ns

• Measurement Conditions for AC Characteristics



**Figure 15-3. Output Load Circuit**



## 15.3 MCU Operational Timing

This section provides the following timing charts:

15.3.1 Bus Timing	Figures 15-4 to 15-6
15.3.2 Control Signal Timing	Figures 15-7 to 15-10
15.3.3 16-Bit Free-Running Timer Timing	Figures 15-11 to 15-12
15.3.4 8-Bit Timer Timing	Figures 15-13 to 15-15
15.3.6 SCI Timing	Figures 15-15 to 15-17
15.3.7 I/O Port Timing	Figure 15-18
15.3.8 Parallel Handshaking Interface Timing	Figures 15-19 to 15-21

### 15.3.1 Bus Timing

#### (1) Basic Bus Cycle (without Wait States) in Expanded Modes

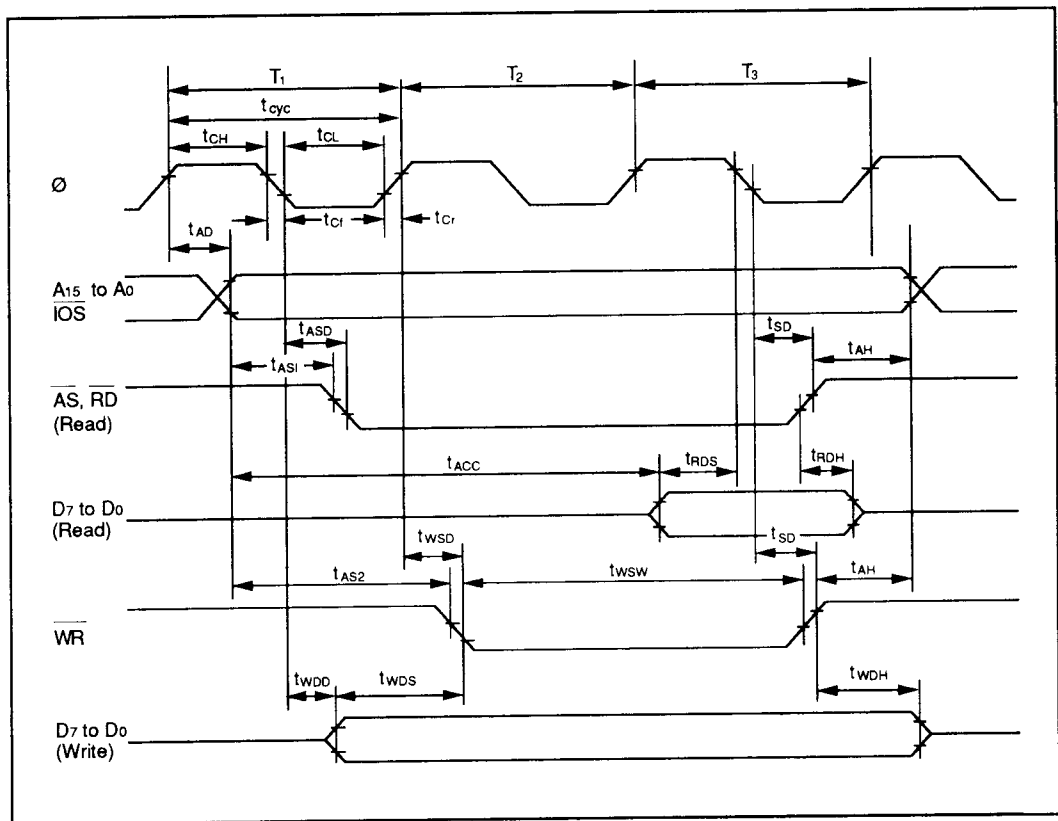
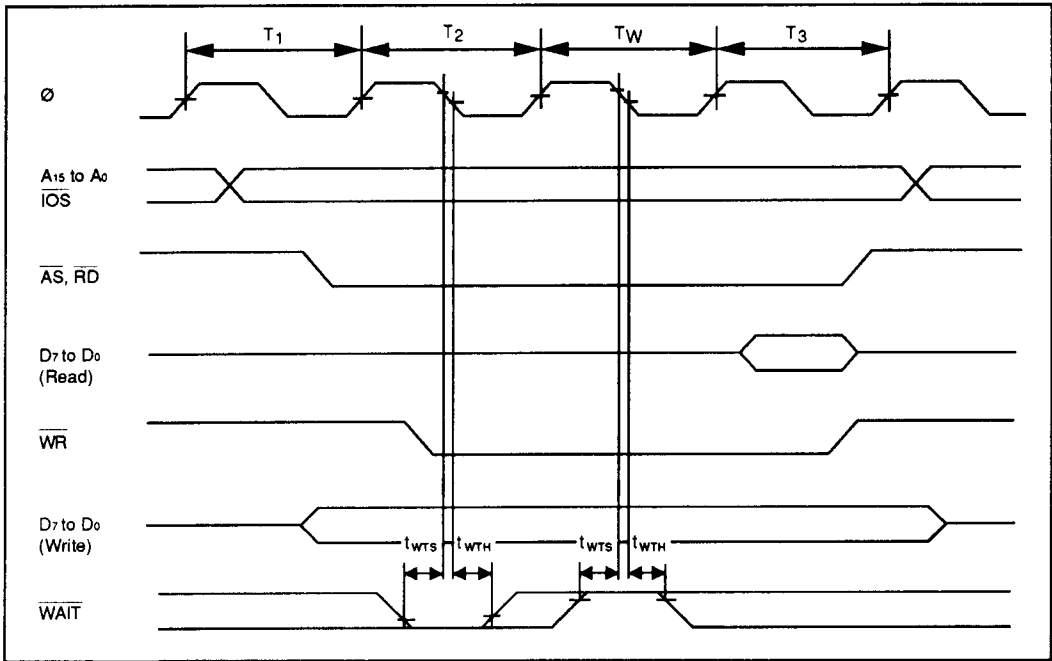


Figure 15-4. Basic Bus Cycle (without Wait States) in Expanded Modes

**(2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes**



**Figure 15-5. Basic Bus Cycle (with 1 Wait State) in Expanded Modes**

### (3) E Clock Bus Cycle

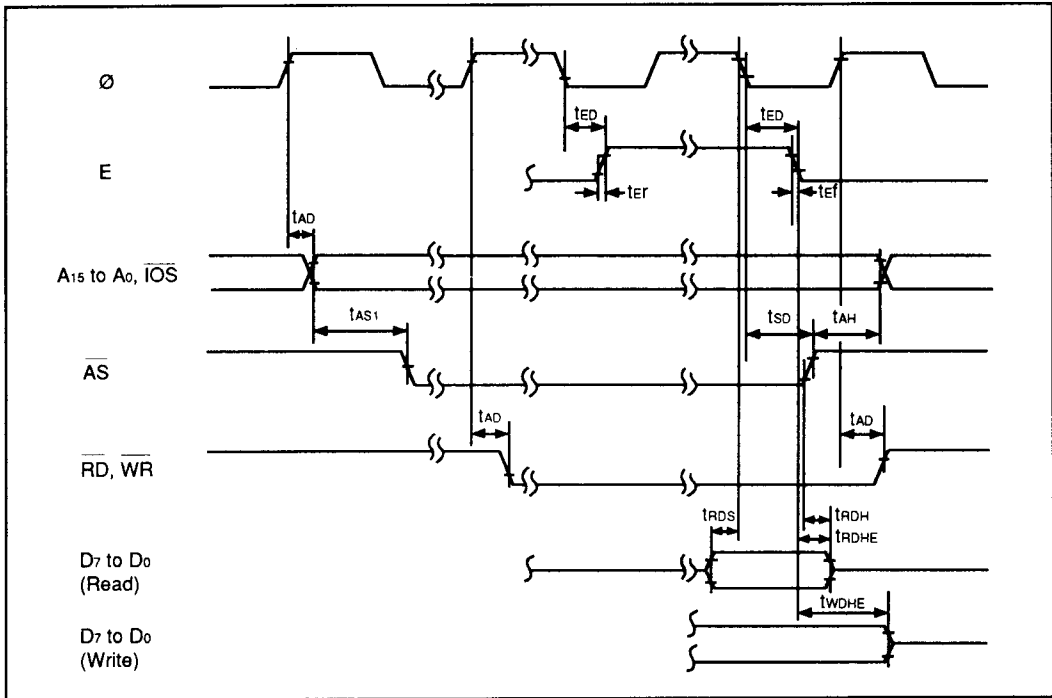


Figure 15-6. E Clock Bus Cycle

## 15.3.2 Control Signal Timing

### (1) Reset Input Timing

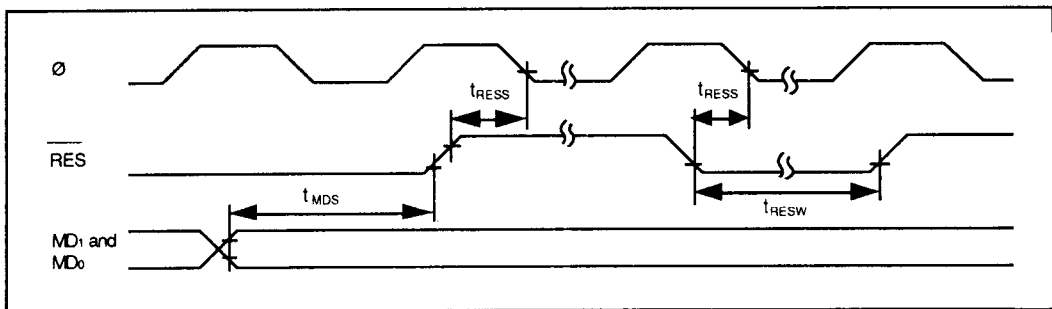


Figure 15-7. Reset Input Timing

## (2) Interrupt Input Timing

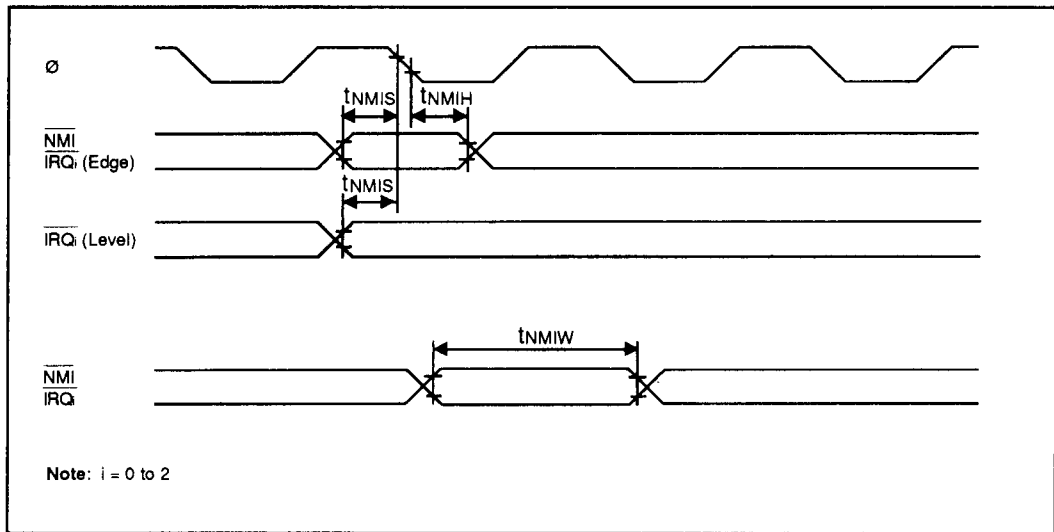


Figure 15-8. Interrupt Input Timing

### (3) Clock Settling Timing

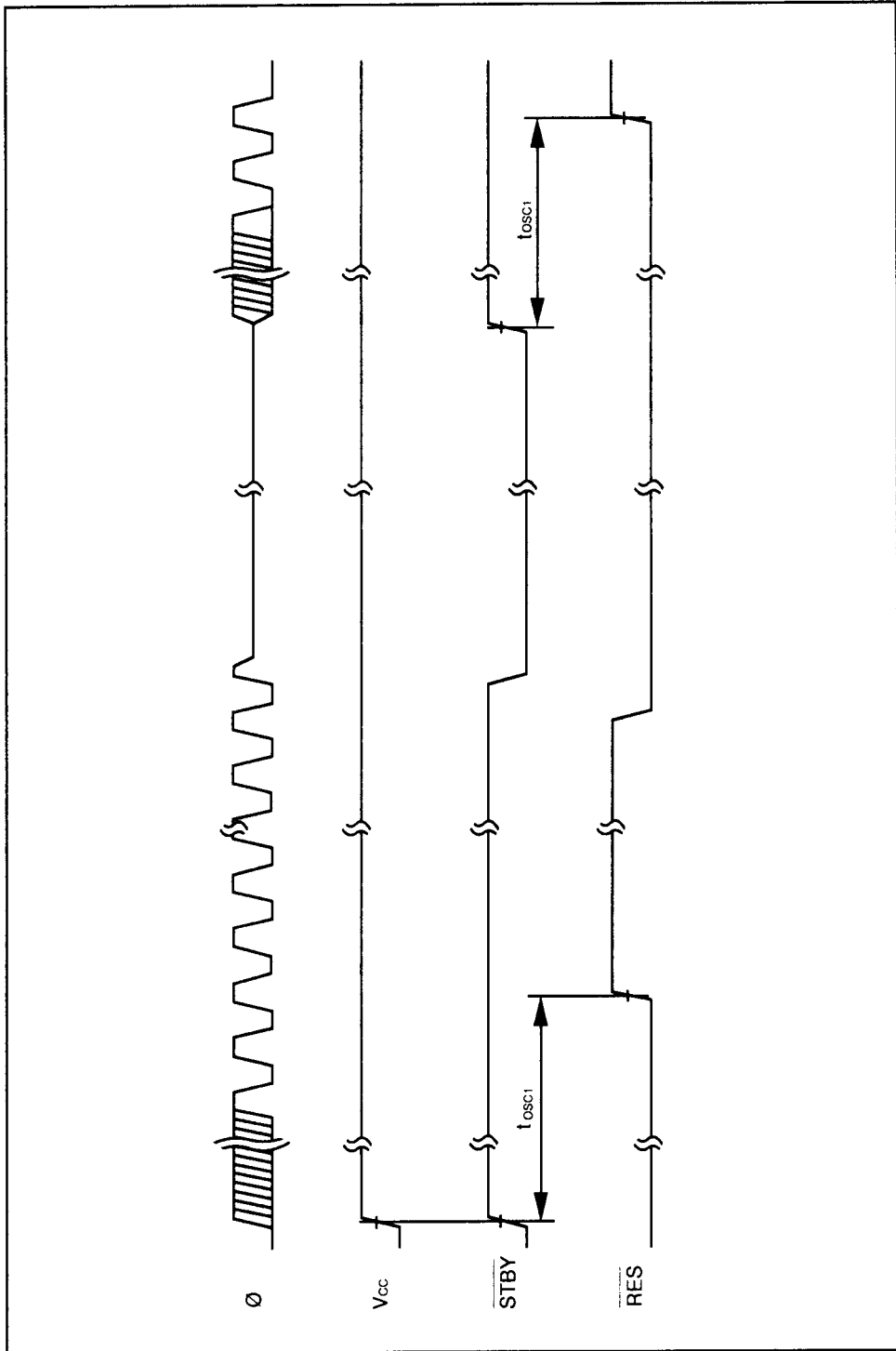


Figure 15-9. Clock Settling Timing

#### (4) Clock Settling Timing for Recovery from Software Standby Mode

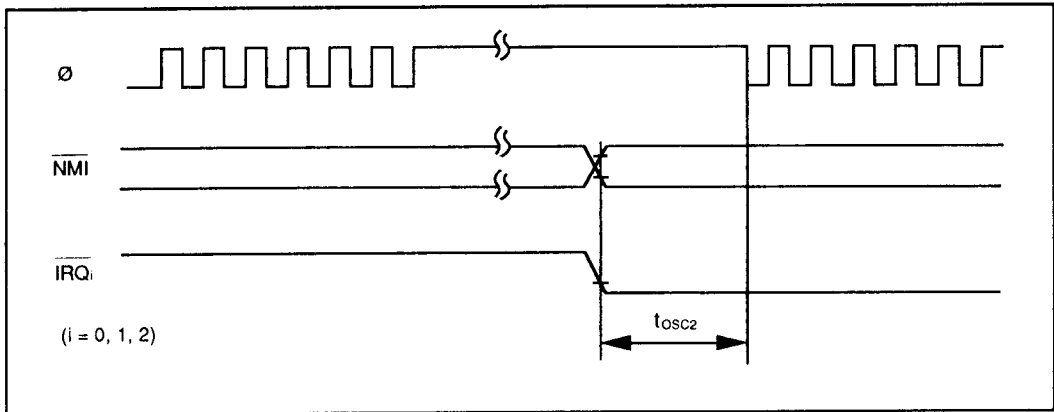


Figure 15-10. Clock Settling Timing for Recovery from Software Standby Mode

### 15.3.3 16-Bit Free-Running Timer Timing

#### (1) Free-Running Timer Input/Output Timing

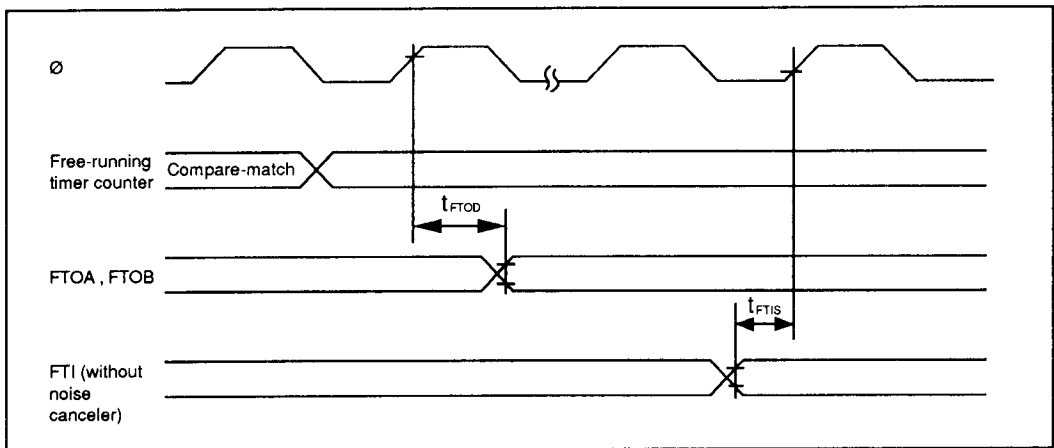


Figure 15-11. Free-Running Timer Input/Output Timing

(2) External Clock Input Timing for Free-Running Timer

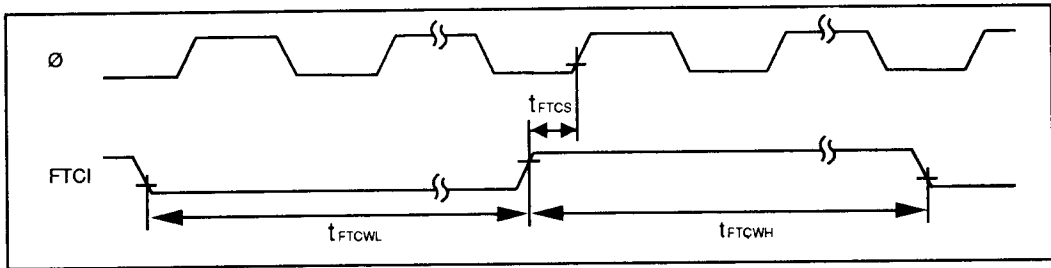


Figure 15-12. External Clock Input Timing for Free-Running Timer

15.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

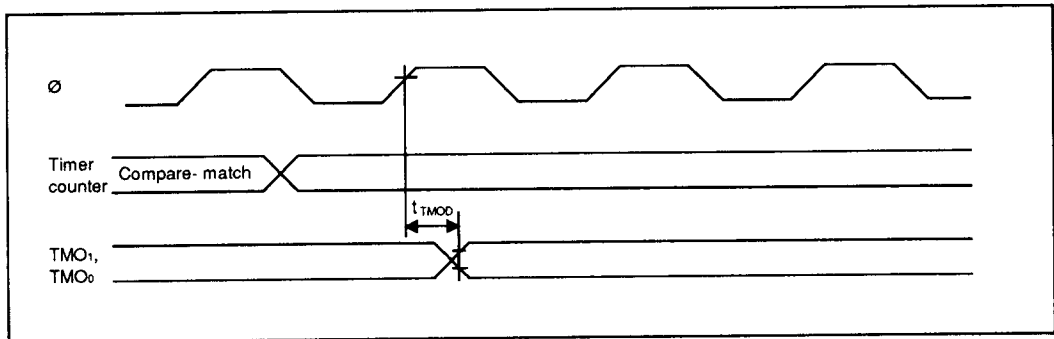


Figure 15-13. 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

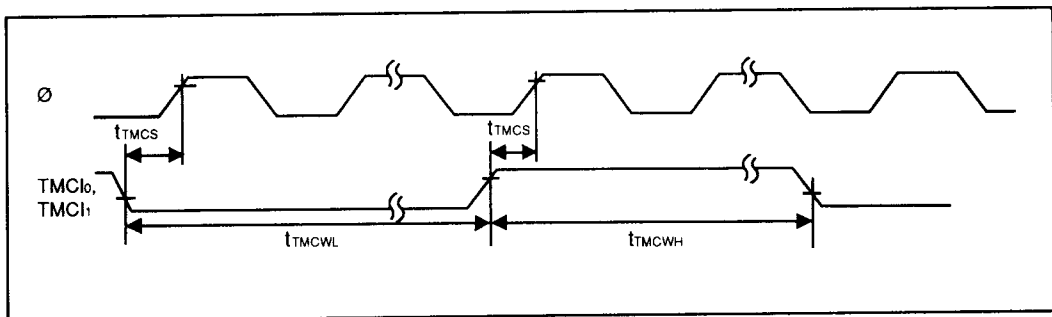


Figure 15-14. 8-Bit Timer Clock Input Timing

### (3) 8-Bit Timer Reset Input Timing

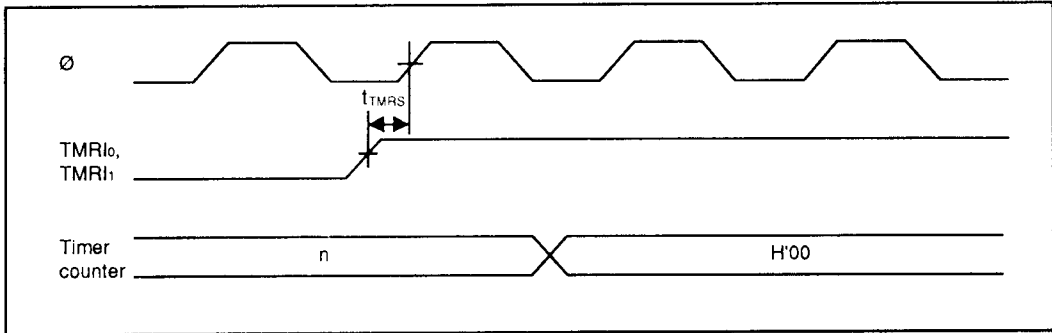


Figure 15-15. 8-Bit Timer Reset Input Timing

## 15.3.5 Serial Communication Interface Timing

### (1) SCI Input/Output Timing

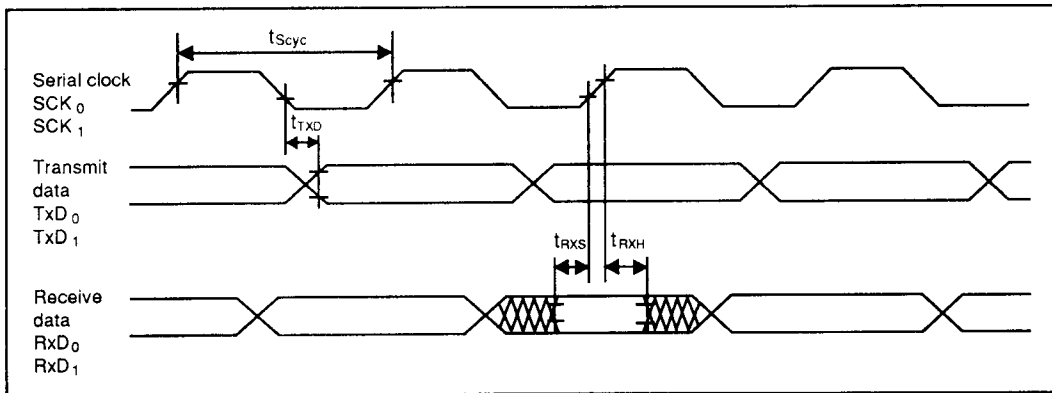


Figure 15-16. SCI Input/Output Timing (Synchronous Mode)

### (2) SCI Input Clock Timing

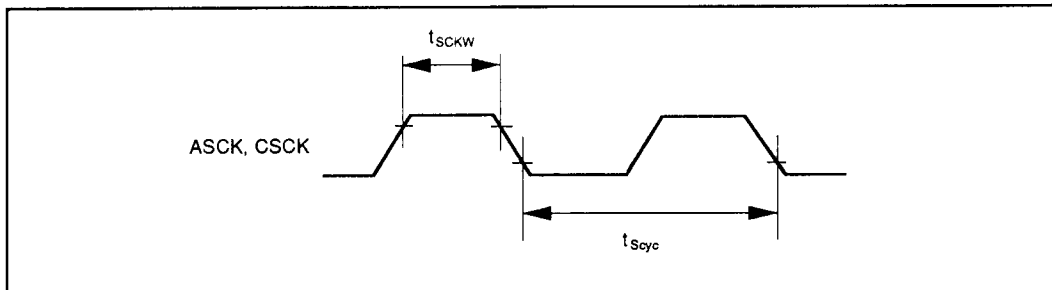


Figure 15-17. SCI Input Clock Timing



### 15.3.6 I/O Port Timing

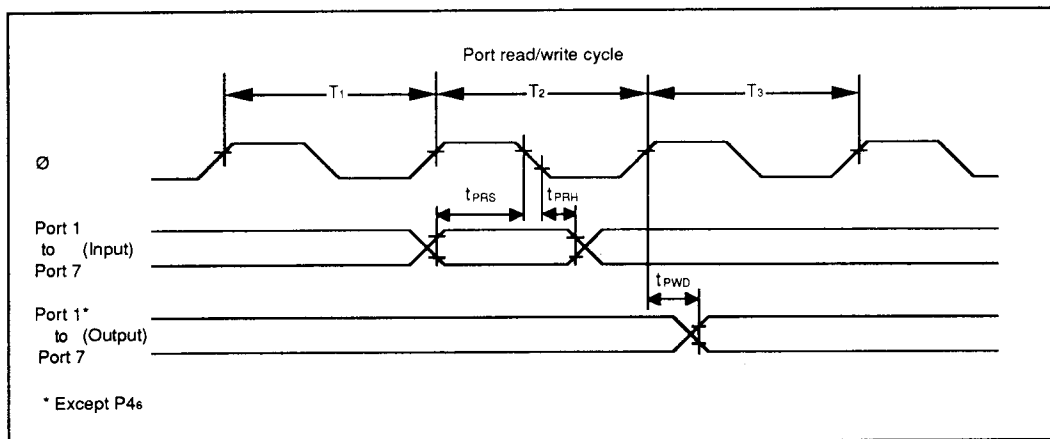


Figure 15-18. I/O Port Input/Output Timing

### 15.3.7 Parallel Handshake Interface Timing

#### (1) Input Strobe Input Timing

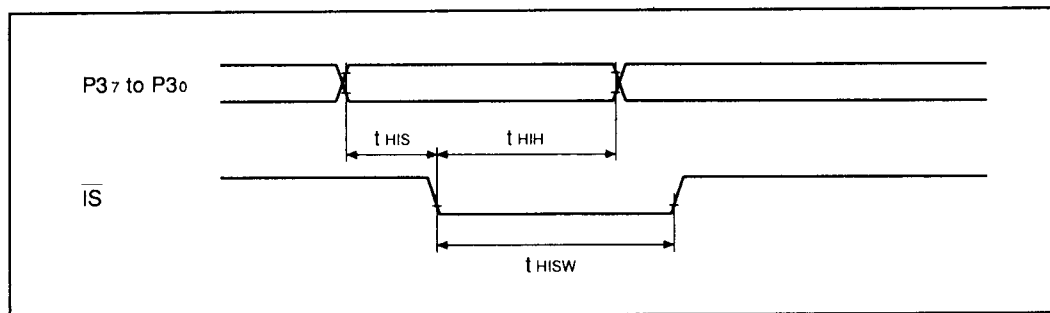


Figure 15-19. Input Strobe Input Timing

## (2) Output Strobe Output Timing

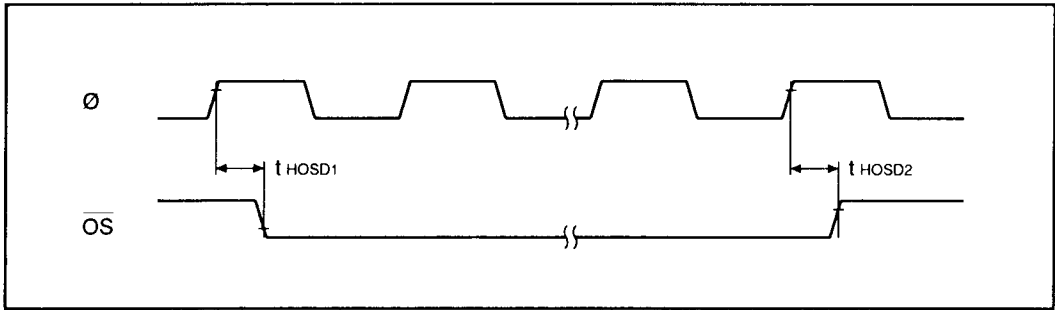


Figure 15-20. Output Strobe Output Timing

## (3) Busy Output Timing

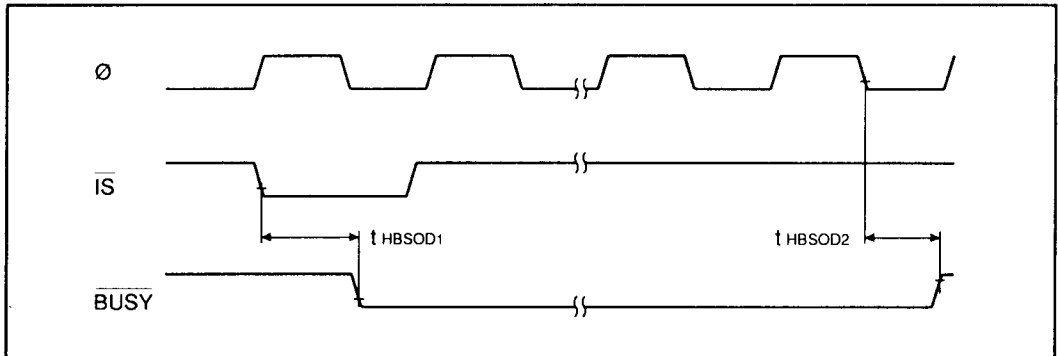


Figure 15-21. Busy Output Timing

Table C-1. Pin States (cont.)

T-90-01

Pin Name	MCU		Hardware Standby	Software Standby	Sleep Mode	Normal Operation
	Mode	Reset				
P55 to P50,	1	3-State	3-State	Prev. state (note 3)	Prev. state	I/O port
	2					
	3					
P66 to P60,	1	3-State	3-State	Prev. state (note 3)	Prev. state	I/O port
	2					
	3					
P77/ $\overline{\text{WAIT}}$	1	3-State	3-State	3-state	3-state	$\overline{\text{WAIT}}$
	2					
	3					
P76 to P74, $\overline{\text{AS}}$ , $\overline{\text{WR}}$ , $\overline{\text{RD}}$ ,	1	High	3-State	High	High	$\overline{\text{AS}}$ , $\overline{\text{WR}}$ , $\overline{\text{RD}}$
	2					
	3	3-State				
P73 to P70,	1	3-State	3-State	Prev. state	Prev. state	I/O port
	2					
	3					

## Notes:

1. 3-state: High-impedance state
2. Prev. state: Previous state. Input ports are in the high-impedance state (with the MOS pull-up on if DDR = 0 and DR = 1). Output ports hold their previous output level.
3. On-chip supporting modules are initialized, so these pins revert to I/O ports according to the DDR and DR bits.
4. I/O port: Direction depends on the data direction (DDR) bit. Note that these pins may also be used by the on-chip supporting modules.

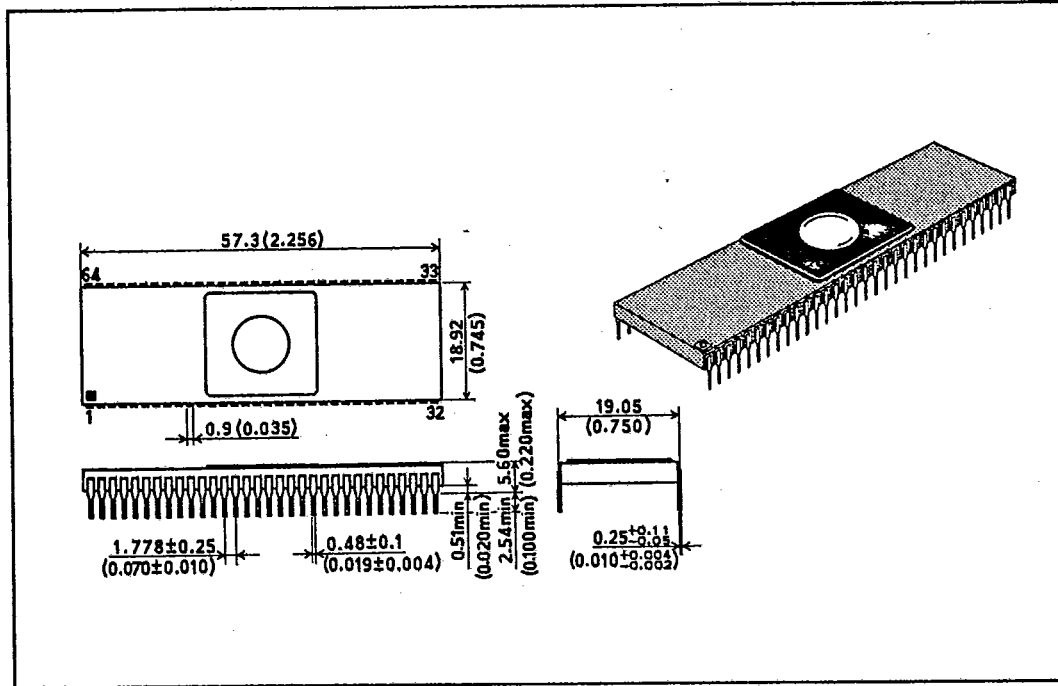
See section 5, I/O Ports for further information.

Appendix D. Package Dimensions

T-90-20

Figure D-1 shows the dimensions of the DC-64S package. Figure D-2 shows the dimensions of the DP-64S package. Figure D-3 shows the dimensions of the FP-64A package.

Unit: mm (inch)



D

Figure D-1. Package Dimensions (DC-64S)

Unit: mm (inch)

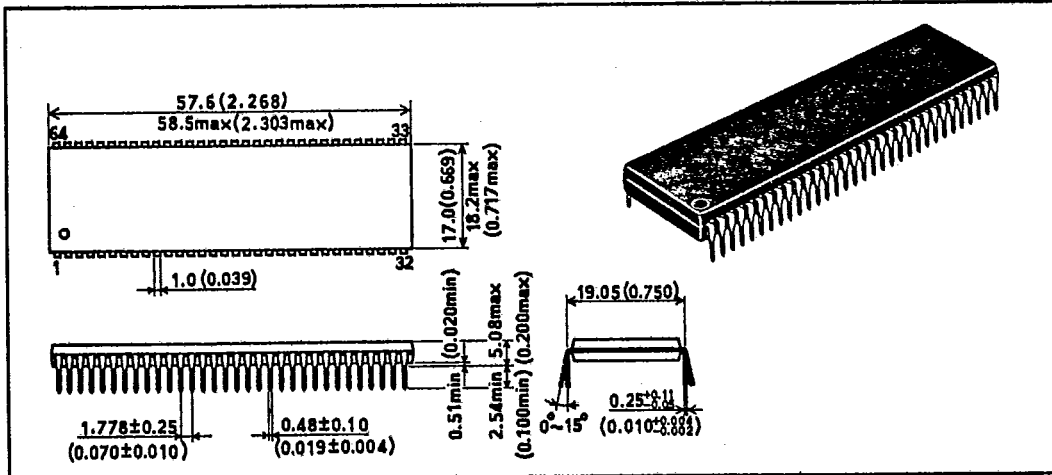


Figure D-2. Package Dimensions (DP-64S)

Appendix E. Package Dimensions

T-90-20

Figure D-1 shows the dimensions of the DC-64S package. Figure D-2 shows the dimensions of the DP-64S package. Figure D-3 shows the dimensions of the FP-64A package. Figure D-4 shows the dimensions of the CP-68 package.

Unit: mm

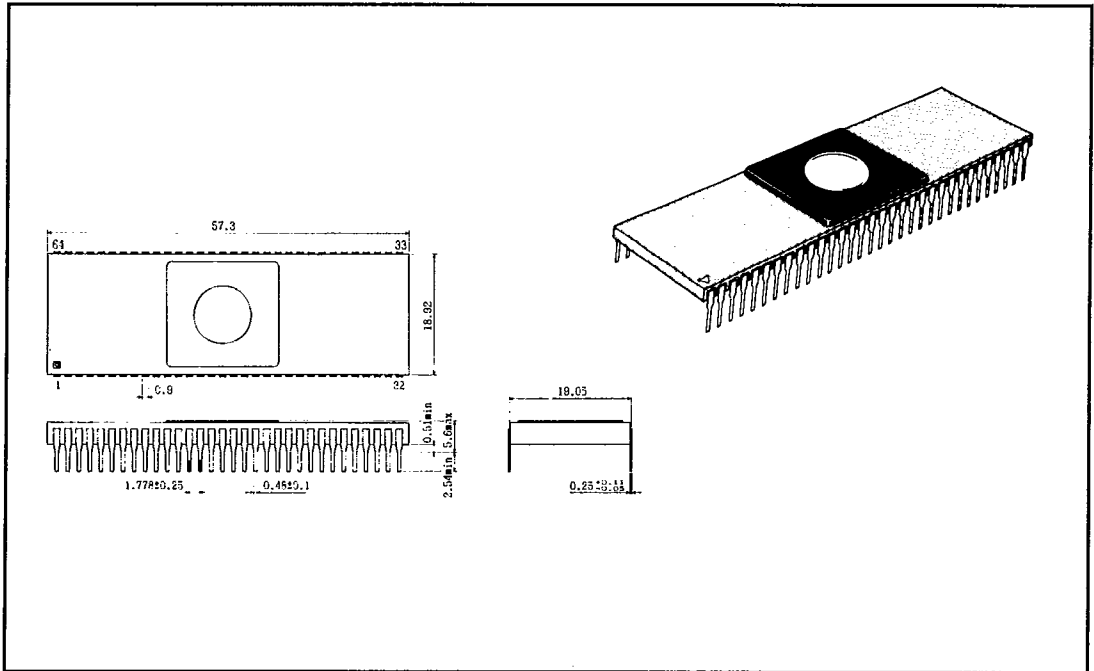


Figure E-1. Package Dimensions (DC-64S)

Unit: mm

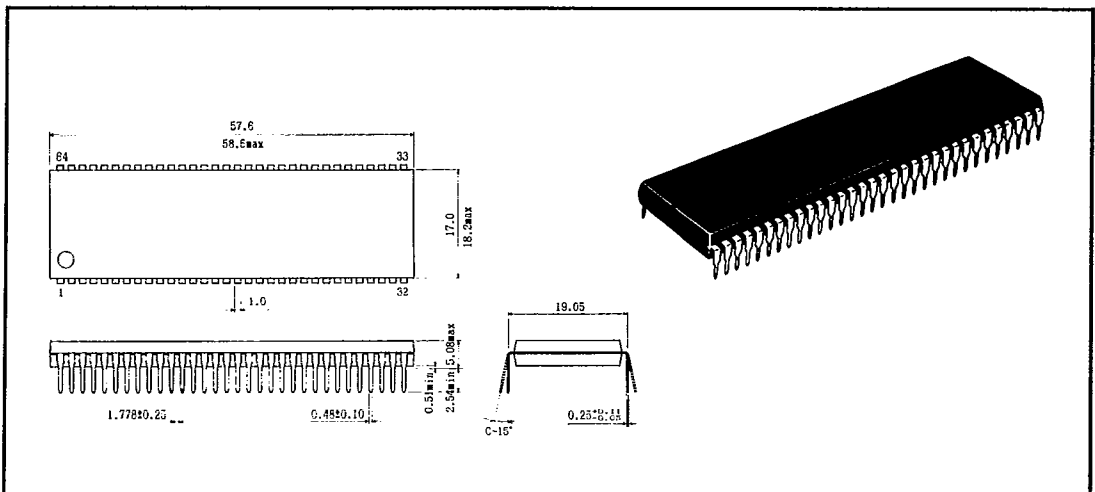


Figure E-2. Package Dimensions (DP-64S)

Unit: mm

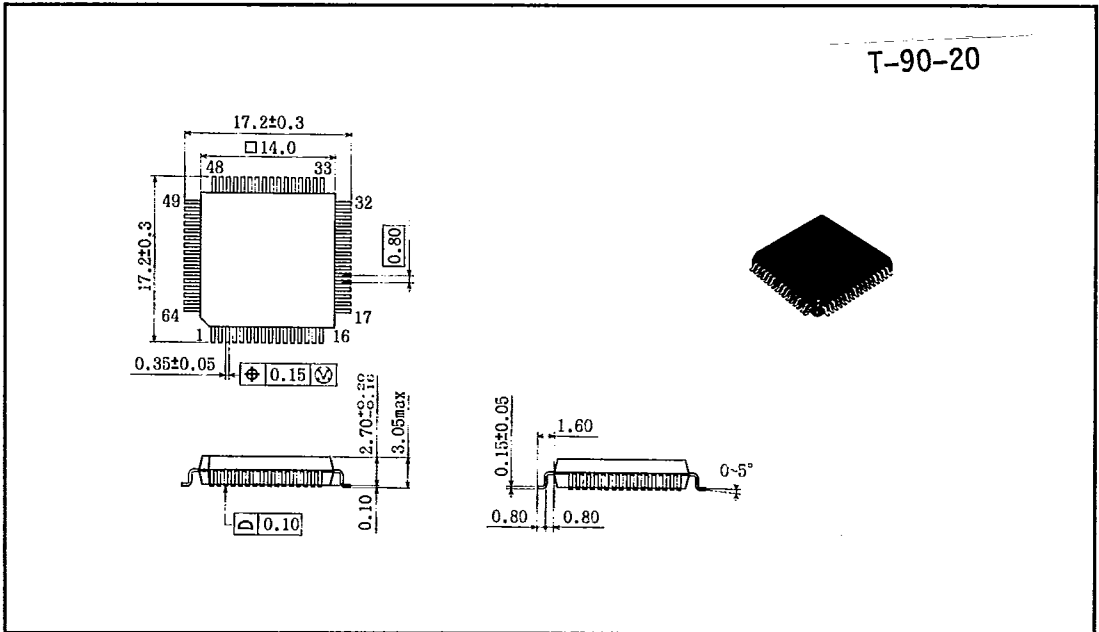


Figure E-3. Package Dimensions (FP-64A)

Unit: mm

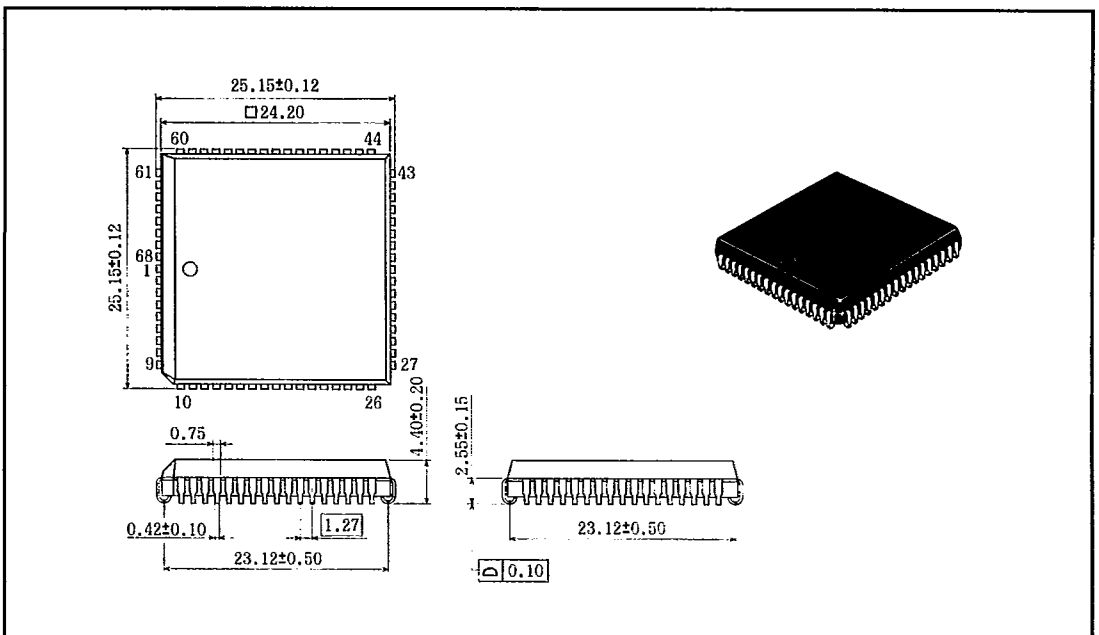


Figure E-4. Package Dimensions (CP-68)