NTR0202PL

Power MOSFET
400 mA, 20 V
P−Channel SOT−23 Package

ON Semiconductor®

http://onsemi.com

Features

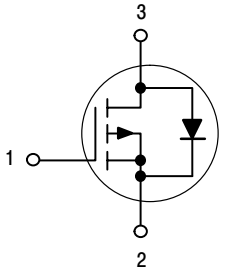
- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
  R_{Dson} = 0.80 Ω, V_{GS} = 10 V
  R_{Dson} = 1.10 Ω, V_{GS} = 4.5 V
- Miniature SOT−23 Surface Mount Package Saves Board Space

Applications

- Dc−Dc Converters
- Computers
- Printers
- PCMCIA Cards
- Cellular and Cordless Telephones

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
20 V	550 mΩ @ 10 V	400 mA

P−Channel

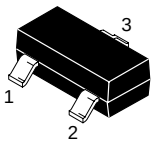


MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

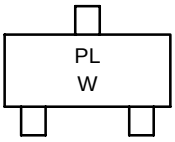
Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	20	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±20	Vdc
Continuous Drain Current @ T_A = 25°C Pulsed Drain Current ($t_p \le 10$ μs)	I_D I_{DM}	0.4 1.0	A
Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	225	mW
Operating and Storage Temperature Range	T_J, T_{stg}	− 55 to 150	°C
Thermal Resistance − Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MARKING DIAGRAM

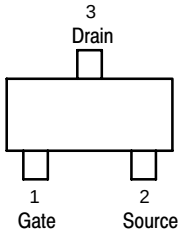


SOT−23
CASE 318
STYLE 21



PL = Device Code
W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTR0202PLT1	SOT−23	3000 Tape & Reel
NTR0202PLT3	SOT−23	10,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μA) (Positive Temperature Coefficient)		$V_{(BR)DSS}$	20 –	– 33	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 25°C) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	– –	– –	1.0 10	μAdc
Gate−Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) (Negative Temperature Coefficient)		$V_{GS(th)}$	1.1 –	1.9 3.0	2.3 –	Vdc mV/°C
Static Drain−to−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 200 mAdc) (V_{GS} = 4.5 Vdc, I_D = 50 mAdc)		$R_{DS(on)}$	– –	0.55 0.80	0.80 1.10	Ω
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 200 mAdc)		g_{fs}		0.5		Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 5.0 Vdc, V_{GS} = 0 Vdc, F = 1.0 MHz)	C_{iss}	–	70	–	pF
Output Capacitance		C_{oss}	–	74	–	
Reverse Transfer Capacitance		C_{rss}	–	26	–	
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	(V_{DD} = 15 Vdc, I_D = 200 mAdc, V_{GS} = 10 V, R_G = 6.0 Ω)	$t_{d(on)}$	–	3.0	–	ns
Rise Time		t_r	–	6.0	–	
Turn−Off Delay Time		$t_{d(off)}$	–	18	–	
Fall Time		t_f	–	4	–	
Total Gate Charge	(V_{DS} = 15 Vdc, I_D = 200 mAdc, V_{GS} = 10 Vdc)	Q_{TOT}	–	2.18	–	nC
Gate−Source Charge		Q_{GS}	–	0.41	–	
Gate−Drain Charge		Q_{GD}	–	0.40	–	
BODY−DRAIN DIODE CHARACTERISTICS (Note 2)						
Diode Forward Voltage (Note 2) (I_S = 400 mAdc, V_{GS} = 0 V) (I_S = 400 mAdc, V_{GS} = 0 V, T_J = 150°C)		V_{SD}	– –	0.8 0.65	1.0 –	Vdc
Reverse Recovery Time	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	–	11.8	–	ns
		t_a	–	9	–	
		t_b	–	3	–	
Reverse Recovery Stored Charge	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	Q_{RR}	–	0.007	–	μC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

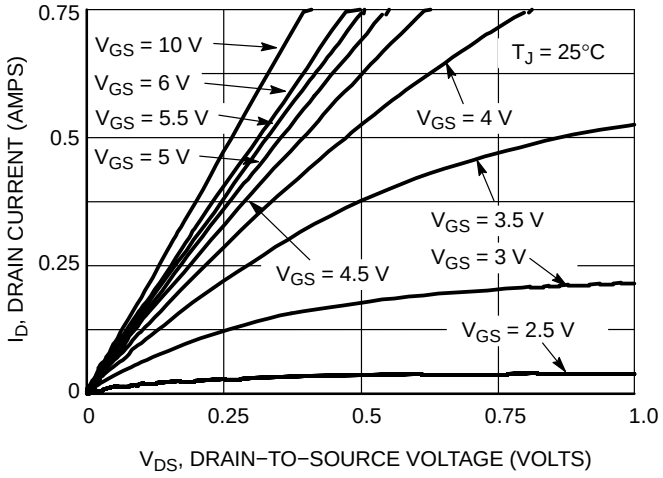


Figure 1. On−Region Characteristics

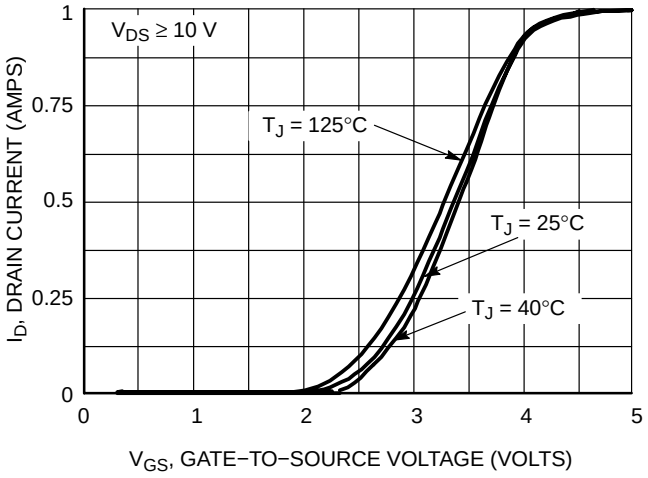


Figure 2. Transfer Characteristics

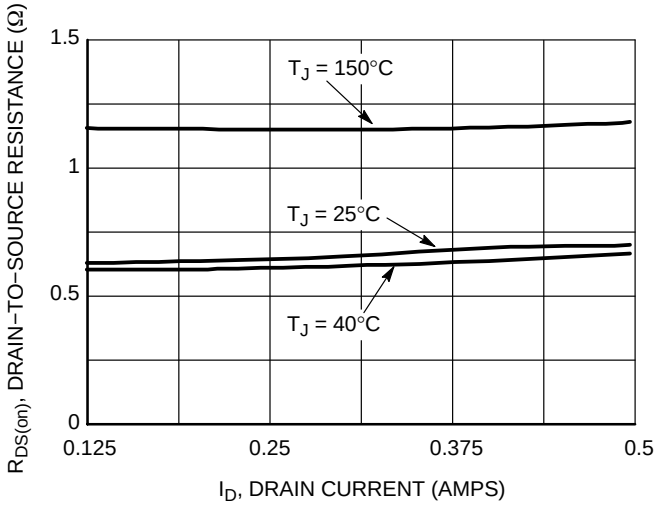


Figure 3. On−Resistance versus Gate−to−Source Voltage

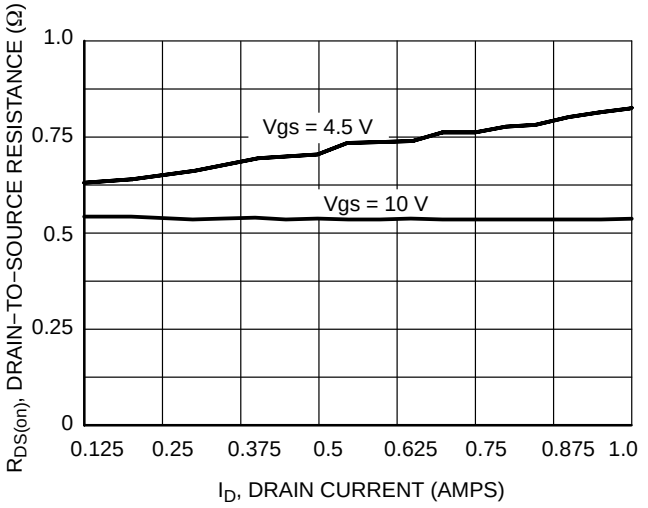


Figure 4. On−Resistance versus Drain Current and Gate Voltage

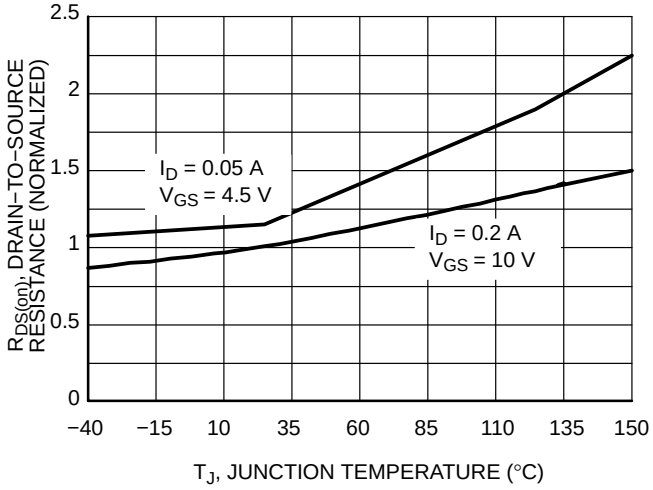


Figure 5. On−Resistance Variation with Temperature

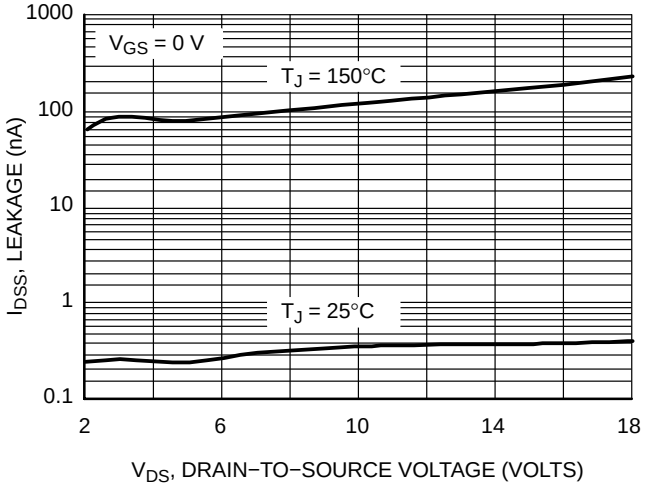


Figure 6. Drain−to−Source Leakage Current versus Voltage

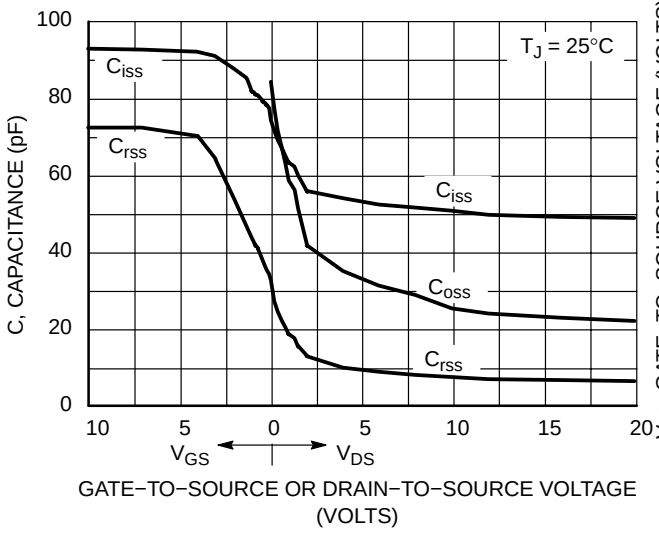


Figure 7. Capacitance Variation

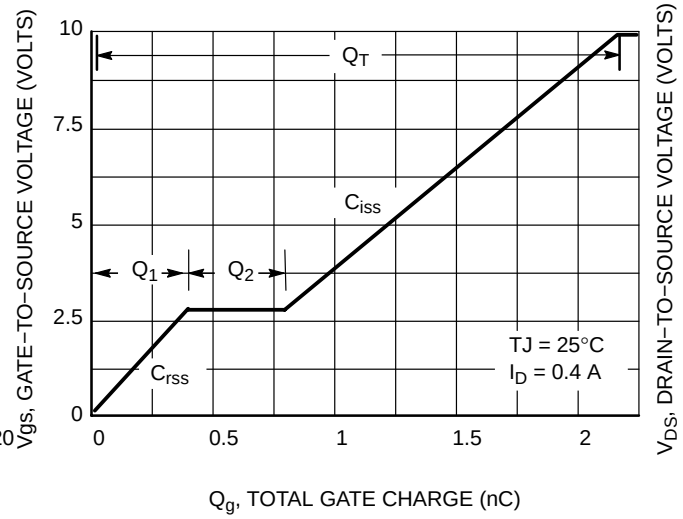


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

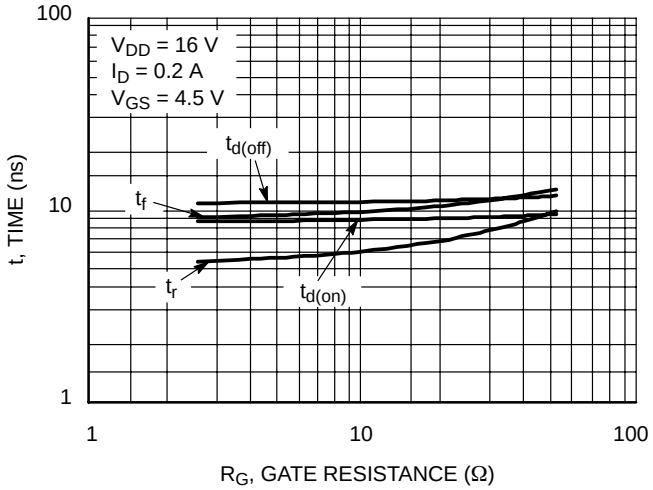


Figure 9. Resistive Switching Time Variation versus Gate Resistance

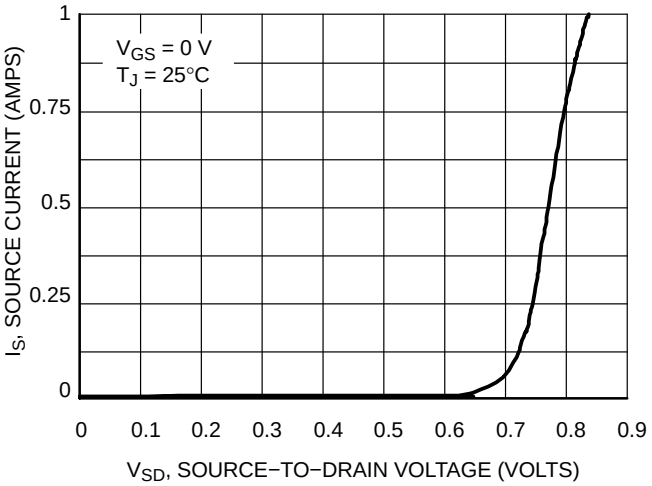
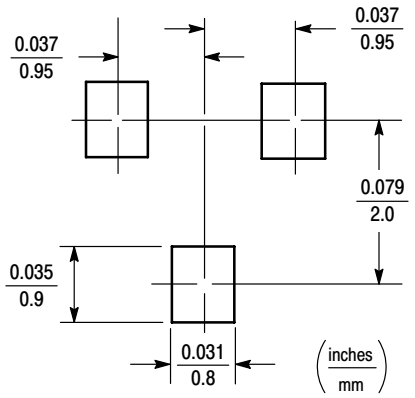


Figure 10. Diode Forward Voltage versus Current

INFORMATION FOR USING THE SOT−23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT−23 POWER DISSIPATION

The power dissipation of the SOT−23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT−23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT−23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT−23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

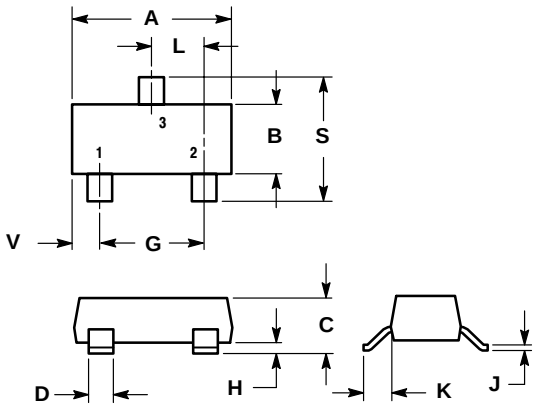
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−09
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIUMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01, −02, AND −06 OBSOLETE, NEW STANDARD 318−09.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0385	0.0498	0.99	1.26
D	0.0140	0.0200	0.36	0.50
G	0.0670	0.0826	1.70	2.10
H	0.0040	0.0098	0.10	0.25
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

Thermal Clad is a registered trademark of the Bergquist Company.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
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ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

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