4-Bit asynchronous bus arbiter — 74F786

FEATURES

- Arbitrates between 4 asynchronous inputs
- Separate grant output for each input
- Common output enable
- On board 4 input AND gate
- Metastable–free outputs
- Industrial temperature range available (–40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F786	6.6ns	55mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
16–pin plastic DIP	N74F786N	I74F786N
16–pin plastic SO	N74F786D	I74F786D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{BR}0 - \overline{BR}3$	Bus request inputs (active low)	1.0/3.0	20µA/1.8mA
A, B, C, D	AND gate inputs	1.0/1.0	20µA/0.6mA
$\overline{EN}$	Common bus grant output enable input (active low)	1.0/1.0	20µA/0.6mA
YOUT	AND gate output	150/40	3.0mA/24mA
$\overline{BG}0 - \overline{BG}3$	Bus grant outputs (active low)	150/40	3.0mA/24mA

Note to input and output loading and fan out table
1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

DESCRIPTION

The 74F786 is an asynchronous 4–bit arbiter designed for high speed real–time applications. The priority of arbitration is determined on a first–come first–served basis. Separate bus grant ($\overline{BG}$n) outputs are available to indicate which one of the request inputs is served by the arbitration logic. All $\overline{BG}$n outputs are enabled by a common enable ($\overline{EN}$) pin. In order to generate a bus request signal a separate 4 input AND gate is provided which may also be used as an independent AND gate. Unused bus request ($\overline{BR}$) inputs may be disabled by tying them high.

The 74F786 is designed so that contention between two or more request signals will not glitch or display a metastable condition. In this situation an increase in the $\overline{BR}$n to $\overline{BG}$n t_{PHL} may be observed. A typical 74F786 has an h = 6.6ns, t = 0.41ns and To = 5µsec.

Where:

h = Typical propagation delay through the device and t and To are device parameters derived from test results and can most nearly be defined as:

t = A function of the rate at which a latch in a metastable state resolves that condition.

To = A function of the measurement of the propensity of a latch to enter a metastable state. To is also a very strong function of the normal propagation delay of the device.

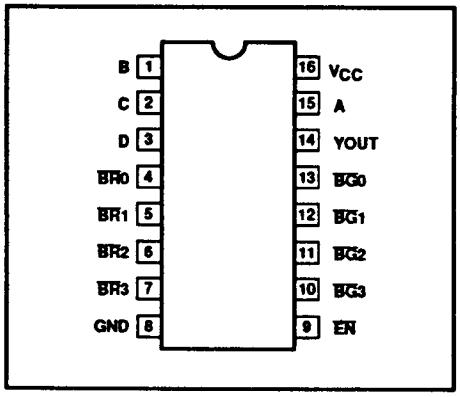
For further information, please refer to the 74F786 application notes.

FUNCTIONAL DESCRIPTION

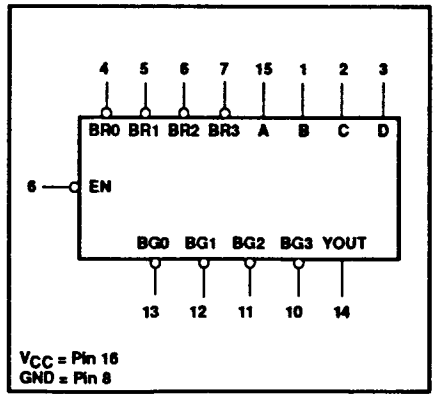
The $\overline{BR}$n inputs have no inherent priority. The arbiter assigns priority to the incoming requests as they are received, therefore, the first $\overline{BR}$ asserted will have the highest priority. When a bus request is received its corresponding bus grant becomes active, provided that $\overline{EN}$ is low. If additional bus requests are made during this time they are queued. When the first request is removed, the arbiter services the bus request with the next highest priority. Removing a request while a previous request is being serviced can cause a grant to be changed when arbitrating between three or four requests. For that reason, the user should not remove ungranted requests when arbitrating between three or four requests. This does not apply to arbitration between two requests.

If two or more $\overline{BR}$n inputs are asserted at precisely the same time, one of them will be selected at random, and all $\overline{BG}$n outputs will be held in the high state until the selection is made. This guarantees that an erroneous $\overline{BG}$n will not be generated even though a metastable condition may occur internal to the device. When the $\overline{EN}$ is in the high state the $\overline{BG}$n outputs are forced high.

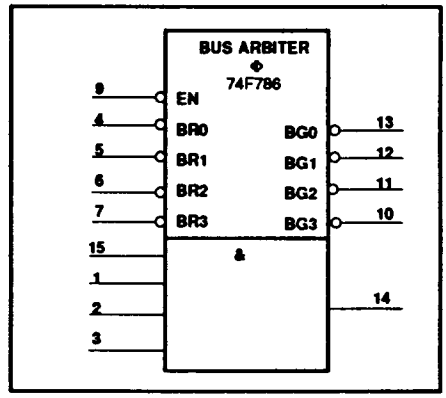
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME	FUNCTION
$\overline{BR0} - \overline{BR3}$	4, 5, 6, 7	Input	Bus request inputs (active low)	The logic of this device arbitrates between these four inputs. Unused inputs should be tied high.
A, B, C, D	15, 1, 2, 3	Input	Inputs of the 4–input AND gate	
$\overline{EN}$	9	Input	Enable input	When low it enables the $\overline{BG0} - \overline{BG3}$ outputs.
$\overline{BG0} - \overline{BG3}$	13, 12, 11, 10	Output	Bus grant outputs (active low)	These outputs indicate the selected bus request. $\overline{BG0}$ corresponds to $\overline{BR0}$, $\overline{BG1}$ to $\overline{BR1}$, etc.
YOUT	14	Output	Output of the 4–input AND gate	
GND	8	Ground	ground (0V)	
V_{CC}	16	Power	Positive supply voltages	

ARBITER FUNCTION TABLE

INPUTS					OUTPUTS			
$\overline{EN}$	$\overline{BR0}$	$\overline{BR1}$	$\overline{BR2}$	$\overline{BR3}$	$\overline{BG0}$	$\overline{BG1}$	$\overline{BG2}$	$\overline{BG3}$
L	1	X	X	X	L	H	H	H
L	X	1	X	X	H	L	H	H
L	X	X	1	X	H	H	L	H
L	X	X	X	1	H	H	H	L
H	X	X	X	X	H	H	H	H

Notes to mode selection function table
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. 1 = First of inputs to go low

ARBITER FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	YOUT
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

Notes to AND function table
1. H = High–voltage level
2. L = Low–voltage level

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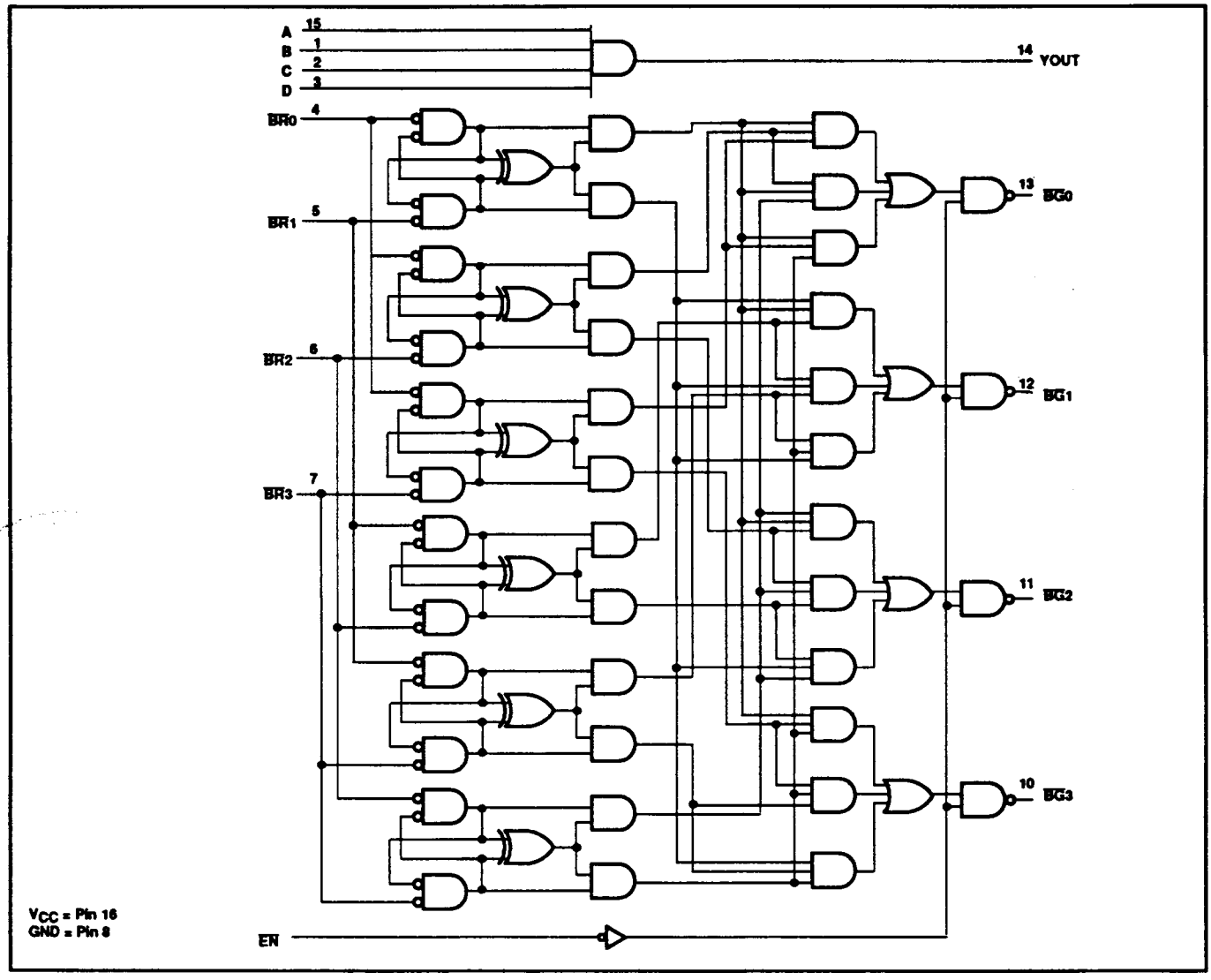
LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		48	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				24	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.3		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	A – D, $\overline{EN}$	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{BRn}$						-1.8	mA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				55	80	mA

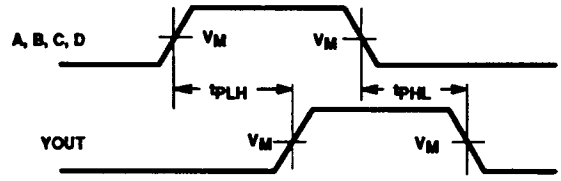
Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

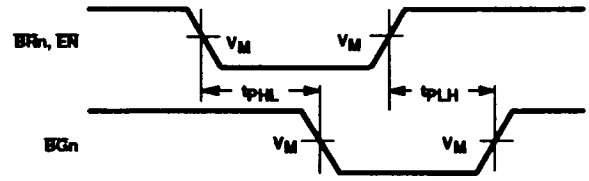
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, A, B, C, D to YOUT	Waveform 1	2.5 2.5	4.5 4.5	7.5 7.5	2.0 2.5	8.5 7.5	2.0 2.5	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{BRn}$ to $\overline{BGn}$	Waveform 2	5.0 4.5	7.0 6.5	10.0 9.5	4.5 4.0	10.5 10.0	4.5 4.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{EN}$ to $\overline{BGn}$	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	2.5 2.5	8.5 8.0	ns
t_{PHL}	Propagation delay, $\overline{BRa}$ to $\overline{BGb}$	Waveform 2	5.0	7.0	10.0	4.5	10.5	4.5	10.5	ns

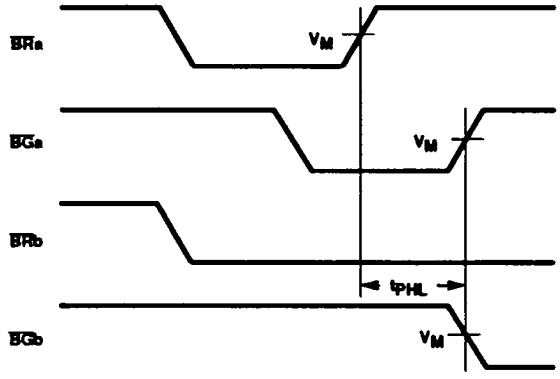
AC WAVEFORMS



Waveform 1. Propagation delay for AND gate to output



Waveform 2. Propagation delay for bus request or enable to bus grant output

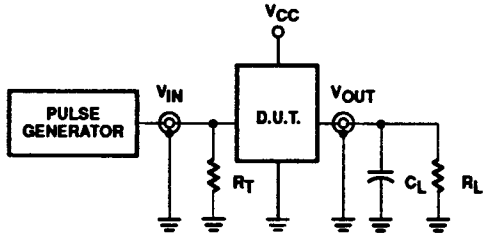


Waveform 3. Propagation delay for bus request to bus grant output

Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. a and b represents any of the bus requests or grants. $\overline{BG}$a low–to–high transition and the $\overline{BG}$b high–to–low transition occur simultaneously.

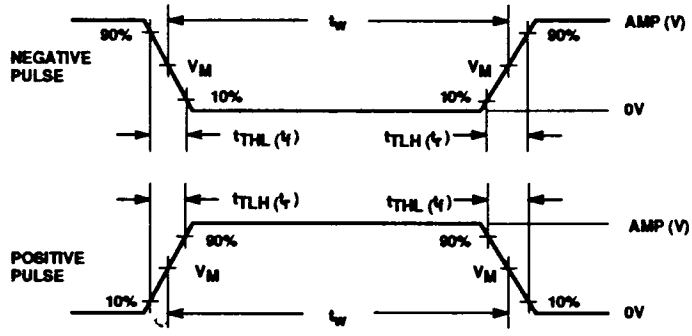
TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns