ONE CHIP PLUS™

ONE-CHIP PLUS™

88C01

MICRO CHANNEL™ INTERFACE CHIP

FEATURES

- Complete Micro Channel interface.
- Programmable decoding for extended memory, expanded memory, multiple I/O ports, and ROM.
- Direct Memory Access (DMA) arbitration and burst mode DMA.
- Programmable memory and I/O timing to accommodate wide access time ranges on memory and peripheral chips.
- User definable Programmable Option Select (POS) registers.
- Programmable Micro Channel board ID.
- Multiplexed memory address lines for direct connection to 1M bit DRAM's.
- User configurable pins to match chip functions to design requirements.
- Meets Micro Channel current drive requirements without buffering.
- Pinout optimized for Micro Channel board layout.

GENERAL DESCRIPTION

The 88C01 provides a complete Micro Channel interface plus the decoding and logic functions required for memory, I/O, and multifunction adapter cards. Full DC and AC bus compatibility is ensured.

The 88C01 can greatly reduce the number of components required for a Micro Channel adapter design. Savings of 20 to 35 ICs are common. Fewer ICs translates into lower parts cost, lower board cost, lower production labor cost, and lower failure rates.

By providing a complete Micro Channel interface, the 88C01 can greatly reduce board design time, while ensuring full Micro Channel compatibility.

The 88C01 includes a unique user configuration capability, which can adjust the characteristics and pinout of the chip to the specific needs of a design. There are over 20 user configurable features that can be set with an inexpensive configuration PROM.

The pinout of the 88C01 has been selected for optimal printed circuit layout. A large ground plane for noise immunity is possible even on a simple double-sided PC board.

ONE CHIP PLUS DEVELOPMENT KIT

With ONE CHIP PLUS you get more than a piece of silicon. The ONE CHIP PLUS development kit provides complete support for Micro Channel interface design, including tools, documentation, software tips, and the process for obtaining an IBM-approved ID number. The development kit contains these items:

- Prototyping board with a working memory adapter circuit, breadboarding area, and connections for logic analyzer probes.
- Interactive 88C01 configuration software.
- A DOS expanded memory driver (meets the EMM 4.0 specification). This can be licensed for use with PS/2™ memory boards.
- EPROM-based code for memory add-in cards which allows any amount of on-board memory to be used with any PS/2 operating system, including OS/2™.
- Recommended PC board layout.
- CAE component library definition for the 88C01, set up for popular CAE programs like OrCAD™.
- Acquisition Engine™ software, which provides background or foreground data acquisition and control for I/O adapters. This can be licensed for distribution with I/O boards, and customized software modules for your product can be easily added.

FUNCTIONAL DESCRIPTION

The 88C01 consists of 6 major functional blocks, shown in figure 1.

The POS register block contains the 8 Programmable Option Select registers required for Micro Channel interfaces.

The memory address mapping block provides support for expanded memory (using the Lotus-Intel-Microsoft specification, EMM 4.0), as well as extended memory for RAMdisks or OS/2. Configurable address line multiplexing saves additional external circuitry by driving 1M bit DRAM chips directly.

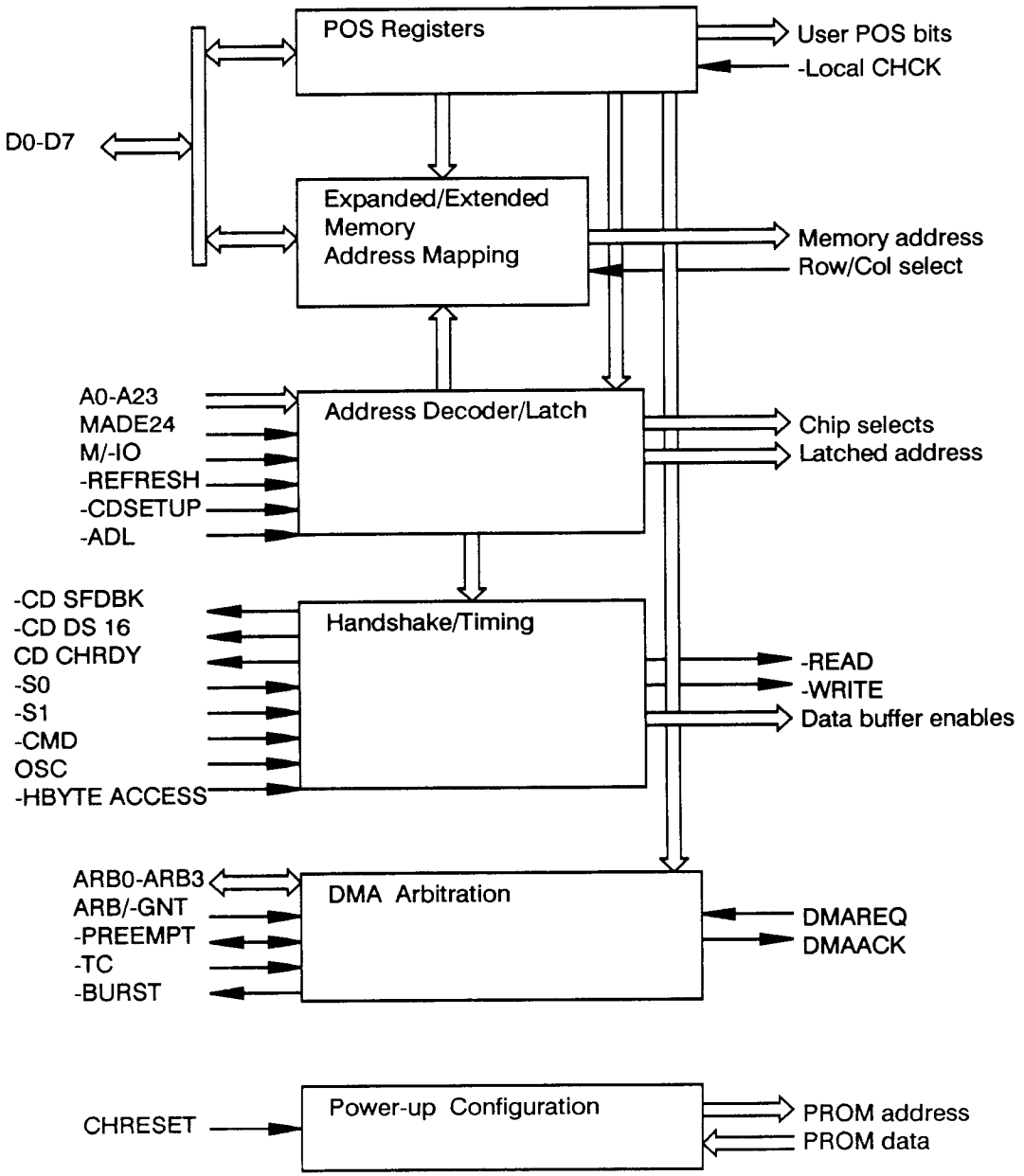
The address decoder block recognizes Micro Channel bus cycles which access the board, and provides chip select signals.

The handshake/timing block decodes the Micro Channel control signals to provide the more commonly used READ and WRITE strobes. This block also generates the Micro Channel feedback signals which govern data bus width and timing.

The DMA arbitration block handles the Micro Channel bus arbitration algorithm, including support for burst mode transfers.

The configuration block is unique to the 88C01. It allows board-specific data such as ID numbers, timing values, address ranges, and optimal pinouts to be set simply by reading data from an external 1K bit TTL PROM.

Figure 1: 88C01 BLOCK DIAGRAM



POS Register Block

This block contains eight registers, shown in table 1. All the registers except 100H and 101H are readable and writeable during setup cycles. Registers 100H and 101H are read-only. Setup cycles occur when the -CDSETUP line is asserted and M/-IO is low to indicate an IO cycle.

POS registers are used in the Micro Channel to eliminate the need for switches on adapter cards. These registers function as software-settable switches that can modify I/O and memory addresses and other board parameters to avoid conflicts.

Each model of adapter card has a 16-bit ID number. The computer can recognize that a new board has been added by reading the ID numbers in all adapter slots. Once a new board is found, automatic configuration software uses a disk file known as the Adapter Description File (ADF) to choose a board setup which does not conflict with other boards in the computer. The POS register values corresponding to that board setup are then written to the board.

Adapter ID

Registers 100H and 101H contain the board ID. This is a read-only value, which can be set through the 88C01's configuration PROM (see Chip Configuration).

Card enable and user bits

Register 102H, bit 0 is the card enable bit. This bit is initially zero at power-up, and is set to one by the computer after POS register initialization is complete. When the card enable bit is zero, the 88C01 disables all chip selects, Micro Channel outputs, and data buffer enables.

The remaining bits in register 102H are user-definable. Many of these bits can be made available on 88C01 pins, depending on configuration information.

Table 1: POS Registers

Address	D7	D6	D5	D4	D3	D2	D1	D0
100H	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
101H	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
102H	user	user	user	user	user	user	user	CE
103H	<----	POS1	-------	---->	<----	POS0	-------	---->
104H	<----	POS3	-------	---->	<----	POS2	-------	---->
105H	CHK	STAT	user	FAIR	ARB3	ARB2	ARB1	ARB0
106H	user	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS	MEMS
107H	PAS	PAS	PAS	MAMT	MAMT	MAMT	MAMT	MAMT

(IDn = board identification bit, user = user-definable POS bit, CE = card enable, POSn = address selection field, CHK = channel check, STAT = channel check status available, FAIR = arbitration fairness, ARBn = DMA arbitration level, MEMS = memory start address, MAMT = memory amount, PAS = page area select)

Address relocation

Registers 103H and 104H contain fields that control the I/O and memory addresses on the board. These fields allow the computer to avoid addressing conflicts. These fields are designated POS0 to POS3, corresponding to the 4 chip select outputs, CS0 to CS3. Each POSn field can be configured in various decoding modes, as shown in table 2.

Table 2: POSn Functions

POS0	(-CS0)	I/O or ROM decode
POS1	(-CS1)	I/O decode (can be DMA)
POS2	(-CS2)	I/O decode
POS3	(-CS3)	I/O decode or page register select for memory.

All four fields can be used for I/O address decoding. In this mode, the POS bits correspond to designated address bits, as shown in the first line of table 3. The remaining address bit values necessary for an address match are provided by chip configuration information (see Chip Configuration). Chip configuration also controls the number of consecutive addresses which trigger the chip select (8 or 16 consecutive address values).

Table 3: POSn Fields

Mode	bit3	bit2	bit1	bit0
I/O address	A13	A12	A8	A4
ROM address	A16	A15	A14	A13

Any value can be used for the base I/O address. For example, if chip configuration sets the base I/O address for POS1 to be 200H, the following choices are available through different settings of the POS1 bits: 200H, 210H, 300H, 310H, 1200H, 1210H, 1300H, 1310H, 2200H, 2210H, 2300H, 2310H, 3200H, 3210H, 3300H, and 3310H. Chip configuration can make the actual address ranges either 8 locations, like 200H-207H, or 16 locations, like 200H-20FH.

The POS0 field can also be configured as a ROM address selector. In this mode, the POS bits correspond to a different set of address bits, as shown in the second line of table 3. These address bits allow an on-board ROM, EPROM, or RAM to be located anywhere in the C0000 to DE000 address range (768K to 888K), in increments of 2000 (8K). The size of the ROM can be configured as 8K, 16K, 32K, or 64K. If the ROM is configured to be larger than 8K, it must start on an address that is an even multiple of its size.

If DMA is used, POS1 selects both the I/O address for the DMA device and the DMA enable register internal to the 88C01. The enable register is at the selected POS1 I/O address plus 8000H (bit A15 equal to one). See the DMA block section for details on the use of the enable register.

When the memory mapping functions of the 88C01 are configured ON, POS3 selects the I/O address for the expanded memory paging registers. CS3 then becomes the memory chip select signal.

DMA priority and error handling

Register 105H contains the DMA arbitration level, arbitration fairness bit, a user-definable bit, and two bits related to error handling.

The CHK bit is used by boards that may send the -CHCK signal on the Micro Channel. This signal is typically generated by a memory parity error. When a board asserts -CHCK, it must indicate this by setting the CHK bit to a zero. The 88C01 sets the CHK bit when it receives the -LOCAL CHCK signal from on-board circuitry.

The STAT bit, if zero, indicates that additional information about a channel check condition is available in registers 106H and 107H. Since the 88C01 uses 106H and 107H for other purposes, the STAT bit should always be set to one.

Memory decoding

Registers 106H and 107H contain information for the memory addressing functions of the 88C01. The MEMS field gives the top 7 bits of the starting address for extended memory on the board, A17-A23 (extended memory is always placed above 1M). The MAMT field gives the amount of extended memory on the board, in units of 512K. Any memory beyond this amount is used for expanded memory. The PAS field selects the memory address range used for the expanded memory paging area. This area is always somewhere in the range from C0000H to D0000H. The PAS field sets the offset from C0000H in units of 16K. If PAS is greater then 4, expanded memory is disabled. (See the Memory mapping section for more detail on expanded and extended memory management and setup)

Address Decoder/Latch Block

This block compares the Micro Channel bus address against the selected address ranges for on-board devices and generates chip select signals. The address ranges come from 88C01 chip configuration information and from the POS registers (see POS block).

Table 4 shows how the decoder interprets the Micro Channel control lines for different types of cycles.

Table 4: Address Decoding

M/-IO	-CDSETUP	Address Match	Cycle Type
high	high	true	memory
low	high	true	I/O
low	low	---	setup (POS)
---	---	false	none

In addition to decoding addresses, this functional block also latches a number of address lines and the chip selects. This is necessary because, in the Micro Channel, address signals go away before the completion of the cycle. The latched signals provided by the 88C01 persist during the cycle so they can be used directly by on-board devices.

Handshake/Timing Block

This block handles the Micro Channel control and timing signals. Read and write data strobes are provided as outputs for on-board devices. High and low byte data buffer enables and a direction control line are provided.

Whenever any on-board device is accessed (one of the chip enables is asserted), the -CD SFDBK signal is sent to the Micro Channel. This tells the bus controller that a device is present.

If 88C01 configuration information indicates that the selected device is a 16-bit device, the -CD DS 16 signal is also sent to the Micro Channel.

The CD CHRDY signal can be used to add wait states for slow devices. The default cycle on the Micro Channel lasts for 200 nsec. A synchronous extended cycle adds an additional 100 nsec. An asynchronous extended cycle can add any additional amount of time, up to a maximum of around 3 usec.

The 88C01 can drive the CD CHRDY signal low to extend cycles based on chip configuration information. I/O cycles and memory cycles can be separately configured to a choice of cycle times, to match the speeds of standard I/O and memory chips.

The 88C01 can also delay the assertion of the -READ and -WRITE signals for I/O devices. This is necessary on some devices in order to guarantee a minimum address to -READ setup time.

DMA Arbitration Block

This block handles the Micro Channel bus arbitration protocol. The DMA arbitration block can be configured to be active or inactive, depending on the needs of a particular design. If DMA is not needed, the DMA pins can be redefined to provide other signals (see Chip configuration).

In order to carry out a DMA transfer, the following steps must occur:

* The DMA controller on the system board should be programmed with the transfer count and other information.
* DMA must be enabled in the 88C01. The 88C01 contains a DMA enable register which is initially set to zero when CHRESET occurs at power-up. Software for a DMA device must write a one to the enable register, whose address depends on the POS1 field (it is the I/O port address plus 8000 hex). The software application notes contained in the ONE CHIP PLUS development kit show how to write code that automatically determines the current I/O address setting for Micro Channel adapters.
* On-board logic can assert the DMAREQ signal. The 88C01 will start the Micro Channel arbitration process, attempting to gain control of the bus.
* When the bus is granted, the DMA controller on the system board will begin to execute the transfer. DMA transfers consist of pairs of memory and I/O cycles. That is, a memory read followed by an I/O write or an I/O read followed by a memory write. During the I/O cycle, the 88C01 sends out the DMAACK signal, to be used by adapter logic much like a

chip select. Normal READ or WRITE strobes and buffer enables occur during DMA.

In single-cycle DMA, bus arbitration will occur after one DMA transfer cycle pair. If DMAREQ is de-asserted and then asserted again, the 88C01 will once again attempt to gain control to do another transfer cycle.

Each time DMAREQ is re-asserted, another single DMA cycle will take place. Eventually, the transfer count in the system board DMA controller will go to zero. At this time, the 88C01 resets its DMA enable register. This features avoids extra undesired arbitration cycles. To see why this is necessary, consider a DMA output operation to a typical device. Most devices will assert DMAREQ when they are ready for another output byte. So, after the last byte is written out and the device is ready, it will again assert DMAREQ. If the 88C01 did not automatically disable and avoid asking for Micro Channel access, arbitration would occur, but the DMA controller would not carry out any cycles because its count is zero. The Micro Channel times out in this case and declares a fatal error. The 88C01 avoids the problem with its internal enable register.

Burst Mode DMA

The one disadvantage of single-cycle DMA is that arbitration occurs even if another DMAREQ signal happens immediately. Time is wasted in the arbitration process if no other board is requesting access to the Micro Channel. Burst mode allows these extra arbitrations to be avoided by allowing multiple DMA transfer cycles to occur without interruption until the transfer count goes to zero or another device wishes to contend for bus control.

The 88C01 can optionally use burst mode DMA. Chip configuration sets burst mode on or off. If burst mode is enabled, DMAREQ **must** be kept asserted as long as additional data remains available from the device, in order to keep the burst going. Conversely, as soon as the device cannot guarantee to have another data byte (or word) ready for the very next bus cycle, DMAREQ **must** be released to terminate the burst. For this reason, adapters which use burst mode usually involve somewhat more complex circuitry.

The only way in which a device typically can guarantee to have more data ready as fast as the Micro Channel controller asks for it is to have the data stored in buffer memory on the adapter board. This can be a FIFO chip or a RAM. Any device which receives data in blocks, like a disk drive or possibly a network interface is a good candidate for burst mode DMA. DMAREQ would be asserted as soon as a block of data arrives, and would be deasserted as soon as DMAACK occurs with only one value left in the buffer memory.

To use burst mode, the following steps must be followed:

* Set up just as for normal DMA, including the enable register. The 88C01 must be configured to enable burst mode.
* The extended programming features of the Micro Channel DMA controller MUST be used to cause the Micro Channel to output the adapter's I/O address during DMA cycles. See pages 3-14 and 3-20 of the PS/2 model 50 Tech. Ref. or pages 3-20 and 3-26 of the model 80 Tech. Ref.
* Send DMAREQ to the 88C01. The 88C01 will attempt to win the bus. When it does, it will immediately assert the Micro Channel -BURST signal, to maintain control.
* When DMAACK occurs and only one last data value is available for input, or only one buffer memory location is free for output, DMAREQ must be de-asserted. The Micro Channel requires that -BURST be released 35 nsec before the end of the -CMD pulse. The timing diagrams in this data sheet show the response time necessary on the adapter card DMAREQ line in order to guarantee the Micro Channel spec. (Note that 200 nsec default cycles require that -BURST be released before latched address information is available, which is not practical with the 88C01).
* Currently, the FAIR field in POS 105H MUST be set to a one (enabled).

Memory Mapping Block

This block handles mapping and multiplexing of address signals to support extended and expanded memory. Extended memory is memory above the 1M address range. Expanded memory follows the Lotus-Intel-Microsoft Expanded Memory Specification (EMM 4.0). With EMM, a 64K area called the paging area is set aside somewhere in the C0000H to DFFFFH address range. Up to four 16K pieces, called pages, of expanded memory can be placed in the paging area at any time. I/O registers are used to control which 4 pages are mapped in. A total of up to 32M of expanded memory can be present on one or more boards in the computer.

When the memory function of the 88C01 is enabled during chip configuration, the values in POS registers 106H and 107H control memory setup. The MEMS field sets the starting address for extended memory, and the MAMT field sets the amount of extended memory.The PAS field controls the expanded memory function, as shown in table 5. PAS is initialized to a disabled setting on power-up.

Table 5: Page Area Select

PAS	Page Area
000	C0000H
001	C4000H
010	CC000H
011	C8000H
100	D0000H
other	disabled

Any memory on the adapter not assigned as extended memory is available as expanded memory. The 88C01 maps Micro Channel paging area accesses into physical memory addresses on the board. These physical address values will start at the value specified in MAMT, so the first portion of on-board memory is used for extended memory and the remaining part is used for expanded memory. For example, if MAMT is 1 (512K), the first page of expanded memory will be physical address 80000H on the board.

Expanded memory pages are swapped into the paging area by writing to the paging registers with I/O write operations (these registers are also readable). The paging register base address is controlled with the POS3 field in the same way as any other I/O address. There are four paging registers, one for each 16K page in the paging area. Each paging register is a 16-bit register, and they are at sequential I/O addresses (incremented by two each time). For example, the paging registers could be at addresses 258H, 25AH, 25CH, and 25EH.

The contents of a paging register are shown in table 6. The enable bit is one to allow memory accesses in the corresponding page. The remaining bits select one of the physical memory pages available on the adapter. Page number 0 is the first 16K block following the memory set aside for extended memory. The total number of pages available depends on the amount of memory on the adapter card. The 88C01's paging registers can handle up to 1024 pages, or 16M, of expanded memory.

The paging registers correspond to the 4 16K portions of the paging area by matching A2 and A1 of the paging register address with A15 and A14 of the paging area address. For example, if the paging area starts at C4000H, A15 and A14 for the first 16K page are 01 (binary). The paging register which controls that 16K area has 01 in the A2 and A1 bits. So, if the paging register base address is 258H, the register for the first 16K area is 25AH. Table 7 shows the order of the four paging registers for each possible paging area selection, using B to designate the base I/O address.

Table 7: Paging Registers vs. Paging Area

B = Base address

Paging Area	Paging Registers			
C0000H	B	B+2	B+4	B+6
C4000H	B+2	B+4	B+6	B
C8000H	B+4	B+6	B	B+2
CC000H	B+6	B	B+2	B+4
D0000H	B	B+2	B+4	B+6

The memory block in the 88C01 not only generates the higher order address lines for expanded and extended memory, it is also capable of multiplexing these lines with the low order address lines to provide signals suitable for directly driving 1M bit DRAM chips. The row/col select input to the 88C01 controls the multiplexing. One setting of row/col select produces MA1-MA10 on the

Table 6: Paging Register Value

low byte	enable	pg6	pg5	pg4	pg3	pg2	pg1	pg0
high byte	x	x	x	x	x	pg9	pg8	pg7

output lines and the other produces MA11-MA20. MA21 through MA23 can optionally be made available on additional pins to select among multiple banks of RAMs for memory boards larger than 2M bytes.

The ONE CHIP PLUS Development Kit contains drivers for expanded memory and EPROM code to automatically initialize POS registers 106H and 107H, based on the amount of other memory in the computer. The computer does not automatically set up these registers with built-in code. The development kit also contains further examples of programming the paging registers.

Chip Configuration Block

This block controls parameters of the 88C01 which are fixed for any particular board design, but differ from board to board. The 88C01 reads configuration information at power-up (CHRESET asserted) to set the board ID, timing values, pinout choices, and other options.

Rather than provide all possible signals on separate pins, which would require almost 100 pins and increase the size and complexity of the chip, the sockets and the manufacturing technology, the 88C01 allows pinout configuration. Each application will only need a subset of the possible signals, so configurations have been carefully selected for optimum use of the 84 available pins. These configurations are user selectable.

An external 1K bit TTL PROM such as a 74S287 provides the configuration information. The ONE CHIP PLUS development kit contains software to allow easy generation of configuration PROMs. A configuration PROM is an inexpensive part (around a dollar) which adds great flexibility to the 88C01. The PROM is connected to pins on the 88C01 which function as PROM address and data lines during CHRESET, and as latched bus address outputs at other times. The PROM itself should have its output enabled only during CHRESET.

CHRESET must be asserted for at least 50 usec to allow the 88C01 to read configuration information (the Micro Channel specification provides 100 msec as the minimum CHRESET time). Data is clocked in using the Micro Channel oscillator signal.

A complete table of configuration bits in the PROM is given in an appendix at the end of this data sheet. Table 8 shows available configuration options.

Pinout choices are governed by the specific application. For example:

* If only 8-bit devices are used on a board, there is no need for the high byte buffer enable signal, so those pins can be redefined as user POS bit outputs.
* If DMA is not used, the DMA pins can be redefined as user POS bits and memory address bits.
* If a board is just an I/O adapter, without expanded or extended memory, the memory function can be disabled and the address outputs defined as the low order address bits A0 to A9, saving an external latch.

The ONECHIP software in the development kit is designed to guide a designer through the optimal selection process.

Table 8: Configuration Options

Enable expanded and extended memory?	YES/NO
Enable direct memory access (DMA)?	YES/NO
Burst mode?	YES/NO
POS0 mode?	I/O or ROM
Base I/O address for each chip select?	0 to FFFFH
Number of consecutive I/O locations for each chip select?	8 or 16
Data width for each chip select?	8 or 16 bits
ROM size (if ROM decoding selected)?	8K, 16K, 32K, or 64K
Micro Channel ID number?	0 to FFFFH
I/O access time?	configurable
Memory access time?	configurable
Address to -READ,-WRITE setup time?	0-220 nsec
DMAREQ polarity?	HIGH/LOW
DMAACK polarity?	HIGH/LOW
User POS bit outputs?	YES/NO

88C01 PIN DESCRIPTION

SIGNAL	TYPE	DESCRIPTION
A0-A23	input	Address. Generates all memory, I/O, and internal decoding. A0 is the least significant bit and A23 the most significant.
MADE24	input	Memory address enable 24. When low during a memory cycle, indicates that the processor is addressing the first 16M bytes.
-REFRESH	input	Refresh. When low, a memory refresh cycle occurs. Address lines A0 through A8 determine the refresh address.
M/-IO	input	Memory/-Input Output. When high, a memory cycle is indicated. When low, the current cycle is an I/O cycle.
-ADL	input	Address Decode Latch. The trailing edge of -ADL is used to latch valid address and status bits.
-S0	input	Status bit 0. Defines the type and indicates the start of a Micro Channel cycle.
-S1	input	Status bit 1. Defines the type and indicates the start of a Micro Channel cycle.
-CD SETUP	input	Card Setup. When low, indicates that a setup cycle is occurring. Setup cycles are otherwise just like normal I/O cycles. Setup cycles allow access to the POS registers for board ID and other setup information.
-CMD	input	Command. During a write cycle data is valid while -CMD is active. During a read cycle, data must be valid before the trailing edge of -CMD, and must be held through the trailing edge.
14.3 MHz OSC	input	Oscillator. This timing signal is used to generate the Micro Channel handshake timing.
CHRESET	input	Channel Reset. When active, devices in the Micro Channel are reset. All devices must become disabled (a later write to a POS register will enable the board). The 88C01 carries out its initialization during CHRESET, reading configuration information from a small TTL PROM.

This table shows the signals used by the 88C01. Some boxes in the table contain more than one signal name. These are configurable pins on the 88C01, whose function may be chosen based on configuration PROM information.

88C01 PIN DESCRIPTION (continued)

SIGNAL	TYPE	DESCRIPTION
D0-D7	I/O	Data. D0 is the least significant bit and D7 the most significant.
-CD SFDBK	output	Card Selected Feedback. Acknowledges selection of a device on the board. -CD SFDBK is driven low whenever memory or I/O on the adapter is addressed, but not during setup cycles.
-CD DS 16	output	Card Data Size 16. Indicates a 16 bit memory or I/O device. -CD DS 16 can be selectively driven low based on 88C01 configuration information.
CD CHRDY	output	Channel Ready. When driven low, indicates that more time is needed to complete the current memory or I/O cycle. CD CHRDY can be driven low for a selectable period based on 88C01 configuration information.
MA10/11-MA1/12	local output	Mapped, multiplexed memory address. The row/col select input controls the multiplexing function.
LA0-LA1	local output	Latched address.
PROM D0-D1	local input	PROM data (only during CHRESET).
MA2/13-MA9/20	local output	Mapped, multiplexed memory address.
LA2-LA9	local output	Latched address.
PROM A7-A0	local output	PROM address (only during CHRESET).
ARB0	I/O	Arbitration Bus bit 0. Used to arbitrate for bus access during DMA.
POS 105 D5	local output	POS register 105 bit 5. User definable control signal.
ARB1	I/O	Arbitration Bus bit 1. Used to arbitrate for bus access during DMA.
POS 106 D7	local output	POS register 106 bit 7. User definable control signal.
ARB2	I/O	Arbitration Bus bit 2. Used to arbitrate for bus access during DMA.
MA21	local output	Memory Address 21. Optional high-order latched address bit for memory board designs.
ARB3	I/O	Arbitration Bus bit 3. Used to arbitrate for bus access during DMA.
MA22	local output	Memory Address 22. Optional high-order latched address bit for memory board designs.
-PREEMPT	I/O	Preempt. Can be driven by adapters to request usage of the bus (DMA).
MA23	local output	Memory Address 23. Optional high-order latched address bit for memory board designs.

88C01 PIN DESCRIPTION (continued)

SIGNAL	TYPE	DESCRIPTION
-BURST	output (open collector)	Burst. Driven low to indicate that the current bus owner desires multiple bus cycles without having to re-arbitrate each time.
ROW/COL SELECT	local input	Row/Column Select. Used on memory board designs to control address line multiplexing. A low input selects the high order address lines for output to the memory chips and a high input selects the low order address lines.
DMAREQ	local input	DMA Request. Driven by adapter logic to indicate that a DMA cycle is desired. Polarity of this signal is configurable. DMA only occurs if the DMA enable register in the 88C01 has been set.
POS 102 D4	local output	POS register 102 bit 4. User definable control signal.
DMAACK	local output	DMA Acknowledge. Indicates to adapter logic that a DMA cycle is in progress. This signal acts like a chip select. Normal I/O read or write signals will also occur during the cycle.
POS 102 D5	local output	POS register 102 bit 5. User definable control signal.
-TC	input	Terminal Count. A low signal indicates the last cycle of a DMA transfer, based on the count value in the system board's DMA controller.
POS 102 D6	local output	POS register 102 bit 6. User definable control signal.
ARB/-GNT	input	Arbitrate/-Grant. When high, indicates that bus arbitration is in progress. When low, indicates normal bus operation.
POS 102 D7	local output	POS register 102 bit 7. User definable control signal.
-LOCAL CHCK	local input	Local Channel Check. An input from on-board parity checking circuitry that indicates a serious error. On-board circuitry must also drive the Micro Channel -CHCK line. The 88C01 uses this input to control a required channel check indicator flag in the POS registers.
LA12	local output	Latched Address 12. Optional latched A12 output.
-READ	local output	Read. Driven low during the CMD active portion of a bus read cycle.
-WRITE	local output	Write. Driven low during the CMD active portion of a bus write cycle.

88C01 PIN DESCRIPTION (continued)

SIGNAL	TYPE	DESCRIPTION
-CS0	local output	Chip Select 0. Configurable latched address decode output. May be used for I/O devices or adapter EPROM.
MA22	local output	Memory Address 22. Optional high-order latched address bit for memory board designs.
-CS1	local output	Chip Select 1. Configurable latched address decode output. May be used for I/O devices. If DMA is used, the DMA device must use this chip select.
-CS2	local output	Chip Select 2. Configurable latched address decode output. May be used for I/O devices.
LA10	local output	Latched Address 10. Optional latched A10 output.
LA11	local output	Latched Address 11. Optional latched A11 output.
MA21	local output	Memory Address 21. Optional high-order latched address bit for memory board designs.
-CS3	local output	Chip Select 3. Configurable latched address decode output. May be used for I/O devices or memory.
LA11	local output	Latched Address 11. Optional latched A11 output.
-HBYTE ACCESS	input	A combination of the Micro Channel -SBHE signal OR'ed with the 88C01 -CD DS 16 signal. (Note: some earlier data sheets showed this pin as just -SBHE).
POS 102 D7	local output	POS register 102 bit 7. User definable control signal.
-BUFEN LBYTE	local output	Buffer Enable Low Byte. A low signal enables the board's low byte data buffer.
-BUFEN	local output	Buffer Enable. A low signal enables the data buffer. This signal is activated for both low and high bytes, and external decoding with -SBHE and A0 is necessary. This signal is selected when the -SBHE pin is redefined as POS 102 D7.
-BUFEN HBYTE	local output	Buffer Enable High Byte. A low signal enables the board's high byte data buffer.
POS 102 D6	local output	POS register 102 bit 6. User definable control signal.

88C01 Operating Conditions

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	-2.0	7.0	V
V_I	DC input voltage	-2.0	$V_{CC}+1.0$	V
T_{AMB}	Ambient temperature	-65	135	°C
P_D	Power dissipation	--	500	mW

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.75	5.25	V
V_I	DC input voltage	0	V_{CC}	V
T_A	Operating temperature	0	70	°C

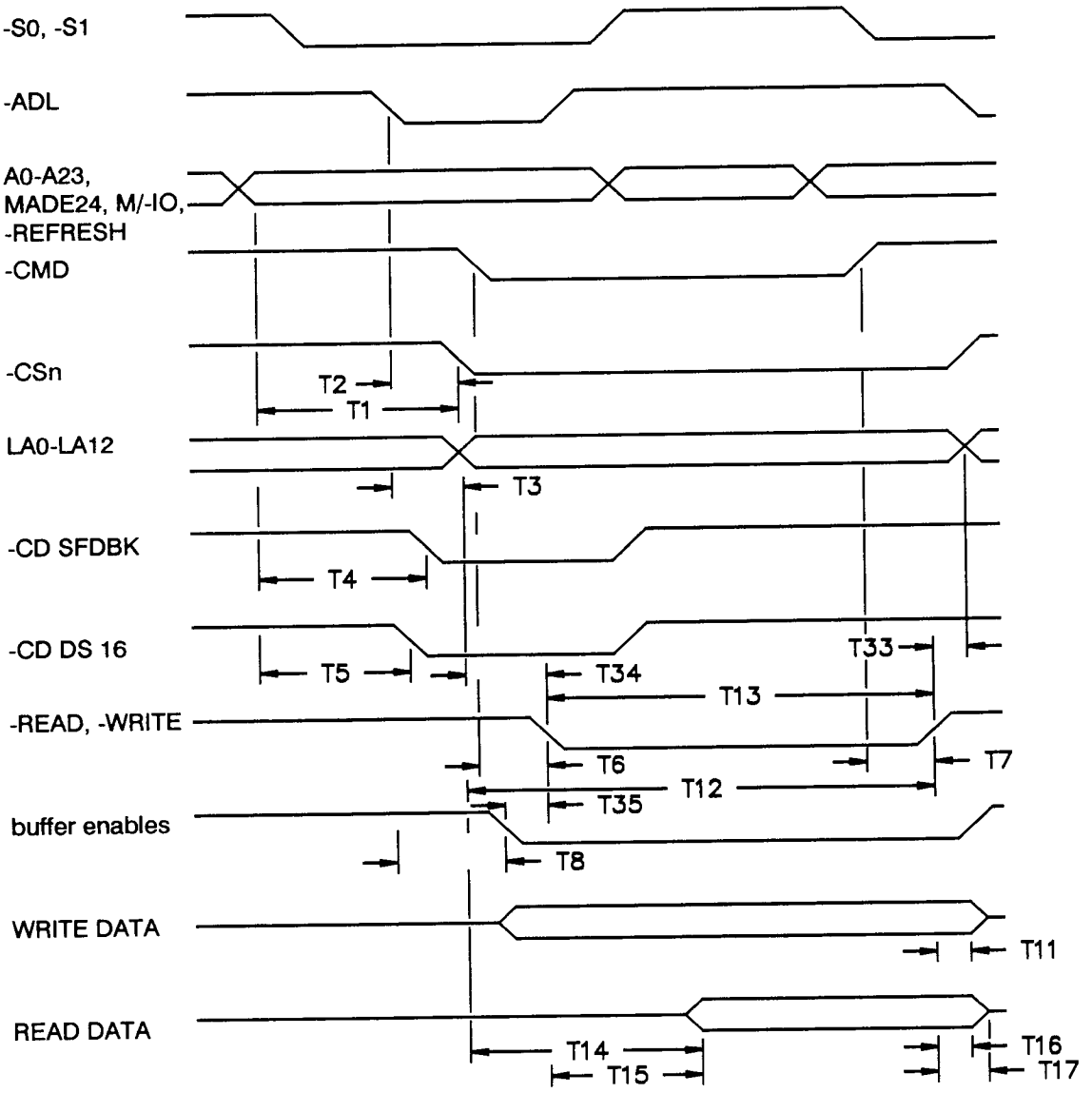
DC Characteristics (V_{CC} = 5V +/-5%, T_A = 0-70°C)

Symbol	Parameter	Min	Max	Unit
V_{IH}	HIGH level input voltage	2.0	--	V
V_{IL}	LOW level input voltage	--	0.8	V
V_{OH}	HIGH level output voltage	2.4	--	V
V_{OL}	LOW level output voltage	--	0.5	V
I_{CC}	V_{CC} supply current	--	90	mA
I_{OL}	Output drive current (low)	--	note 1	mA
I_{OH}	Output drive current (high)	--	2.0	mA

Notes:

1. All outputs can sink 12 mA, except: (LA12, D0-D7, user POS bits, DMAACK = 4 mA), (-PREEMPT, -BURST, ARB0-ARB3 = 24 mA)
2. The 88C01 is implemented in 1.5 micron CMOS, with TTL input and output buffers.

88C01 Default Cycle Timing



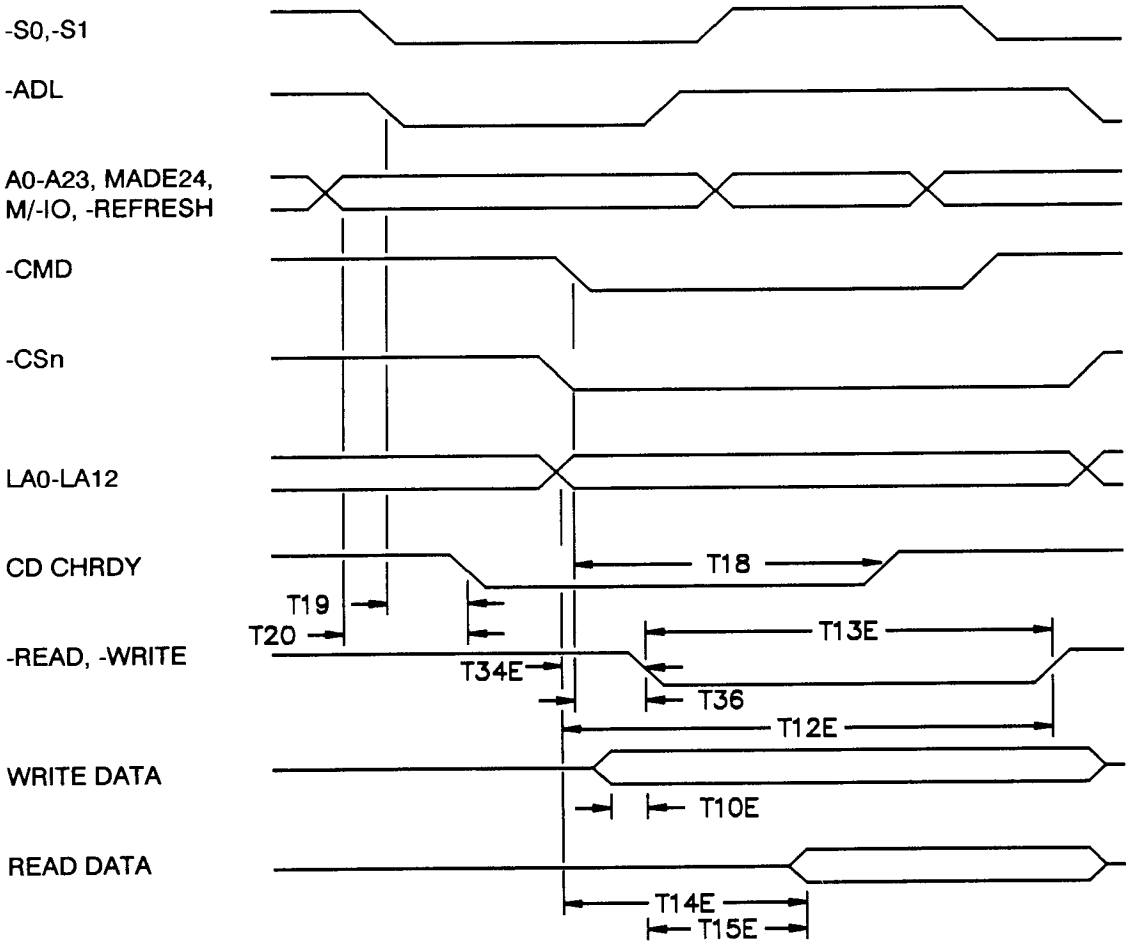
Default Cycle Timing (V_{CC} = 5V +/-5%, T_A = 0-70°C)

	Parameter	Min/Max (nsec)	
T1	Address valid to -CSn	-/60	
T2	-ADL to -CSn	-/35	
T3	-ADL to latched address outputs valid	-/45	note 3
T4	Address valid to -CD SFDBK	-/60	
T5	Address valid to -CD DS 16	-/55	
T6	-CMD active to -READ or -WRITE active	5/25	
T7	-CMD inactive to -READ or -WRITE inactive	5/20	
T8	-ADL to buffer enable active	-/25	
	Derived Parameters		note 4
T11	-WRITE inactive to WRITE DATA invalid (hold)	10 + m/-	note 5
T12	Latched address out valid to -WRITE inactive (write access)	90/-	
T13	-READ or -WRITE pulse width	80/-	
T14	Latched address out valid to READ DATA valid (read access)	-/55	
T15	-READ active to READ DATA valid	-/35	
T16	-READ inactive to READ DATA invalid (hold)	0/-	
T17	buffer enable inactive to READ DATA tristate	-/30	
T33	Latched address hold from -READ or -WRITE inactive	40/-	
T34	Latched address setup to -READ or -WRITE active	10/-	
T35	buffer enable active to -READ or -WRITE active	40/-	

Notes:

1. The 88C01 assumes incoming Micro Channel signals meet the specs given in the IBM Technical Reference.
2. Output capacitance loading as specified in the IBM Technical Reference. Non-Micro Channel signals assume 50 pF loading.
3. I/O or ROM addresses only. Mapped memory address timing is in a separate table.
4. These values are derived from Micro Channel specifications combined with T1-T8.
5. m is the minimum delay through the adapter's data buffer. For the 74ALS245, m is 3 nsec. So T11 is 10 + m, or 13, nsec.
6. 88C01 signal delays for different outputs track each other. This means a worst case minimum value for one delay will never combine with a worst case maximum for another.

88C01 Extended Cycle Timing



Synchronous Extended Cycle Timing (Vcc = 5V +/-5%, T_A = 0-70°C)

	Parameter	Min/Max (nsec)
T18	-CMD active to CD CHRDY active	-/30
T19	Status active to CD CHRDY inactive	0/30
T20	Address valid to CD CHRDY inactive	-/60
	Derived Parameters	
T12E	Latched address out valid to -WRITE inactive (write access)	190/-
T13E	-READ or -WRITE pulse width	180/-
T14E	Latched address out valid to READ DATA valid (read access)	-/155
T15E	-READ active to READ DATA valid	-/135

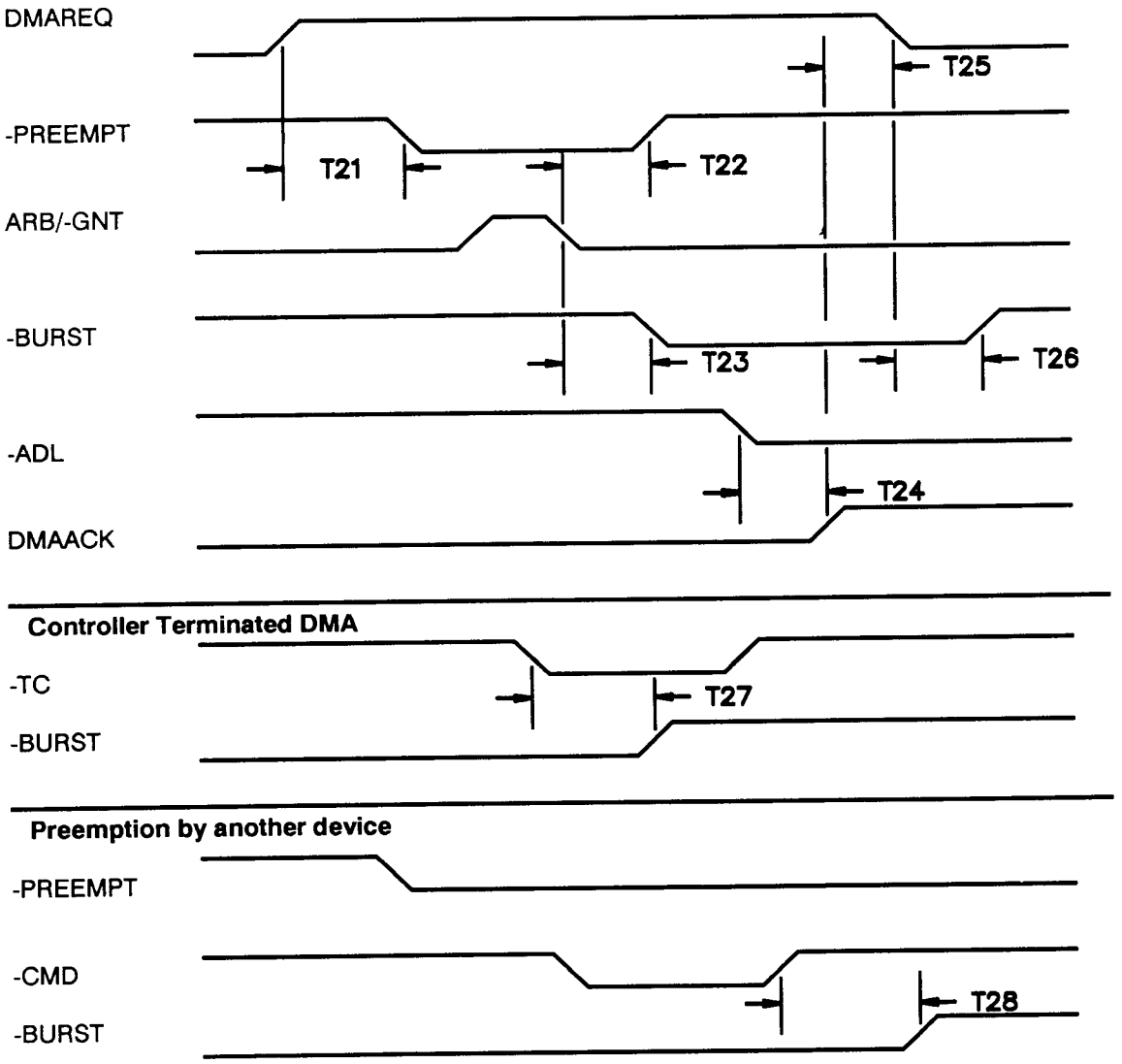
Asynchronous Extended Cycle Timing (Vcc = 5V +/-5%, T_A = 0-70°C)

	Parameter	Min/Max (nsec)
T18	-CMD active to CD CHRDY active	see note 1
T19	Status active to CD CHRDY inactive	0/30
T20	Address valid to CD CHRDY inactive	-/60
T36	-READ or -WRITE delay from -CMD active	see note 2
	Derived Parameters	
T10E	WRITE DATA valid to -WRITE active (setup)	T36-M/- note 4
T12E	Latched address out valid to -WRITE inactive (write access)	T18+90/-
T13E	-READ or -WRITE pulse width	see note 3
T14E	Latched address out valid to READ DATA valid (read access)	-/T18+55
T15E	-READ active to READ DATA valid	-/T18-T36+25
T34E	Latched address setup to -READ or -WRITE active (I/O only)	T36+10/-

Notes:

1. T18 can be any of the following configured minimum values: 210, 280, 350, 490, 770, or 1330 nsec.
2. T36 can be any of the following configured minimum values: 0, 10, 80, 150, or 220 nsec. Note: T36 only applies to I/O cycles! Memory cycles always use a zero delay.
3. If zero is selected for T36, then T13E is at least (T18+80) nsec. If T36 is non-zero, then T13E is at least (T18-T36 +55) nsec.
4. M is the maximum delay through the adapter's data buffer. For a 74F245, M is 8 nsec.

88C01 DMA Timing



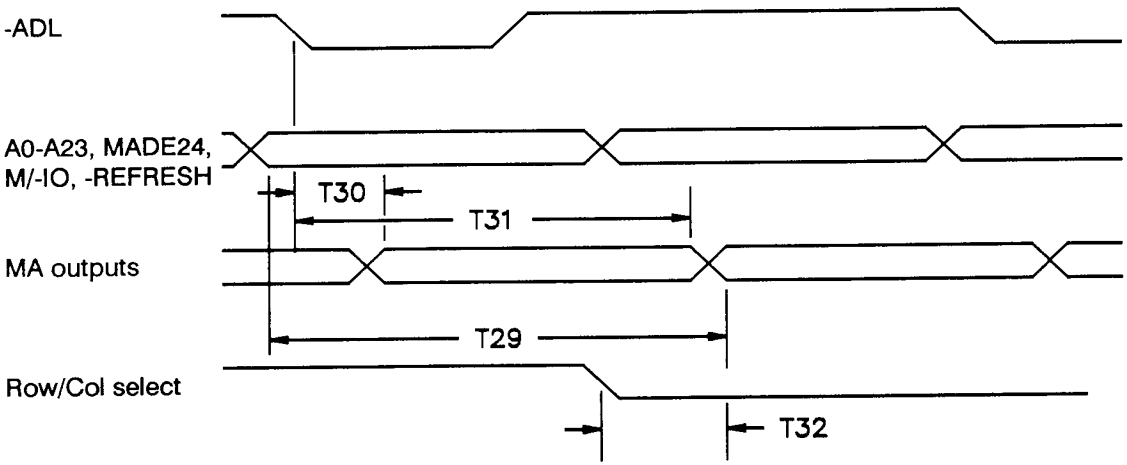
DMA Timing (V_{CC} = 5V +/-5%, T_A = 0-70°C)

	Parameter	Min/Max (nsec)	
T21	DMAREQ active to -PREEMPT active	-/60	note 1
T22	ARB/-GNT low (grant) to -PREEMPT inactive	0/50	note 2
T23	ARB/-GNT low (grant) to -BURST active	-/50	note 3
T24	-ADL active to DMAACK active	-/40	note 4
T25	DMAACK active to DMAREQ inactive	0/45	note 5
T26	DMAREQ inactive to -BURST inactive	-/35	note 6
T27	-TC active to -BURST inactive	-/30	
T28	-CMD inactive to -BURST inactive	-/40	note 7

Notes:

1. The polarity of the DMAREQ signal is configurable.
2. -PREEMPT is released only if the 88C01 wins the bus. Other boards may still hold -PREEMPT low.
3. -BURST is asserted only if the 88C01 wins the bus and burst mode is configured ON.
4. DMAACK is active only during the I/O portion of a DMA cycle pair. The polarity of the DMAACK signal is configurable. See Application Note #1, section on DMA devices.
5. Only applicable in burst mode. Adapter logic must respond within this time to guarantee that -BURST is released quickly enough. DMAREQ should be released when the cycle now beginning will use the last available adapter data.
6. Micro Channel timing requirements for synchronous or asychronous extended cycles will be met as long as T25 is met. 200 nsec default cycles would require releasing -BURST based on unlatched address and status signals, which are not made available to adapter logic. Thus, burst mode DMA should use at least a synchronous extended cycle.
7. -BURST is released when another adapter attempts to preempt the bus. By releasing -BURST after -CMD goes inactive, one more DMA cycle will occur before arbitration begins.

88C01 Mapped Memory Address Timing



Mapped Memory Address Timing (V_{CC} = 5V +/-5%, T_A = 0-70°C)

	Parameter	Min/Max (nsec)	
T29	Address valid to upper MA outputs valid	-/70	
T30	-ADL active to lower MA outputs valid	-/45	note 4
T31	-ADL active to upper MA outputs valid	-/45	
T32	Row/Col select low to upper MA outputs valid	7/35	note 4
	Derived Parameters	note 2	
	Default cycle: lower MA outputs valid to -WRITE inactive	85/-	
	Default cycle: lower MA outputs valid to READ DATA valid	-/55	
	Default cycle: lower MA outputs valid to -READ or -WRITE	10/-	
	Sync. ext. cycle: lower MA outputs valid to -WRITE inactive	185/-	
	Sync. ext. cycle: lower MA outputs valid to READ DATA valid	-/155	
	Sync. ext. cycle: lower MA outputs valid to -READ or -WRITE	10/-	
	Async. ext. cycle: lower MA outputs valid to -WRITE inactive	T18+85/-	note 3
	Async. ext. cycle: lower MA outputs valid to READ DATA valid	-/T18+55	
	Async. ext. cycle: lower MA outputs valid to -READ or -WRITE	T36+10/-	

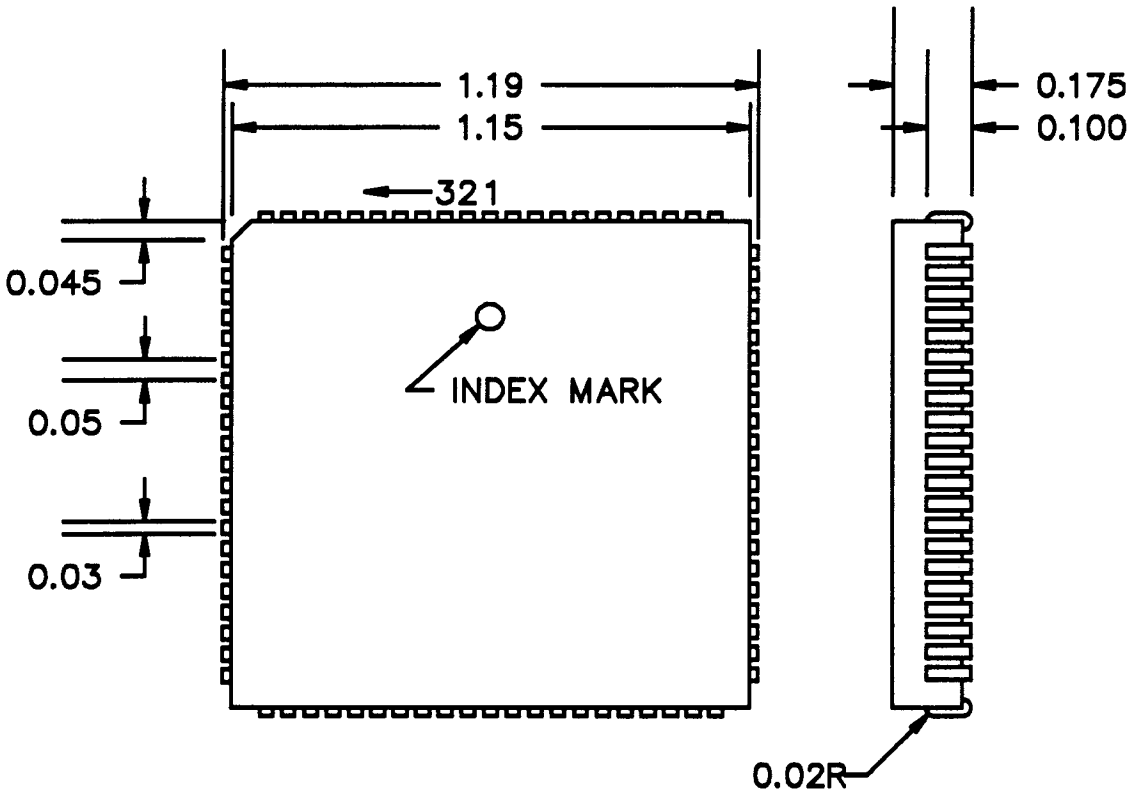
Notes:

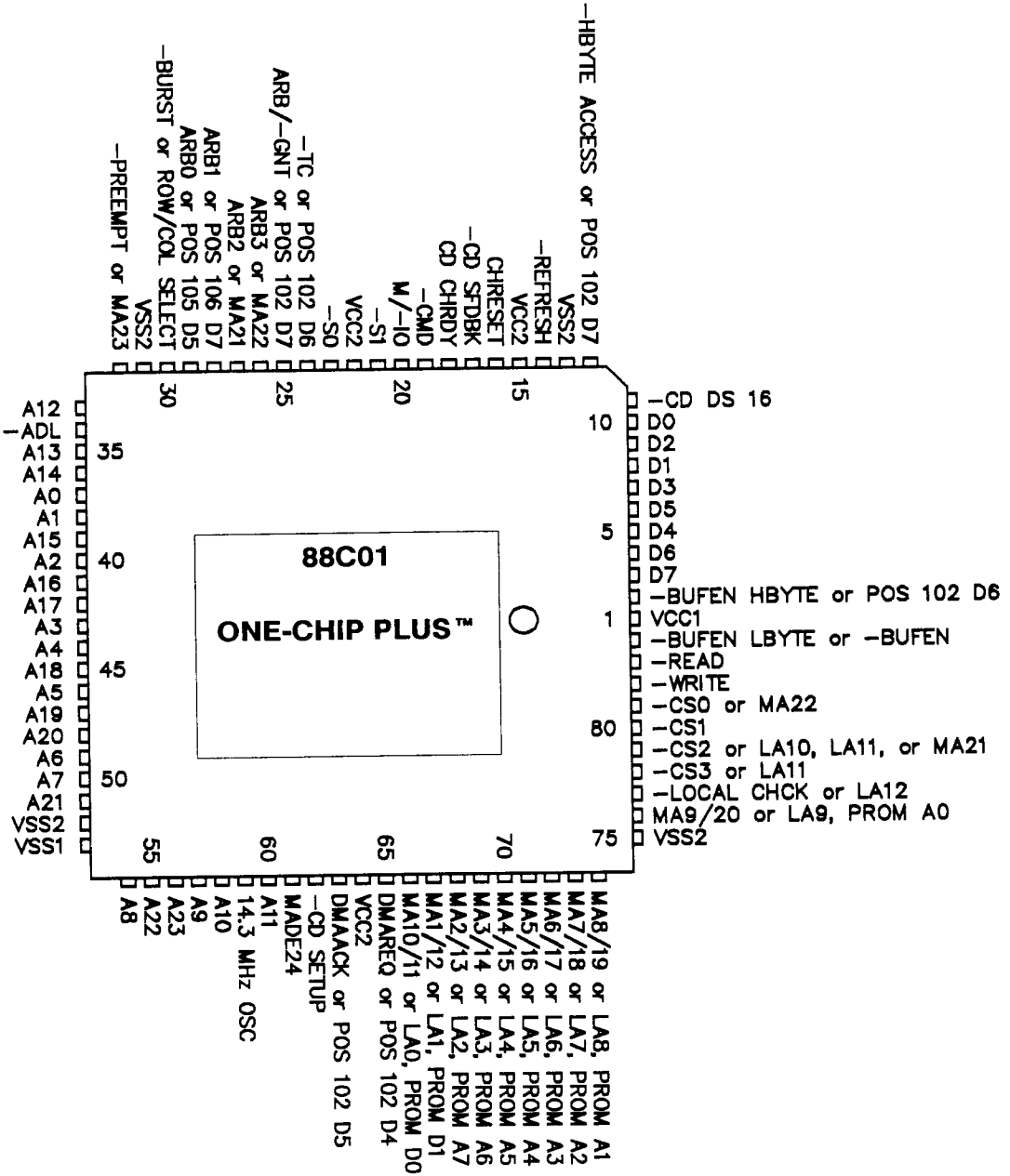
1. Row/Col select produces multiplexed memory address signals suitable for 1M DRAM chips. External circuitry must generate appropriate timing signals for the DRAMs (RAS and CAS) as well as the Row/Col select signal. 88C01 configuration can disable the multiplexor if external multiplexing is desired.
2. These times are derived from a combination of Micro Channel specifications and T29 to T32. Adapter logic must provide read data within the specified time.
3. See previous timing chart for T18 configurable choices.
4. The value given assumes a loading of 200 pF. This time includes a rise time of 12 nsec or a fall time of 6 nsec, which will scale with varying capacitive loading.

88C01 Configuration PROM contents

Bit #	Function when bit = 1
0-15	Micro Channel ID #
16	Use A10 for address outputs (for DRAM multiplexing), otherwise use A0
17	Disable row/col select
18	Choose low order address outputs (only used if row/col pin disabled)
19	ROM size: don't compare A13
20	ROM size: don't compare A14
21	ROM size: don't compare A15
22	Enable CS0 for ROM decoding
23-31	I/O CS0 decode: address compare value for A3,5,6,7,9,10,11,14,15
32	16 I/O locations for CS0
33	Enable CS0 for I/O decoding
34-42	I/O CS1 decode: address compare value for A3,5,6,7,9,10,11,14,15
43	16 I/O locations for CS1
44	Enable CS1 for I/O decoding
45	Enable I/O decoding for DMA enable register
46-54	I/O CS2 decode: address compare value for A3,5,6,7,9,10,11,14,15
55	16 I/O locations for CS2
56	Enable I/O decoding for CS2
57-65	I/O CS3 decode: address compare value for A3,5,6,7,9,10,11,14,15
66	16 I/O locations for CS3
67	Enable I/O decoding for CS3
68	Enable expanded/extended memory decoding for CS3
69-71	I/O CHRDY delay selection
72-74	Memory CHRDY delay selection
75	I/O CS1: 8 bit device
76	I/O CS0: 8 bit device
77	I/O CS2: 8 bit device
78	I/O CS3: 8 bit device
79	ROM: 8 bit device
80	Memory: 8 bit device
81	Select LA12 pin (otherwise -LOCAL CHCK)
82	Select -CS3 pin (otherwise LA11)
83-84	Select (83 is LSB): 00 = MA21, 01 = LA11, 10 = LA10, 11 = -CS2
85	Select -CS0 pin (otherwise MA22)
86	Select -SBHE and -BUFEN HBYTE signals (otherwise user POS bits)
88	Enable DMA function and pins
89	DMAACK polarity = HIGH (otherwise low)
91	Enable burst mode DMA
92	DMAREQ polarity = LOW (otherwise high)
93-95	-READ/-WRITE delay selection
87,90	(reserved)

88C01 Mechanical Specifications





88C01 PINOUT

Pin #	Function
1	VCC1
2	-BUFEN HBYTE or POS 102 D6
3-10	D7-D0 (Note order of pins)
11	-CD DS 16
12	-SBHE or POS 102 D7
13	VSS2
14	-REFRESH
15	VCC2
16	CHRESET
17	-CD SFDBK
18	CD CHRDY
19	-CMD
20	M/-IO
21	-S1
22	VCC2
23	-S0
24	-TC or POS 102 D6
25	ARB/-GNT or POS 102 D7
26	ARB3 or MA22
27	ARB2 or MA21
28	ARB1 or POS 106 D7
29	ARB0 or POS 105 D5
30	-BURST or ROW/COL SELECT
31	VSS2
32	-PREEMPT or MA23
33	A12
34	-ADL
35	A13
36	A14
37	A0
38	A1
39	A15
40	A2
41	A16
42	A17

Pin #	Function
43	A3
44	A4
45	A18
46	A5
47	A19
48	A20
49	A6
50	A7
51	A21
52	VSS2
53	VSS1
54	A8
55	A22
56	A23
57	A9
58	A10
59	14.3 MHz OSC
60	A11
61	MADE24
62	-CD SETUP
63	DMAACK or POS 102 D5
64	VCC2
65	DMAREQ or POS 102 D4
66-67	MAn or LAn, PROM D0-D1
68-74	MAn or LAn, PROM A7-A1
75	VSS2
76	MA9/20 or LA9, PROM A0
77	-LOCAL CHCK or LA12
78	-CS3 or LA11
79	-CS2 or LA10, LA11, or MA21
80	-CS1
81	-CS0 or MA22
82	-WRITE
83	-READ
84	-BUFEN LBYTE or -BUFEN

Note: VSS1 and VCC1 supply internal logic in the 88C01. VSS2 and VCC2 supply the input/output drivers.

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