VTC Inc.
Value the Customer™

VM5603

(1,7) ENCODER-DECODER WITH WRITE PRECOMPENSATION

PRELIMINARY

July, 1993

FEATURES

- (1,7) RLL Code
- Data Rates from 10 to 64 Mbits/sec
- Differential ECL Encoded Data and Clock
- Compatible with Zoned-Density Recording
- Programmable Write Precompensation
- Programmable Preamble Length Counted Before Decoder Enabled
- Designed to Operate with VM5351 Data Separator and VM5711 Reference Clock Generator
- Compatible with the AM95C95 Disk Data Controller
- Single Supply 5-Volt Operation
- Differential ECL Type Encoded Write Data Output
- Available in a 28-Lead PLCC Package
- The VM5603 Replaces the VM5602

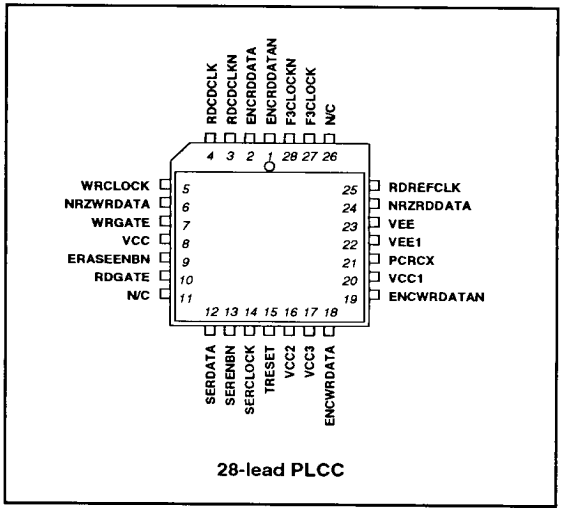
DESCRIPTION

The primary function of the VM5603 (1,7) ENDEC circuit is to encode and decode the 2/3 rate (1,7) Run Length Limited (RLL) modulation code used by the disk drive recording channel. In WRITE mode the device receives NRZ write data and a write clock from the drive controller and puts out (1,7) encoded data to be recorded on the disk media. In READ mode the device inputs (1,7) encoded read data and a code rate clock from the drive read channel and outputs NRZ read data and a read clock to the drive controller.

The device also provides programmable write precompensation (WPC). This adjusts the encoded write data bit to bit timing to help compensate for fixed head/media induced read time errors (bit shift). An erase function is provided to enable DC erasure during drive testing and formatting.

The device is designed to be compatible with the AM95C95 Disk Data Controller IC in SCSI drive interface applications. It is also designed to be ESDI compatible. It is intended to support hard sector formats only.

CONNECTION DIAGRAM



28-lead PLCC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage:
- V_{CC} (V_{EE} = 0) ..... 0V to 7.0V
- Ambient Operating Temperature ..... 0° to +70°C

Junction Operating Temperature ..... 0° to +130°C
Voltage Applied to TTL Inputs ..... -0.5V to V_{CC} +0.5V
Voltage Applied to ECL Inputs ..... 0V to V_{CC}
Storage Temperature ..... -55° to 150°C
Maximum Power Dissipation 650mW
Thermal Impedance Θ_{JA};
- 28-lead PLCC ..... 53°C/W

RECOMENDED OPERATING CONDITIONS

Supply Voltage:
- V_{CC} (V_{EE} = 0) ..... +4.5V to 5.5V

Junction Temperature ..... 25° to 125°C
Data Rate Frequency (RD REF CLK) ..... 10 to 64Mbits/sec
Write Precomp Full Scale Time Shift .....3.5 to 14ns

DATA RECOVERY CIRCUITS

WRITE DATA ENCODE

The write data encode function includes the WRITE CLOCK RE-SYNC, ENCODER, WRITE PRECOMP and WRITE DATA DRIVER blocks.

The write clock re-sync block receives TTL-level NRZ write data (NRZ WR DATA pin) and the write clock (WR CLOCK) pin from the drive controller. The drive controller uses the read reference clock (RD REF CLK) pin output from the VM5603 as a data rate reference to clock out NRZ write data. The RD REF CLK signal is returned as WR CLOCK by the controller. However, in an ESDI application RD REF CLK must also pass through an arbitrary cable delay before it is returned as WR CLOCK. This creates an unknown phase relationship between WR CLOCK, and RD REF CLK, its source. The purpose of the Write Clock Re-sync block is to automatically choose the appropriate internal WR CLOCK phase to reliably clock in NRZ WR DATA. This edge selection occurs upon each assertion of WR GATE.

The encoder block takes each pair of NRZ WR DATA bits and encodes them into three encoded write data (ENC WR DATA) bits according to the following code tables.

DATA	CODE
11	101
10	100
01	001
00	010

In instances where the above table produces code sequences which violate the (1,7) run length constraint, the following violation code table is invoked:

DATA	CODE
11 11	101 000
11 10	100 000
01 11	001 000
01 10	010 000

The MSB (left-most bit) is written/read first.

The NRZ WR DATA input must be held LO for 3 WR CLOCK periods after the assertion of WR GATE to allow internal clock edge selection (described above) and initialization of the encoder to a 3T code sequence (all zeros data). WR GATE must not be terminated prior to the completion of a write sequence. The WPC block receives encoded write data and outputs precompensated data according to the following bit sequence algorithm:

BIT SEQUENCE					COMPENSATION
N-2	N-1	N	N+2	N+2	(at time N)
1	0	1	0	1	none
0	0	1	0	0	none
1	0	1	0	0	early
0	0	1	0	1	late

The magnitude of the WPC time shift is controlled by the shift register block output bits: B_0, B_1, B_2. With all bits LO, no precompensation is employed. Seven timing values (binary sequence) can be programmed into the SHIFT REGISTER block, with all bits HI yielding the maximum or full scale time shift. The maximum shift is used when writing at lower data rates (inner zones on the disk). The minimum shift is used when writing at higher data rates (outer zones on the disk). The full scale time shift magnitude is set by an external capacitor and resistor tied from the PCRCX pin respectively to VCC and ground. This RC network sets-up a time constant whose slope determines the amount of WPC shift. The full scale time shift is adjusted externally by the capacitor, C_{EXT}, tied from the PCRCX pin to VCC. The capacitor value is related to the full scale time shift by the following expression:

$$C_{EXT} = (5.86)(t_{WPC})$$

C_{EXT} is in pF and t_{WPC} is the full scale time shift in ns. The capacitor C_{EXT} is relatively small, so, parasitic capacitances associated with the PCRCX pin should be minimized. An external resistor R_{EXT} is tied from the PCRCX pin to ground and set to 2kΩ for **all applications**. This resistor is necessary to balance the internal circuitry and for the WPC time constant. It must be used even if the WPC function is not. To turn off the WPC function and minimize any time shift due to parasitic capacitance, it is recommended to set all of the WPC bits (B0 - B2) to zero and remove the capacitor from the PCRCX pin.

The WRITE DATA DRIVER block inputs the encoded WPC data (ENC PR DATA) and translates it to a TTL level output; ENC WR DATA N. The ERASE ENB N input, when held LO, forces the ENC WR DATA N output HI regardless of the other device inputs. The input will float HI if left unconnected. The ENC WR DATA N output is held HI when WR GATE is inactive.

READ DATA DECODE

The read data decode function includes the Decoder, Data Clk Generator/Read Initialize, Shift Register and Read Data/ Ref Clk Driver blocks.

The DECODER block receives differential ECL-level encoded read data (ENC RD DATA, ENC RD DATA N) and a code rate clock (RD CD CLK, RD CD CLK N) from the drive read channel. On the assertion of read gate (RD GATE), the Data Clk Generator/Read Initialize block counts a programmed number of data clock periods to give the drive read channel PLL/Data Synchronizer time to lock to the read data. The number of data clock periods is set by bits B3 through B7 of the shift register block, which loads a programmable counter. The least significant bit, B3, counts four periods. The five bit binary counter provides a programmable count from 4 to 124 in steps of 4. All zeros loaded into the register puts the device in a special test mode such that the first clock edge of RD REF CLK gives VFOLKN assertion.

When the programmed count is reached, the Decoder begins receiving read data, looking for the first 010 010 code sequence which is the preamble PLL lock field pattern (all zeros NRZ data). When the pattern is detected, the Decoder is framed to the proper incoming read code phase, and 7 code clock cycles later, begins putting out decoded read data at

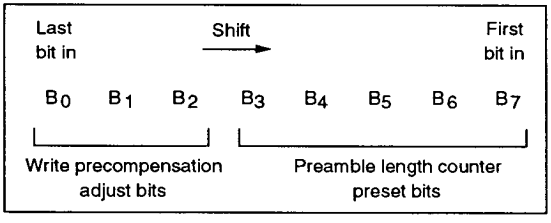
NRZ RD DATA. The NRZ RD DATA output has been held LO up to this time. The decode algorithm is the inverse of the coding algorithm specified in the coding table. Single-bit error propagation is 5 bits maximum.

The Data Clk Generator/Read Initialize block also receives differential ECL level 3F CLOCK, 3F CLOCK N signals from the drive read channel PLL/Data Synchronizer, This input must provide a data rate clock with a 50% duty cycle. The rising edge of 3F CLOCK must be synchronous with read code clock (RD CD CLK) and meet the timing constraints outlined in the AC characteristics section. The 3F CLOCK input is divided by 3, then output as RD REF CLK.

The Read Data/Ref Clk Driver block puts out TTL level NRZ RD DATA and RD REF CLK. It includes logic to hold the NRZ RD DATA output LO when RD GATE is inactive. The RD REF CLK output must be continuous when switching between operating modes with no more than two missing periods and no short duration glitches occurring at an interval less than one half a data rate period.

SHIFT REGISTER

The SHIFT REGISTER block is an eight bit DFF-type serial storage register. Data is shifted into the register via the SER DATA and SER CLOCK pins when the SER ENBN pin is true (LO). When the SER ENBN pin is HI, the SER DATA and SER CLOCK inputs are ignored. The serial register data is put out as bits B_0 through B_7. B_7 is the most significant bit and it is shifted into the serial register first.



Shift register code for programmable preamble length counter. Count = DATA CLK periods (RD REF CLK) from READ GATE assertion.

LSb B3	B4	B5	B6	MSb B7	Count
1	1	1	1	1	4
0	1	1	1	1	8
1	0	1	1	1	12
0	0	1	1	1	16
1	1	0	1	1	20
0	1	0	1	1	24
1	0	0	1	1	28
0	0	0	1	1	32
1	1	1	0	1	36
0	1	1	0	1	40
1	0	1	0	1	44
0	0	1	0	1	48
1	1	0	0	1	52
0	1	0	0	1	56
1	0	0	0	1	60
0	0	0	0	1	64
1	1	1	1	0	68
0	1	1	1	0	72
1	0	1	1	0	76
0	0	1	1	0	80
1	1	0	1	0	84
0	1	0	1	0	88
1	0	0	1	0	92
0	0	0	1	0	96
1	1	1	0	0	100
0	1	1	0	0	104
1	0	1	0	0	108
0	0	1	0	0	112
1	1	0	0	0	116
0	1	0	0	0	120
1	0	0	0	0	124
0	0	0	0	0	1st CLK edge of RD REF CLK gives VFOLKN High to Low

Shift register code for WPC magnitude.

LSb B0	B1	MSb B2	Write Precomp Magnitude
0	0	0	NONE
1	0	0	(1/7)FS
0	1	0	(2/7)FS
1	1	0	(3/7)FS
0	0	1	(4/7)FS
1	0	1	(5/7)FS
0	1	1	(6/7)FS
1	1	1	FS

PIN DESCRIPTIONS

INPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
ENC RD DATA N	1	Differential, ECL level encoded read data from the drive read channel PLL/Data Synchronizer.
ENC RD DATA	2	
RD CD CLK N	3	Differential, ECL level, code rate clock from the drive read channel PLL/Data Synchronizer. Used to clock in ENC RD DATA in read mode and used as a code rate reference clock in write mode.
RD CD CLK	4	
WR CLOCK	5	TTL level clock at the system data rate used to clock in NRZ WR DATA, active on rising edge.
NRZ WR DATA	6	TTL level NRZ write data from the drive controller, high-true.
WR GATE	7	TTL Level, high-true, input from the drive controller used to put the device in write (encode) mode.
ERASE ENB N	9	TTL level input which, when low, holds the EN WR DATA N output high regardless of the other device inputs, The pin has an internal resistor pull-up.

RD GATE 10 TTL level, high-true, input from the drive controller used to put the device in read (decode) mode.

SER DATA 12 TTL level data input to the shift register. High true data is clocked in using SER CLOCK. The MSB of the register word (B7) is clocked in first.

SER ENBN 13 TTL level shift enable and latch input. When low, it enables SER DATA to be clocked into the serial register using SER CLOCK. When high, the SER DATA and SER CLOCK inputs are ignored and the data existing in the serial register passes through a parallel set of transparent latches.

SER CLOCK 14 TTL level clock input to the shift register. The rising edge is used to clock in SER DATA.

TRESET 15 TTL active low pin used to reset the device for testing at VTC. Normally left open in application.

3F CLOCK 27
3F CLOCK N 28 A differential ECL level clock at three times the system data rate, active on the rising edge. This clock comes from the drive read channel PLL/Data Synchronizer. It is used to generate the RD REF CLK output.

OUTPUT PINS:

PIN NAME	PIN NO.	DESCRIPTION
ENC WR DATA	18	This pin is one side of a differential ECL output, with ENC WR DATA N being its complement. The rising edges are (1,7) encoded write data transitions to be recorded on the drive media. When WR GATE is not true, this output is held low.
ENC WR DATA N	19	This pin is a differential ECL output, with ENC WR DATA being its complement. The falling edges are (1,7) encoded write data transitions to be recorded on the drive media. When WR GATE is not true, this output is held high.
NRZ RD DATA	24	TTL level, high true, NRZ read data output to the drive controller. When RD GATE is not true, this output is held low. The output is also held low after the assertion of RD GATE for the duration of the internal programmable counter time.
RD REF CLK	25	TTL level clock output. In read mode it is used to clock NRZ RD DATA into the drive controller electronics. In write mode the driver controller uses it as a data rate reference clock to clock out NRZ WR DATA. The output runs continuously with no more than two missing clock pulses and no short duration glitches associated with mode changes.

ANALOG PINS:

PIN NAME	PIN NO.	DESCRIPTION
PCRCX	21	Used to set the WPC full scale time shift value with an external resistor to ground and external capacitor to VCC.

Note: C_{EXT} can range between 0 and 100pF. Care should be taken when choosing C_{EXT} at higher data rates such that the full scale time shift does not extend the window size. For example at 64Mbits/sec NRZ data rate, the RDCDCLK is 96MHz. This equates to a window size of 10.4ns. If a 100pF capacitor is used for C_{EXT}, then the full scale WPC shift would be 17.1ns and the shifted pulse would be lost.

POWER PINS:

PIN NAME	PIN NO.	DESCRIPTION
VCC	8	+5V supply for internal logic.
VCC1	20	+5V supply for TTL output buffers.
VCC2	16	+5V supply for analog functions.
VCC3	17	+5V supply for ECL output buffers.
VEE1	22	Ground for TTL output circuits.
VEE	23	Ground for internal logic and analog.

DC CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
TTL Inputs (Note 1)						
Voltage In High	V_{IH}		2.0			V
Voltage In Low	V_{IL}				0.8	V
Input Current High	I_{IH}	$V_{IN} = 2.7V$, $V_{CC} = 5.5V$			20	µA
Input Current High	I_{IH}	$V_{IN} = 6.0V$, $V_{CC} = 5.5V$			100	µA
Input Current Low	I_{IL}	$V_{IN} = 0.5V$, $V_{CC} = 5.5V$			-0.6	mA
Clamp Voltage	V_{IK}	Input Current = -18mA, $V_{CC} = 4.5V$			-1.2	V
TTL Outputs						
Voltage Output High	V_{OH}	$I_{OH} = -400µA$, $V_{CC} = 4.5V$	2.5			V
Voltage Output Low	V_{OL}	$I_{OL} = 4mA$, $V_{CC} = 4.5V$			0.4	V
Output Short Circuit Current	I_{OS}	(Note 3) $V_{CC} = 5.5V$	-20		-130	mA
ECL Inputs (Differential) (Notes 2 and 4)						
Voltage In	V_{IN}		V_{CC} - 2.3		V_{CC} - 0.3	V
Differential Input Voltage	V_{DIFF}		200			mV
Input Current	I_{IN}	$V_{CC} = 5.5V$, $V_{IN} = 3.1V$ to $5.3V$			25	µA
ECL Outputs (Differential) (Note 2)						
Voltage Output High	V_{OH}	$T_A = 0°C$	V_{CC} - 1.02		V_{CC} - 0.78	V
Voltage Output High	V_{OH}	$T_A = 25°C$	V_{CC} - 0.98		V_{CC} - 0.75	V
Voltage Output High	V_{OH}	$T_A = 70°C$	V_{CC} - 0.93		V_{CC} - 0.67	V
Voltage Output Low	V_{OL}	$0°C \le T_A < 70°C$	V_{CC} - 1.95		V_{CC} - 1.60	V
Power Supply Current	I_{CC}		50		120	mA

EXTERNAL COMPONENT SELECTION

COMPONENT	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
PCRCX Capacitor	C_{EXT}		0		100	pF
PCRCX Resistor	R_{EXT}		2.0		2.0	kΩ

CONTROL FUNCTION DELAYS

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
SER ENBN Pulse Width	t_{pwSERE}		20			ns
SER DATA Setup Time	t_{sSERD}		40			ns
SER DATA Hold Time	t_{hSERD}		0			ns
SER ENBN Setup Time	t_{sSERE}		40			ns
SER ENBN Hold Time	t_{hSERE}		40			ns
SER CLOCK Period	t_{SERC}		100			ns

Note 1: TTL inputs will float to a logic one if unconnected.
Note 2: All inputs and outputs denoted as ECL track with the V_{CC} supply voltage.
Note 3: Not more than one output shorted at one time duration of test not to exceed one second.
Note 4: DC test limits are specified after thermal equilbruium has been established. All ECL outputs are loaded with 50Ω to V_{CC} - 2.0V.

AC CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$, $R_{EXT} = 2k\Omega$.

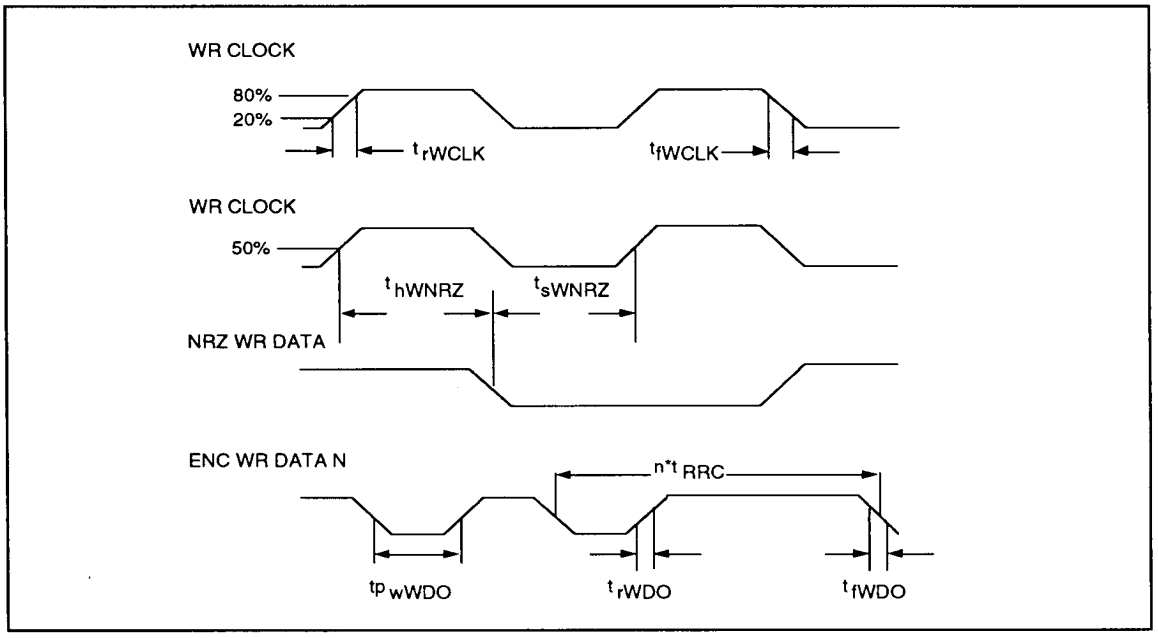
PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
NRZ WR DATA in Setup Time	t_{sWNRZ}			< 5		ns
NRZ WR DATA in Hold Time	t_{hWNRZ}			< 2		ns
WR CLOCK Duty Time	t_{dcWCLK}		35	50	65	%
ENC WR DATA N Output Propogation Delay from WR CLOCK Positive Edge	t_{pdWDO}	Note 5	13 * t_{RCC} +5ns		14 * t_{RCC} + 25ns	ns
ENC WR DATA/N Fall Time (C_{load} = 15pF)	t_{fWDO}			3.25		ns
ENC WR DATA/N Rise Time (C_{load} = 15pF)	t_{rWDO}			2.75		ns
ENC WR DATA/N Pulse Width	t_{pwWDO}	Note 5 (Precomp off: no C_{EXT})		t_{RCC}		ns
Full Scale WPC Time Shift	t_{WPC}		-15%	C_{EXT}/5.86	+15%	ns
WPC Time Shift Linearity	LIN (WPC)		-0.4		0.4	LSB
t_{WPC} Symmetry $\lvert t_{WPC}$ (early)$\rvert$ - $\lvert t_{WPC}$ (late)$\rvert$	SYM (WPC)		-0.5 * C_{EXT}/5.86	0	0.5 * C_{EXT}/5.86	ns

READ CHARACTERISTICS Unless otherwise specified, $V_{CC} = V_{CC1} = V_{CC2} = V_{CC3} = 5V \pm 10\%$, $T_A = 25°C$.

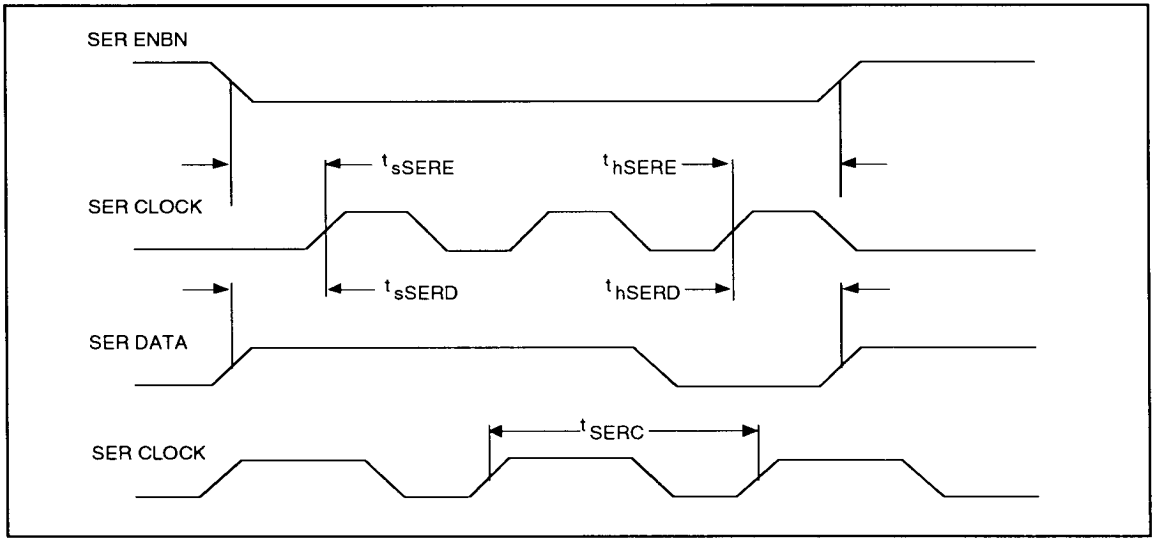
PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
ENC RD DATA in Setup Time	t_{sERD}			5		ns
ENC RD DATA in Hold Time	t_{hERD}			2		ns
RD CD CLK Duty Cycle	t_{dcRCC}		45		55	%
NRZ RD DATA Output Propogation Delay from RD CD CLK Positive Edge	t_{pdRNRZ}	Note 5	7 * t_{RCC} +5		8 * t_{RCC} +25	ns
RD REF CLK Output Fall Time (C_{load} = 15pF)	t_{rRRC}			3.25		ns
RD REF CLK Output Rise Time (C_{load} = 15pF)	t_{fRCC}			2.75		ns
NRZ RD DATA Output High Data Valid	$DVALID_{LH}$	Measured from RDREFCLK falling edge 1.5V threshold		3	5.75	ns
NRZ RD DATA Output Low Data Valid	$DVALID_{HL}$	Measured from RDREFCLK falling edge 1.5V threshold		2.7	4.55	ns
RD REF CLK Duty Cycle	t_{dcRRC}		40		60	%
3F CLOCK Delay Time	t_{d3FC}		3		6	ns
3F CLOCK Duty Cycle	t_{dc3FC}		40		60	%

Note 5: t_{RCC} is cycle time of Read Code Clock.

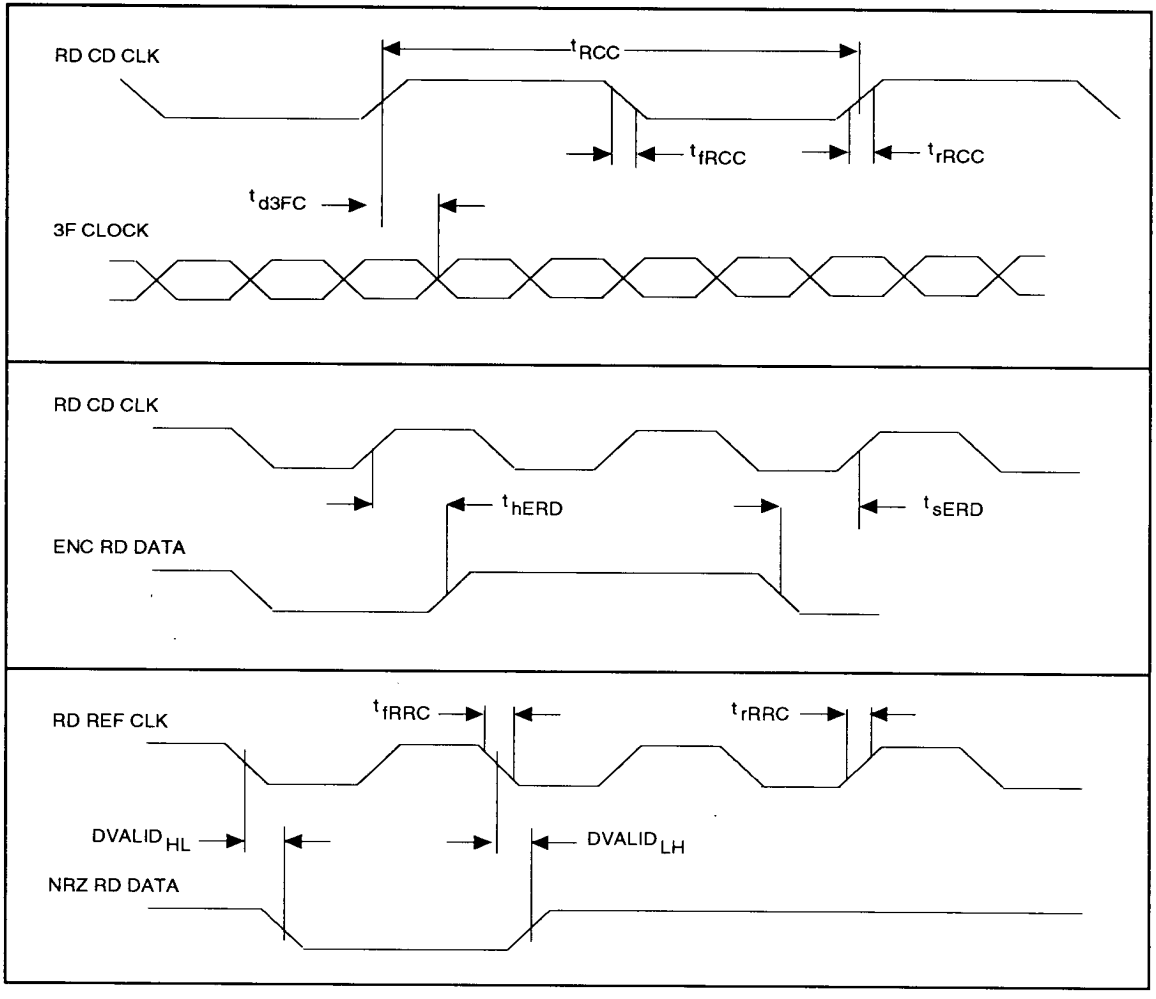
WRITE TIMING DIAGRAMS



CONTROL FUNCTION TIMING DIAGRAMS



READ TIMING DIAGRAMS



VM5603 BLOCK DIAGRAM