VITESSE

Product Preview

VSP947

High Performance Pentium™ Processor Cache Controller for Multiprocessor Systems

FEATURES

- Optimizes Pentium™ Processor Performance
- Zero Wait States -- 1+1+1+1 Pipelined Bursting Read & Write or 2+1+1+1 Non-Pipelined Bursting Read & Write Cycles
- 66-MHz Operation with Migration Path to 80-MHz
- Cache Sizes: 512 KB, 1 MB, 2 MB, and 4 MB
- Uses Standard Asynch-SRAMs for Tag Entries
- Low Power/High Integration Solution
- Copy Back to Reduce Bus Traffic
- Byte Gathering to Reduce System Bus Traffic
- 8-Deep Write Back Buffer to Reduce Penalty for Cache Misses
- Snoop Filtering to Minimize CPU Interrupts
- Write Allocation to Increase Cache Hit Rate
- MESI Protocol for Data Consistency
- Cache to Cache Transfers
- TTL Compatible Inputs and Outputs or GTL Interface
- +5, +2 Volt or +3.3, +2 Volt Power Supplies
- Incorporates Logic to Test Tag SRAM, and JTAG for the Chip

FUNCTIONAL DESCRIPTION

Vitesse's VSP947 is a high performance serial cache controller specifically designed for use in multiprocessor systems based on the Intel Pentium™ processor or overdrive processor. The VSP947 is intended to be used in conjunction with the VSP948 Datapath Chip, also from Vitesse. The complete chipset provides all of the control functions necessary to implement a second-level copy-back cache sub-system up to 4-MByte in size.

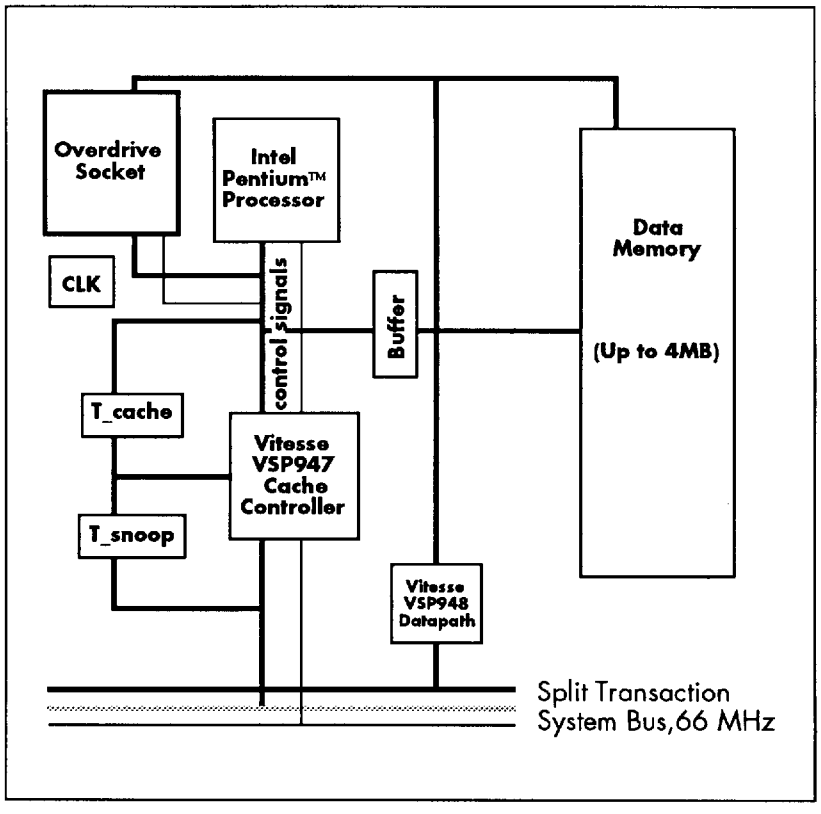
The high speed VSP947 permits the system designer to use standard asynchronous SRAMs for tag entries, and standard burst SRAM for data storage, while allowing the µprocessors to run at full speed (zero-wait-states). The VSP947 integrates all cache management functions for bus arbitration between the processors and the system bus. In addition, the VSP947 provides bursting read and write on both the CPU bus and the system bus, as well as providing an advanced bus snooping mechanism. A 8-deep write back buffer supports zero-wait-state operation on the write-miss cycle as well as supporting concurrent copy-back & write allocation. The chip is configured to allow the designer to specify 512 KB to 4-MByte cache sizes with 32- or 64–byte line sizes.

In addition to controlling the address and tag data directly, the VSP947 interfaces with the VSP948 Datapath Chip to provide control for data and parity on the processor bus. The VSP948 Datapath Chip provides a buffer function for the datapath between the system and processor.

The system bus is a split transaction bus with up to 66 MHz performance. The bus will provide 500 MB/s sustained data throughput.

The VSP947 provides the highest system performance and greatest scalability at the lowest cost. For 66 MHz multiprocessor systems, the VSP947 cache controller is the best solution and Vitesse has a clearly defined roadmap for system upgrades to 80 MHz and beyond.

1-MBYTE CACHE SIMPLIFIED SYSTEM DIAGRAM (66-MHz)



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