

NUP4304MR6

Advance Information

Low Capacitance Diode Array for ESD Protection in Four Data Lines

NUP4304MR6 is a MicroIntegration™ device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

Features

- Low Capacitance (1.5 pF Maximum Between I/O Lines)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
Machine Model = Class C
Human Body Model = Class 3B
- Protection for IEC61000-4-2 (Level 4)
8.0 kV (Contact)
15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground

Applications

- USB 1.1 and 2.0 Data Line Protection
- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I²C Bus Protection

MAXIMUM RATINGS (Each Diode) (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V _R	70	Vdc
Forward Current	I _F	200	mAdc
Peak Forward Surge Current	I _{FM(surge)}	500	mAdc
Repetitive Peak Reverse Voltage	V _{R RM}	70	V
Average Rectified Forward Current (Note 1) (averaged over any 20 ms period)	I _{F(AV)}	715	mA
Repetitive Peak Forward Current	I _{FRM}	450	mA
Non-Repetitive Peak Forward Current t = 1.0 μs t = 1.0 ms t = 1.0 S	I _{FSM}	2.0 1.0 0.5	A

1. FR-5 = 1.0 × 0.75 × 0.062 in.

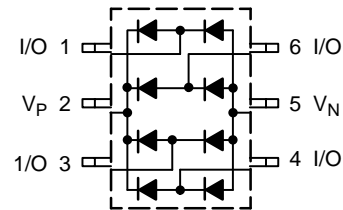
This document contains information on a new product. Specifications and information herein are subject to change without notice.



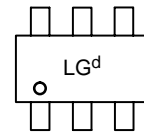
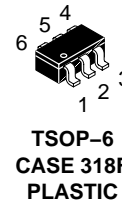
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PIN CONFIGURATION AND SCHEMATIC



MARKING DIAGRAM



LG = Specific Device Code
d = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NUP4304MR6	TSOP-6	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	556	°C/W
Lead Solder Temperature Maximum 10 Seconds Duration	T_L	260	°C
Junction Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (Each Diode)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Reverse Breakdown Voltage ($I_{(BR)} = 100 \mu\text{A}$)	$V_{(BR)}$	70	-	-	Vdc
Reverse Voltage Leakage Current ($V_R = 70 \text{ Vdc}$) ($V_R = 25 \text{ Vdc}$, $T_J = 150^\circ\text{C}$) ($V_R = 70 \text{ Vdc}$, $T_J = 150^\circ\text{C}$)	I_R	-	-	2.5 30 50	μA_{dc}
Capacitance (between I/O pins) ($V_R = 0 \text{ V}$, $f = 1.0 \text{ MHz}$)	C_D	-	0.8	1.5	pF
Capacitance (between I/O pin and ground) ($V_R = 0 \text{ V}$, $f = 1.0 \text{ MHz}$)	C_D	-	1.6	3	pF
Forward Voltage ($I_F = 1.0 \text{ mA}_{dc}$) ($I_F = 10 \text{ mA}_{dc}$) ($I_F = 50 \text{ mA}_{dc}$) ($I_F = 150 \text{ mA}_{dc}$)	V_F	-	-	715 855 1000 1250	mV_{dc}

1. FR-5 = $1.0 \times 0.75 \times 0.062 \text{ in.}$

2. Alumina = $0.4 \times 0.3 \times 0.024 \text{ in. 99.5\% alumina.}$

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Curves Applicable to Each Cathode

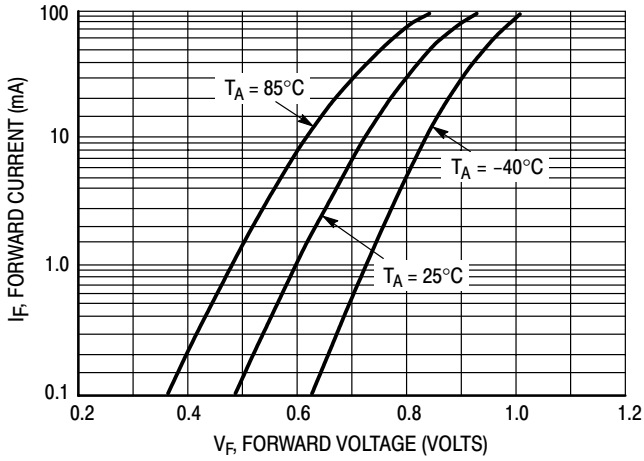


Figure 1. Forward Voltage

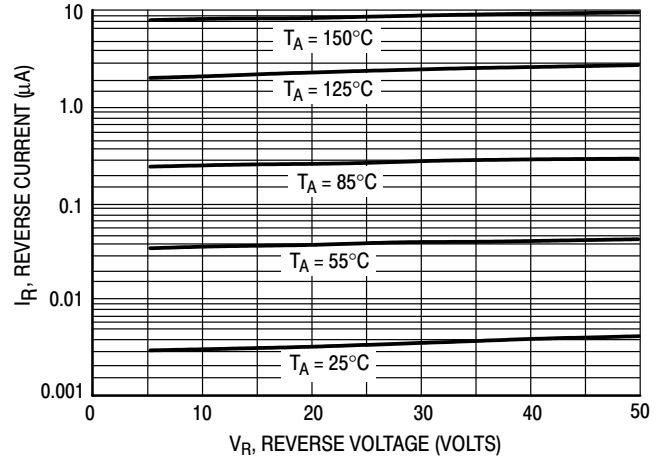


Figure 2. Leakage Current

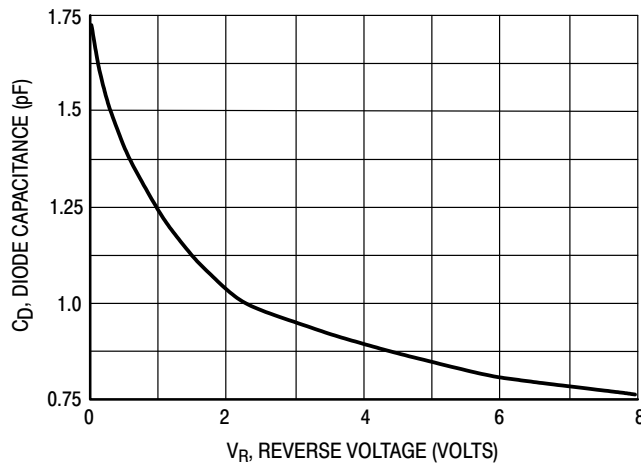
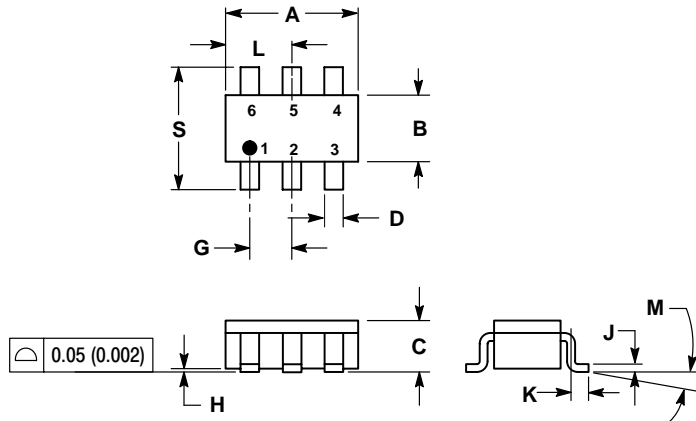


Figure 3. Capacitance

NUP4304MR6

PACKAGE DIMENSIONS

TSOP-6
CASE 318F-05
ISSUE K




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F-01, -02, -03 OBSOLETE. NEW STANDARD 318F-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1142	0.1220	2.90	3.10
B	0.0512	0.0669	1.30	1.70
C	0.0354	0.0433	0.90	1.10
D	0.0098	0.0197	0.25	0.50
G	0.0335	0.0413	0.85	1.05
H	0.0005	0.0040	0.013	0.100
J	0.0040	0.0102	0.10	0.26
K	0.0079	0.0236	0.20	0.60
L	0.0493	0.0649	1.25	1.65
M	0°	10°	0°	10°
S	0.0985	0.1181	2.50	3.00

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