



# STS2DPF20V

## DUAL P-CHANNEL 20V - 0.14Ω - 2A SO-8 2.7V-DRIVE STripFET™ II POWER MOSFET

PRELIMINARY DATA

| TYPE       | V <sub>DSS</sub> | R <sub>DS(on)</sub>              | I <sub>D</sub> |
|------------|------------------|----------------------------------|----------------|
| STS2DPF20V | 20 V             | <0.20Ω (@4.5V)<br><0.25Ω (@2.7V) | 2 A            |

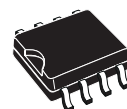
- TYPICAL R<sub>DS(on)</sub> = 0.14Ω (@4.5V)
- TYPICAL R<sub>DS(on)</sub> = 0.2Ω (@2.7V)
- ULTRA LOW THRESHOLD GATE DRIVE (2.7V)
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY

### DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

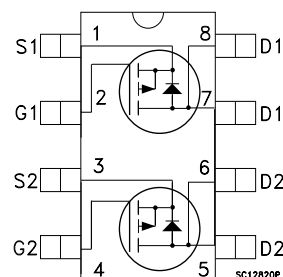
### APPLICATIONS

- BATTERY MANAGMENT IN NOMADIC EQUIPMENT
- POWER MANAGMENT IN CELLULAR PHONES



SO-8

### INTERNAL SCHEMATIC DIAGRAM



### MOSFET ABSOLUTE MAXIMUM RATINGS

| Symbol              | Parameter                                                                                                                                   | Value     | Unit   |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------|
| V <sub>DS</sub>     | Drain-source Voltage (V <sub>GS</sub> = 0)                                                                                                  | 20        | V      |
| V <sub>DGR</sub>    | Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)                                                                                                | 20        | V      |
| V <sub>GS</sub>     | Gate- source Voltage                                                                                                                        | ± 12      | V      |
| I <sub>D</sub>      | Drain Current (continuos) at T <sub>C</sub> = 25°C Single Operation<br>Drain Current (continuos) at T <sub>C</sub> = 100°C Single Operation | 2<br>1.26 | A<br>A |
| I <sub>DM</sub> (●) | Drain Current (pulsed)                                                                                                                      | 8         | A      |
| P <sub>TOT</sub>    | Total Dissipation at T <sub>C</sub> = 25°C Dual Operation<br>Total Dissipation at T <sub>C</sub> = 25°C Single Operation                    | 1.6<br>2  | W<br>W |

(●)Pulse width limited by safe operating area.

Note: For the P-CHANNEL MOSFET actual polarity of Voltages and current has to be reversed

## STS2DPF20V

### THERMAL DATA

|                  |                                                                                         |            |              |
|------------------|-----------------------------------------------------------------------------------------|------------|--------------|
| Rthj-amb         | (*)Thermal Resistance Junction-ambient Single Operation<br>Dual Operation               | 62.5<br>78 | °C/W<br>°C/W |
| T <sub>stg</sub> | Storage Temperature                                                                     | -55 to 150 | °C           |
| T <sub>j</sub>   | Junction-ambient Temperature<br>(*) When Mounted on 0.5 in <sup>2</sup> of 2 oz. Copper | -55 to 150 | °C           |

### MOSFET ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

| Symbol               | Parameter                                             | Test Conditions                                                                       | Min. | Typ. | Max.    | Unit     |
|----------------------|-------------------------------------------------------|---------------------------------------------------------------------------------------|------|------|---------|----------|
| V <sub>(BR)DSS</sub> | Drain-source Breakdown Voltage                        | I <sub>D</sub> = 250 µA, V <sub>GS</sub> = 0                                          | 20   |      |         | V        |
| I <sub>DSS</sub>     | Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0) | V <sub>DS</sub> = Max Rating<br>V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C |      |      | 1<br>10 | µA<br>µA |
| I <sub>GSS</sub>     | Gate-body Leakage Current (V <sub>DS</sub> = 0)       | V <sub>GS</sub> = ± 12 V                                                              |      |      | ±100    | nA       |

### ON (1)

| Symbol              | Parameter                         | Test Conditions                                                                                | Min. | Typ.         | Max.         | Unit   |
|---------------------|-----------------------------------|------------------------------------------------------------------------------------------------|------|--------------|--------------|--------|
| V <sub>GS(th)</sub> | Gate Threshold Voltage            | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA                                     | 0.6  |              |              | V      |
| R <sub>DS(on)</sub> | Static Drain-source On Resistance | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1 A<br>V <sub>GS</sub> = 2.7 V, I <sub>D</sub> = 1 A |      | 0.14<br>0.20 | 0.20<br>0.25 | Ω<br>Ω |

### DYNAMIC

| Symbol              | Parameter                    | Test Conditions                                       | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------|-------------------------------------------------------|------|------|------|------|
| g <sub>fs</sub> (1) | Forward Transconductance     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.5 A        |      | 4.5  |      | S    |
| C <sub>iss</sub>    | Input Capacitance            | V <sub>DS</sub> = 15V, f = 1 MHz, V <sub>GS</sub> = 0 |      | 315  |      | pF   |
| C <sub>oss</sub>    | Output Capacitance           |                                                       |      | 87   |      | pF   |
| C <sub>rss</sub>    | Reverse Transfer Capacitance |                                                       |      | 17   |      | pF   |

**ELECTRICAL CHARACTERISTICS (CONTINUED)****SWITCHING ON**

| Symbol      | Parameter          | Test Conditions                                                                                          | Min. | Typ. | Max. | Unit |
|-------------|--------------------|----------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD} = 10\text{ V}$ , $I_D = 1.5\text{ A}$                                                            |      | 38   |      | ns   |
| $t_r$       | Rise Time          | $R_G = 4.7\Omega$ , $V_{GS} = 4.5\text{ V}$<br>(see test circuit, Figure 1)                              |      | 30   |      | ns   |
| $Q_g$       | Total Gate Charge  | $V_{DD} = 10\text{ V}$ , $I_D = 2\text{ A}$ ,<br>$V_{GS} = 4.5\text{ V}$<br>(see test circuit, Figure 2) |      | 3.8  | 4.8  | nC   |
| $Q_{gs}$    | Gate-Source Charge |                                                                                                          |      | 0.34 |      | nC   |
| $Q_{gd}$    | Gate-Drain Charge  |                                                                                                          |      | 0.8  |      | nC   |

**SWITCHING OFF**

| Symbol       | Parameter           | Test Conditions                                                                                                              | Min. | Typ. | Max. | Unit |
|--------------|---------------------|------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(off)}$ | Turn-off Delay Time | $V_{DD} = 10\text{ V}$ , $I_D = 1\text{ A}$ ,<br>$R_G = 4.7\Omega$ , $V_{GS} = 4.5\text{ V}$<br>(see test circuit, Figure 1) |      | 45   |      | ns   |
| $t_f$        | Fall Time           |                                                                                                                              |      | 11   |      | ns   |

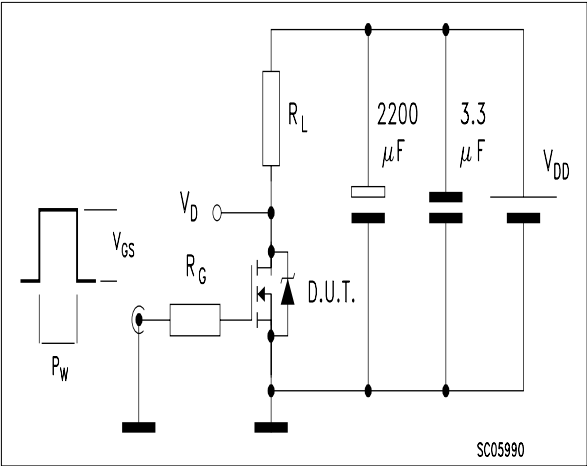
**SOURCE DRAIN DIODE**

| Symbol        | Parameter                     | Test Conditions                                                                                                                                    | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $I_{SD}$      | Source-drain Current          |                                                                                                                                                    |      |      | 2    | A    |
| $I_{SDM} (2)$ | Source-drain Current (pulsed) |                                                                                                                                                    |      |      | 8    | A    |
| $V_{SD} (1)$  | Forward On Voltage            | $I_{SD} = 2\text{ A}$ , $V_{GS} = 0$                                                                                                               |      |      | 1.2  | V    |
| $t_{rr}$      | Reverse Recovery Time         | $I_{SD} = 2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 10\text{ V}$ , $T_j = 150^\circ\text{C}$<br>(see test circuit, Figure 3) |      | 15   |      | ns   |
| $Q_{rr}$      | Reverse Recovery Charge       |                                                                                                                                                    |      | 7.5  |      | nC   |
| $I_{RRM}$     | Reverse Recovery Current      |                                                                                                                                                    |      | 1    |      | A    |

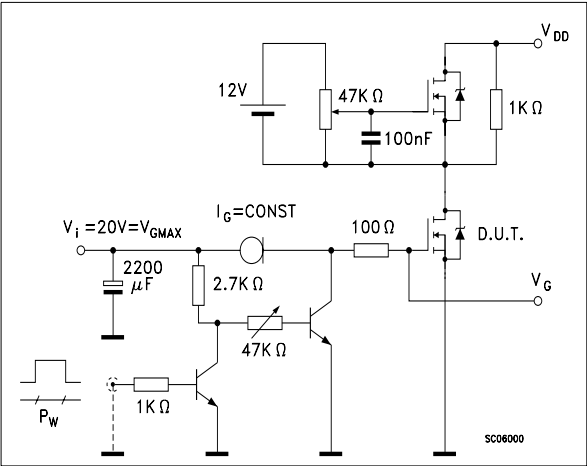
Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

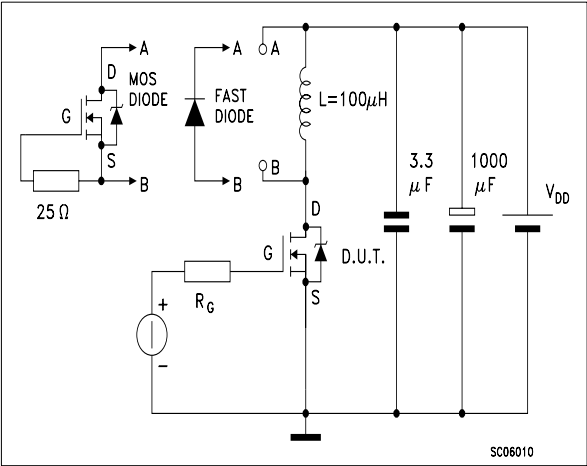
**Fig. 1:** Switching Times Test Circuit For Resistive Load



**Fig. 2:** Gate Charge test Circuit

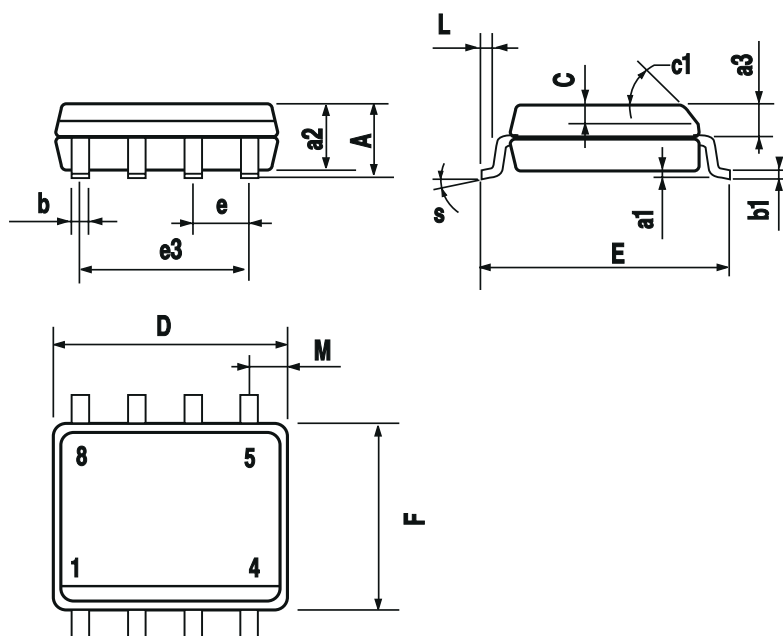


**Fig. 3:** Test Circuit For Diode Recovery Behaviour



## SO-8 MECHANICAL DATA

| DIM. | mm        |      |      | inch  |       |       |
|------|-----------|------|------|-------|-------|-------|
|      | MIN.      | TYP. | MAX. | MIN.  | TYP.  | MAX.  |
| A    |           |      | 1.75 |       |       | 0.068 |
| a1   | 0.1       |      | 0.25 | 0.003 |       | 0.009 |
| a2   |           |      | 1.65 |       |       | 0.064 |
| a3   | 0.65      |      | 0.85 | 0.025 |       | 0.033 |
| b    | 0.35      |      | 0.48 | 0.013 |       | 0.018 |
| b1   | 0.19      |      | 0.25 | 0.007 |       | 0.010 |
| C    | 0.25      |      | 0.5  | 0.010 |       | 0.019 |
| c1   | 45 (typ.) |      |      |       |       |       |
| D    | 4.8       |      | 5.0  | 0.188 |       | 0.196 |
| E    | 5.8       |      | 6.2  | 0.228 |       | 0.244 |
| e    |           | 1.27 |      |       | 0.050 |       |
| e3   |           | 3.81 |      |       | 0.150 |       |
| F    | 3.8       |      | 4.0  | 0.14  |       | 0.157 |
| L    | 0.4       |      | 1.27 | 0.015 |       | 0.050 |
| M    |           |      | 0.6  |       |       | 0.023 |
| S    | 8 (max.)  |      |      |       |       |       |



0016023

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -  
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>