793.723

93C06/46

256 Bit/1K 5.0V CMOS Serial EEPROM

FEATURES

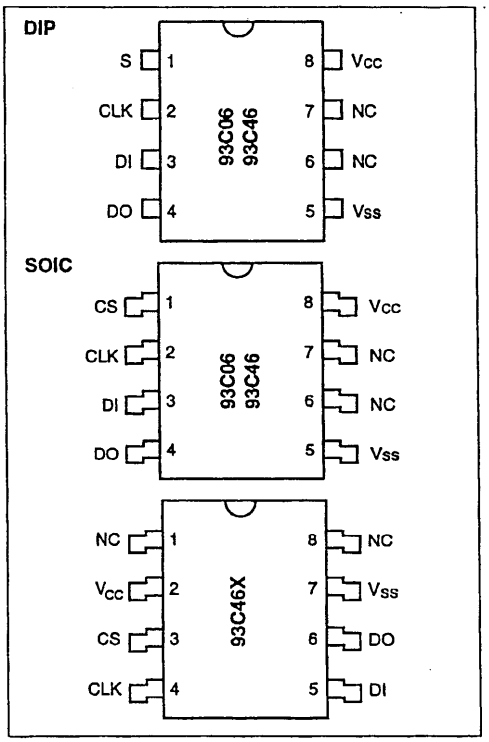
- Low power CMOS technology
- 16 bit memory organization
  - 6 x 16 bit organization (93C06)
  - 64 x 16 bit organization (93C46)
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- **1,000,000 ERASE/WRITE cycles guaranteed**
- Data Retention > 40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C
- 2 ms program cycle time

DESCRIPTION

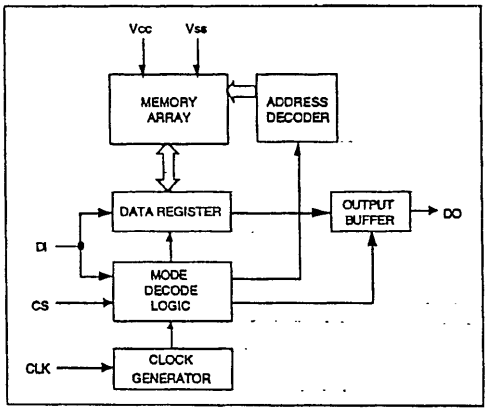
The Microchip Technology Inc. 93C06/46 family of Serial Electrically Erasable PROMs are configured in a x16 organization. Advanced CMOS technology makes these devices ideal for low-power non-volatile memory applications. The 93C06/46 is available in the standard 8-pin DIP and surface mount SOIC packages. The 93C46X comes as SOIC only.

These devices offer fast (1 ms) byte write and extended (-40°C to +125°C) temperature operation. It is recommended that all other applications use Microchip's 93LC46.

PACKAGE TYPE



BLOCK DIAGRAM



4

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V

All inputs and outputs w.r.t. Vss.....-0.6V to Vcc +1.0V

Storage temperature.....-65°C to +150°C

Ambient temperature with power applied .-65°C to +125C

Soldering temperature of leads (10 seconds).....+300°C

ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
Vss	Ground
NC	No Connect; No Internal Connection
Vcc	+5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

Vcc = +5V (±10%)			Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Automotive: Tamb = -40°C to +125°C (Note 3)		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Vcc detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4	—	V	IOH = -400 µA
Low level output voltage	VOL	—	0.4	V	IOL = 3.2 mA
Input leakage current	ILI	—	10	µA	VIN = 0V to Vcc (Note 1)
Output leakage current	ILO	—	10	µA	VOUT = 0V to Vcc (Note 1)
Internal capacitance (all inputs/outputs)	CINT	—	7	pF	VIN/VOUT = 0V (Note 2) Tamb = +25°C, f = 1 MHz
Operating current (all modes)	Icc write	—	4	mA	FCLK = 1 MHz, Vcc = 5.5V
Standby current	Iccs	—	100	µA	CS = 0V, Vcc = 5.5V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.
Note 3: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

FIGURE 1-1: SYNCHRONOUS DATA TIMING

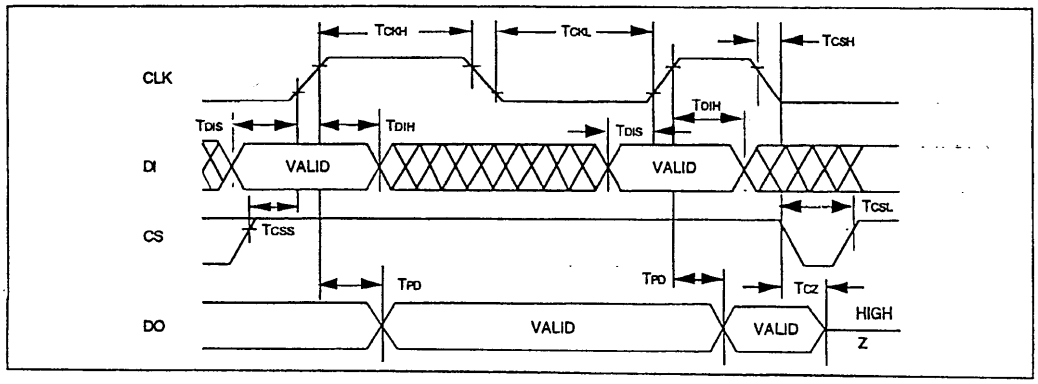


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500	—	ns	
Clock low time	TCKL	500	—	ns	
Chip select setup time	TCSS	50	—	ns	
Chip select6 hold time	TCSH	0	—	ns	
Chip select low time	TCSL	100	—	ns	
Data input setup time	TDIS	100	—	ns	
Data input hold time	TDIH	100	—	ns	
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV	—	100	ns	CL = 100 pF
Program cycle time (Auto Erase and Write)	TWC	—	2 15	ms ms	For ERAL and WRAL
Erase cycle time	TEC	—	1	ms	

4

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C06/46. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status. (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition, the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become "Don't Care" inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

2.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) from the falling edge of the CLK which clocked in the last DI bit (D0 for WRITE, A0 for ERASE) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during Erase and Write cycles if the READY/$\overline{\text{BUSY}}$ status information is outputted by the 93C06/46.

INSTRUCTION SET - 93C06

Instruction	Start BIT	Opcode OP1 OP2	Address	Number of Data In	Data Out	Req. CLK Cycles
READ	1	1 0	0 0 A3 A2 A1 A0	—	D15 - D0	25
WRITE	1	0 1	0 0 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
ERASE	1	1 1	0 0 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	9
EWEN	1	0 0	1 1 X X X X	—	High-Z	9
EWDS	1	0 0	0 0 X X X X	—	High-Z	9
ERAL	1	0 0	1 0 X X X X	—	(RDY/$\overline{\text{BSY}}$)	9
WRAL	1	0 0	0 1 X X X X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25

INSTRUCTION SET - 93C46

Instruction	Start BIT	Opcode OP1 OP2	Address	Number of Data In	Data Out	Req. CLK Cycles
READ	1	1 0	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
WRITE	1	0 1	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
ERASE	1	1 1	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	9
EWEN	1	0 0	1 1 X X X X	—	High-Z	9
EWDS	1	0 0	0 0 X X X X	—	High-Z	9
ERAL	1	0 0	1 0 X X X X	—	(RDY/$\overline{\text{BSY}}$)	9
WRAL	1	0 0	0 1 X X X X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25

3.0 FUNCTIONAL DESCRIPTION

3.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

3.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

3.3 Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached 2.8V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below 2.8V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

3.4 READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the HIGH state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the low going edge of CS, which ever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).

3.5 WRITE Mode

The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first, followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the rising edge of the CLK for the last data bit (D0).

The WRITE cycle takes 2 ms maximum.

4

FIGURE 3-1: READ MODE

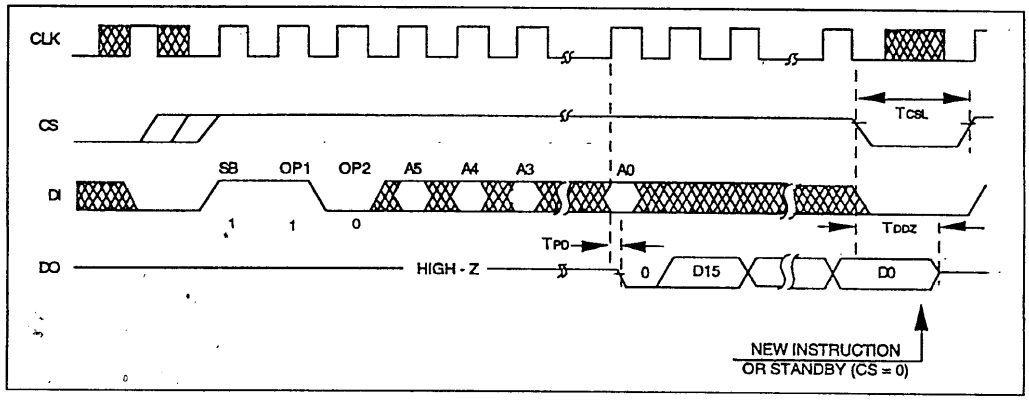
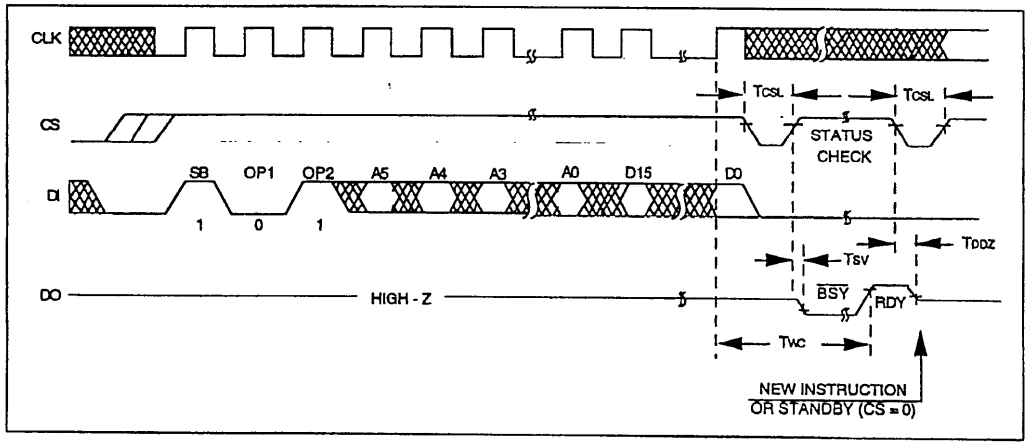


FIGURE 3-2: WRITE MODE

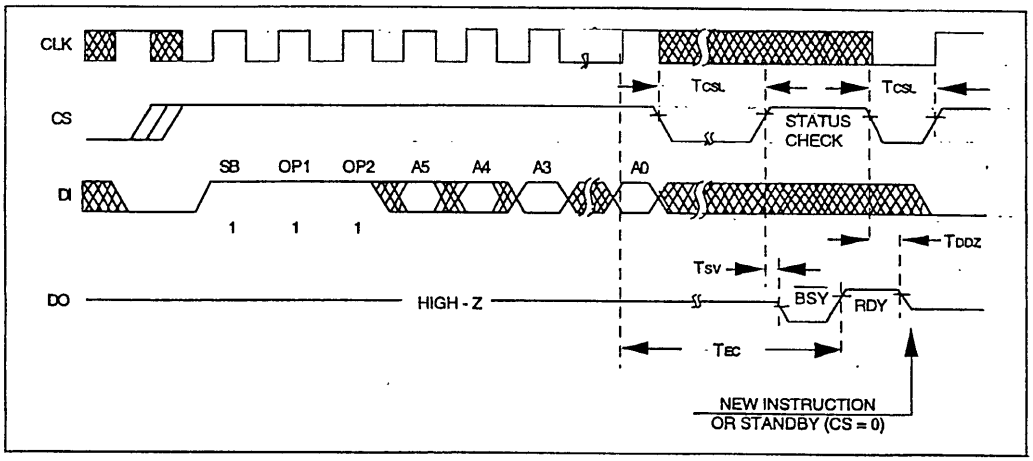


3.6 ERASE Mode

The ERASE instruction forces all the data bits of the specified address to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

The ERASE cycle takes 1 ms maximum.

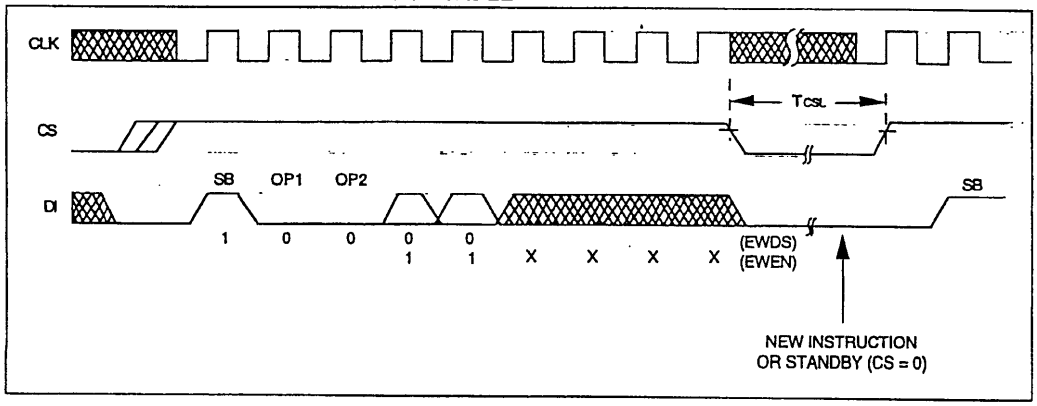
FIGURE 3-3: ERASE MODE



3.7 ERASE/WRITE Enable/Disable (EWEN, EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.

FIGURE 3-4: ERASE/WRITE ENABLE/DISABLE

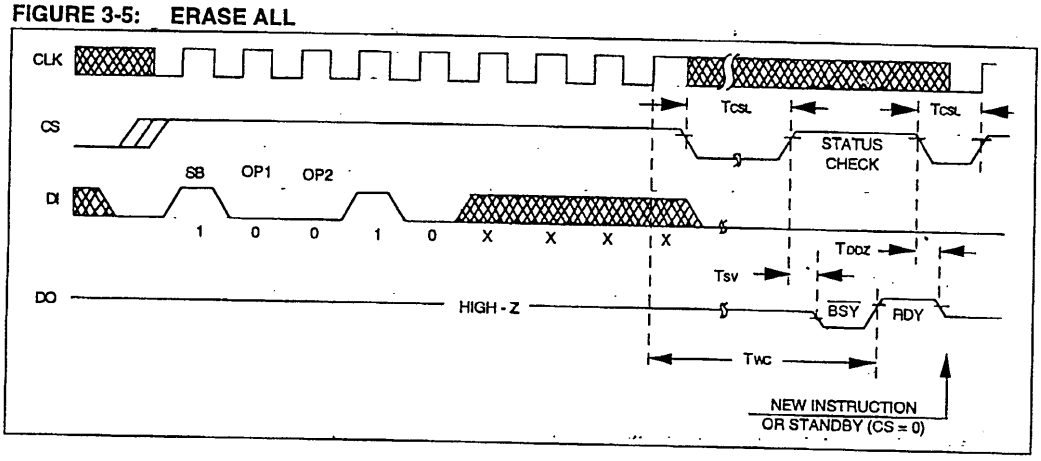


3.8 ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms maximum.

FIGURE 3-5: ERASE ALL



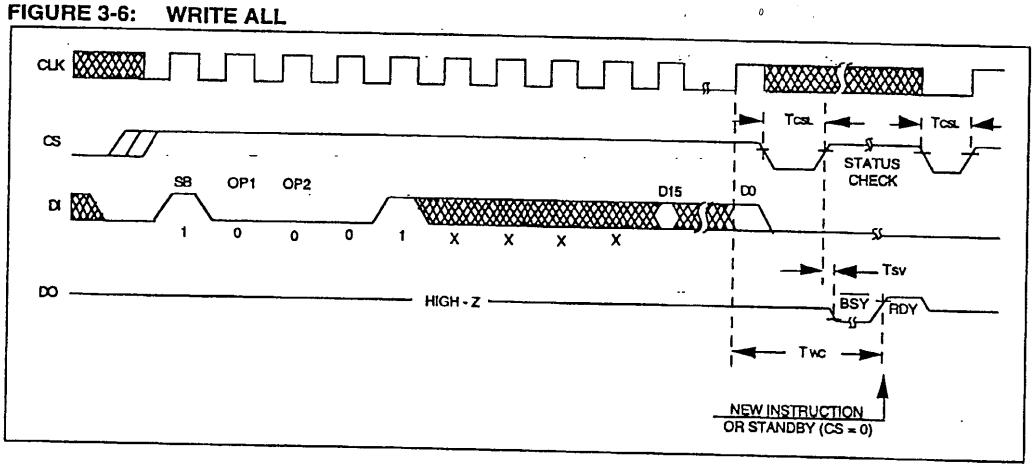
3.9 WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the rising edge of the CLK for the last data bit (DO). WRAL takes 15 ms maximum.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.

FIGURE 3-6: WRITE ALL



4

93C06/46 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

93C06/46 - /P

Package:	J	=	CERDIP (300 mil Body)
	P	=	Plastic DIP (300 mil Body)
	SN	=	Plastic SOIC (150 mil Body)
	SM	=	Plastic SOIC (207 mil Body)
Temperature Range:	Blank	=	0°C to +70°C
	I	=	-40°C to +85°C
	E	=	-40°C to +125°C

Device:	**Configuration**
93C06	256 bit CMOS Serial EEPROM
93C46	1K CMOS Serial EEPROM
93C46X	1K CMOS Serial EEPROM in alternate pinouts (SN package only)
93C06T	CMOS Serial EEPROM (Tape and Reel)
93C46T	CMOS Serial EEPROM (Tape and Reel)
93C46XT	CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.