

- Organization . . . 4194304 × 32
- Single 5-V Power Supply ($\pm 10\%$ Tolerance)
- 72-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets
- Utilizes Eight 16-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages
- Long Refresh Period
32 ms (2048 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Output
- Common $\overline{\text{CAS}}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks
- Enhanced Page Mode Operation With $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ (CBR), $\overline{\text{RAS}}$ -Only, and Hidden Refresh

- Presence Detect
- Performance Ranges:

| | ACCESS TIME | ACCESS TIME | ACCESS TIME | READ OR WRITE CYCLE (MIN) |
|--------------|------------------------|-----------------------|------------------------|---------------------------|
| | t _{RAC} (MAX) | t _{AA} (MAX) | t _{CAC} (MAX) | |
| '497BBK32-60 | 60 ns | 30 ns | 15 ns | 110 ns |
| '497BBK32-70 | 70 ns | 35 ns | 18 ns | 130 ns |
| '497BBK32-80 | 80 ns | 40 ns | 20 ns | 150 ns |

- Low Power Dissipation
- Operating Free-Air-Temperature Range
0°C to 70°C
- Gold-Tabbed Version Available:†
TM497BBK32
- Tin-Lead (Solder) Tabbed Version Available: TM497BBK32S

description

The TM497BBK32 is a 16M-byte dynamic random-access memory (DRAM) organized as four times 4194304 × 8 in a 72-pin leadless single-in-line memory module (SIMM). The SIMM is composed of eight TMS417400DJ, 4194304 × 4-bit DRAMs, each in 24/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. The TMS417400DJ is described in the TMS417400 data sheet.

The TM497BBK32 SIMM is available in the single-sided BK leadless module for use with sockets. The TM497BBK32 SIMM features $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

operation

The TM497BBK32 operates as eight TMS417400DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

refresh

The refresh period is extended to 32 ms and, during this period, each of the 2048 rows must be strobed with $\overline{\text{RAS}}$ in order to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

power up

To achieve proper operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{\text{RAS}}$ -only or CBR) cycle.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

TM497BBK32, TM497BBK32S

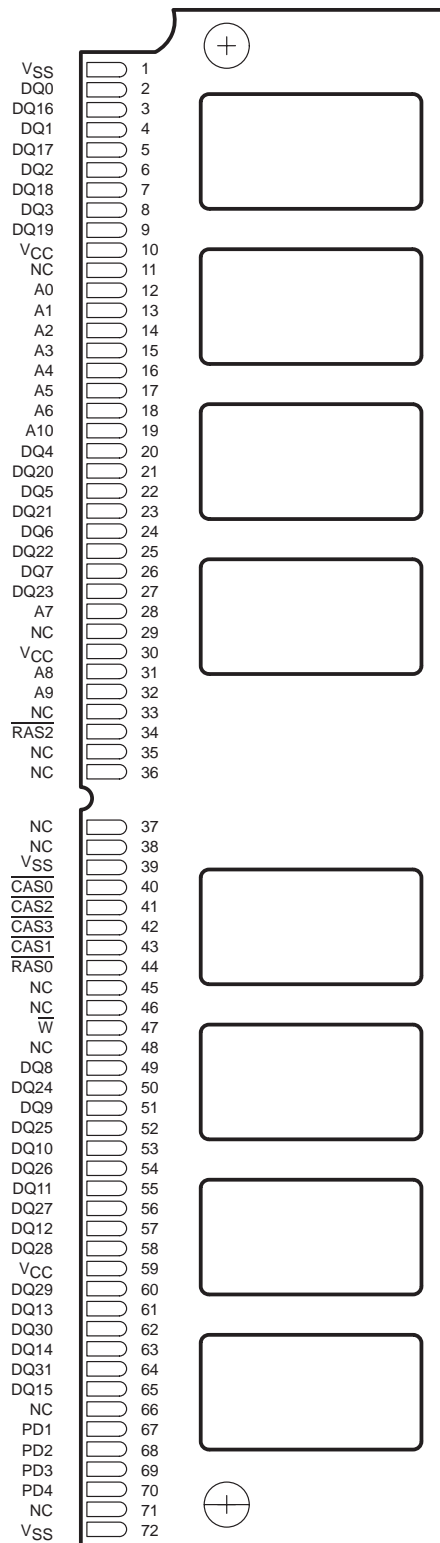
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DYNAMIC RAM MODULE

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BK SINGLE-IN-LINE PACKAGE

(TOP VIEW)



(SIDE VIEW)



PIN NOMENCLATURE

| | |
|------------|-----------------------|
| A0–A10 | Address Inputs |
| CAS0–CAS3 | Column-Address Strobe |
| DQ0–DQ31 | Data In/Data Out |
| NC | No Connection |
| PD1–PD4 | Presence Detects |
| RAS0, RAS2 | Row-Address Strobe |
| VCC | 5-V Supply |
| VSS | Ground |
| W | Write Enable |

PRESENCE DETECT

| | | PD1 (67) | PD2 (68) | PD3 (69) | PD4 (70) |
|------------|-------|-------------|-------------|-------------|-------------|
| TM497BBK32 | 80 ns | VSS | NC | NC | VSS |
| | 70 ns | VSS | NC | VSS | NC |
| | 60 ns | VSS | NC | NC | NC |

Table 1. Connection Table

| DATA BLOCK | RASx | CASx |
|------------|------|------|
| DQ0–DQ7 | RAS0 | CAS0 |
| DQ8–DQ15 | RAS0 | CAS1 |
| DQ16–DQ23 | RAS2 | CAS2 |
| DQ24–DQ31 | RAS2 | CAS3 |

single-in-line memory module and components

PC substrate: $1,27 \pm 0,1$ mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage

Bypass capacitors: Multilayer ceramic

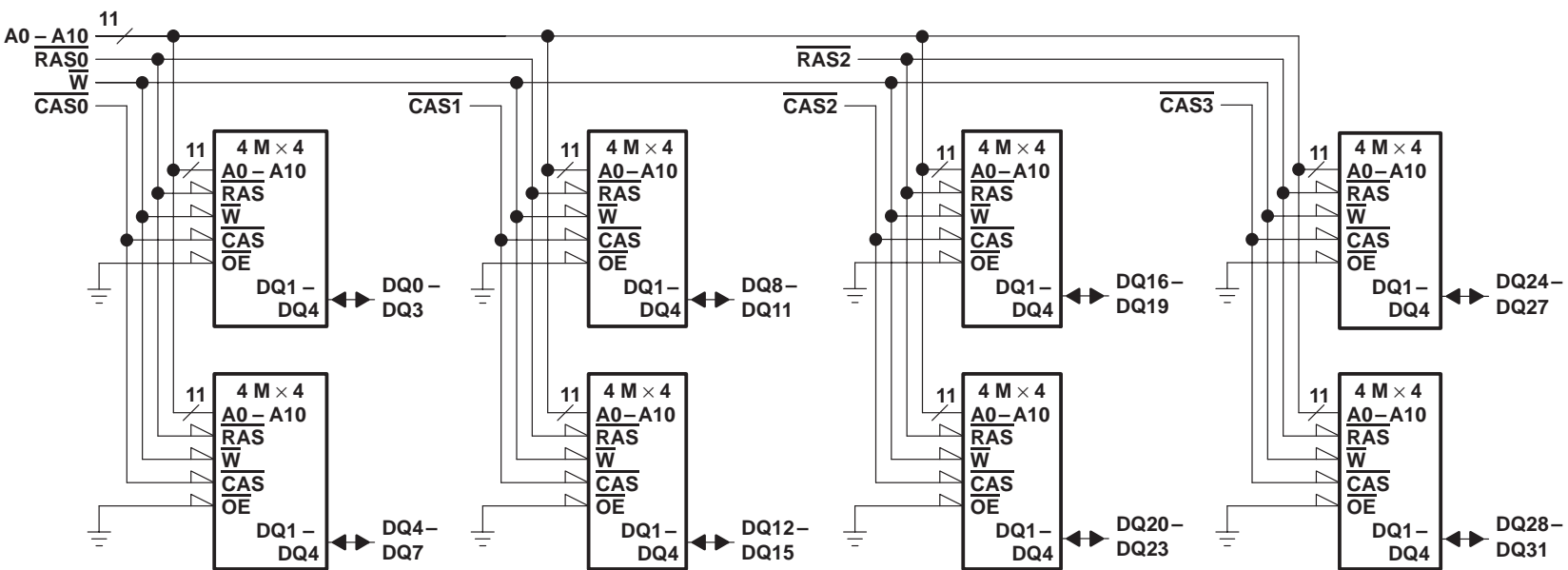
Contact area for TM497BBK32: Nickel plate and gold plate over copper

Contact area for TM497BBK32S: Nickel plate and tin-lead over copper

TM497BBK32, TM497BBK32S 4194304 BY 32-BIT DYNAMIC RAM MODULE

SMMS433B - JANUARY 1993 - REVISED JUNE 1995

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} (see Note 1) | – 1 V to 7 V |
| Voltage range on any pin (see Note 1) | – 1 V to 7 V |
| Short-circuit output current | 50 mA |
| Power dissipation | 8 W |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | – 55°C to 125°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|----------|--------------------------------------|-----|-----|-----|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2.4 | | 6.5 | V |
| V_{IL} | Low-level input voltage (see Note 2) | – 1 | | 0.8 | V |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | '497BBK32-60 | | '497BBK32-70 | | '497BBK32-80 | | UNIT |
|-----------|--|--|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V_{OH} | High-level output voltage | $I_{OH} = -5$ mA | | 2.4 | 2.4 | 2.4 | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 4.2$ mA | | 0.4 | | 0.4 | | V |
| I_I | Input current (leakage) | $V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All others = 0 V to V_{CC} | | ± 80 | | ± 80 | | µA |
| I_O | Output current (leakage) | $V_{CC} = 5.5$ V, $V_O = 0$ V to V_{CC} , CAS high | | ± 10 | | ± 10 | | µA |
| I_{CC1} | Read- or write-cycle current (see Note 3) | $V_{CC} = 5.5$ V, Minimum cycle | | 880 | 800 | 720 | | mA |
| I_{CC2} | Standby current | $V_{IH} = 2.4$ V (TTL), After 1 memory cycle, RAS and CAS high | | 16 | 16 | 16 | | mA |
| | | $V_{IH} = V_{CC} - 0.2$ V (CMOS), After 1 memory cycle, RAS and CAS high | | 8 | 8 | 8 | | mA |
| I_{CC3} | Average refresh current (RAS only or CBR) (see Note 3) | $V_{CC} = 5.5$ V, RAS cycling, (RAS only); CAS low (CBR) | | 880 | 800 | 720 | | mA |
| I_{CC4} | Average page current (see Note 4) | $V_{CC} = 5.5$ V, RAS low, $t_{PC} = \text{MIN}$, CAS cycling | | 560 | 480 | 400 | | mA |

‡ For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

- NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}} = V_{IL}$
4. Measured with a maximum of one address change while $\text{CAS} = V_{IH}$

TM497BBK32, TM497BBK32S

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SMMS433B – JANUARY 1993 – REVISED JUNE 1995

capacitance over recommended ranges of supply voltage and operating free-air temperature, $f = 1$ MHz (see Note 5)

| PARAMETER | | MIN | MAX | UNIT |
|-------------|--|-----|-----|------|
| $C_{i(A)}$ | Input capacitance, address inputs | | 40 | pF |
| $C_{i(R)}$ | Input capacitance, \overline{RAS} inputs | | 28 | pF |
| $C_{i(C)}$ | Input capacitance, \overline{CAS} inputs | | 14 | pF |
| $C_{i(W)}$ | Input capacitance, write-enable input | | 56 | pF |
| $C_{o(DQ)}$ | Output capacitance on DQ pins | | 7 | pF |

NOTE 5: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER | '497BBK32-60 | | '497BBK32-70 | | '497BBK32-80 | | UNIT | | |
|-----------|--|-----|--------------|-----|--------------|-----|------|----|----|
| | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| t_{AA} | Access time from column address | | 30 | | 35 | | 40 | ns | |
| t_{CAC} | Access time from \overline{CAS} low | | 15 | | 18 | | 20 | ns | |
| t_{CPA} | Access time from column precharge | | 35 | | 40 | | 45 | ns | |
| t_{RAC} | Access time from \overline{RAS} low | | 60 | | 70 | | 80 | ns | |
| t_{CLZ} | \overline{CAS} to output in low-impedance state | | 0 | | 0 | | 0 | ns | |
| t_{OH} | Output disable time from start of \overline{CAS} high | | 3 | | 3 | | 3 | ns | |
| t_{OFF} | Output disable time after \overline{CAS} high (see Note 6) | | 0 | | 15 | | 0 | 20 | ns |

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | '497BBK32-60 | | '497BBK32-70 | | '497BBK32-80 | | UNIT | | |
|------------|---|-----|--------------|-----|--------------|-----|------|---------|----|
| | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| t_{RC} | Cycle time, random read or write (see Note 7) | | 110 | | 130 | | 150 | ns | |
| t_{PC} | Cycle time, page-mode read or write (see Notes 7 and 8) | | 40 | | 45 | | 50 | ns | |
| t_{RASP} | Pulse duration, page-mode, \overline{RAS} low | | 60 | | 100 000 | | 70 | 100 000 | ns |
| t_{RAS} | Pulse duration, non-page-mode, \overline{RAS} low | | 60 | | 10 000 | | 70 | 10 000 | ns |
| t_{CAS} | Pulse duration, \overline{CAS} low | | 15 | | 10 000 | | 18 | 10 000 | ns |
| t_{CP} | Pulse duration, \overline{CAS} high | | 10 | | 10 | | 10 | ns | |
| t_{RP} | Pulse duration, \overline{RAS} high (precharge) | | 40 | | 50 | | 60 | ns | |
| t_{WP} | Pulse duration, \overline{W} low | | 10 | | 10 | | 10 | ns | |
| t_{ASC} | Setup time, column address before \overline{CAS} low | | 0 | | 0 | | 0 | ns | |
| t_{ASR} | Setup time, row address before \overline{RAS} low | | 0 | | 0 | | 0 | ns | |
| t_{DS} | Setup time, data before \overline{CAS} low | | 0 | | 0 | | 0 | ns | |
| t_{RCS} | Setup time, \overline{W} high before \overline{CAS} low | | 0 | | 0 | | 0 | ns | |
| t_{CWL} | Setup time, \overline{W} -low before \overline{CAS} high | | 15 | | 18 | | 20 | ns | |
| t_{RWL} | Setup time, \overline{W} -low before \overline{RAS} high | | 15 | | 18 | | 20 | ns | |
| t_{WCS} | Setup time, \overline{W} -low before \overline{CAS} low | | 0 | | 0 | | 0 | ns | |
| t_{WRP} | Setup time, \overline{W} -high before \overline{RAS} low (CBR refresh only) | | 10 | | 10 | | 10 | ns | |

NOTES: 7. All cycles assume $t_T = 5$ ns.

8. To assure t_{PC} min, t_{ASC} should be $\geq t_{CP}$.

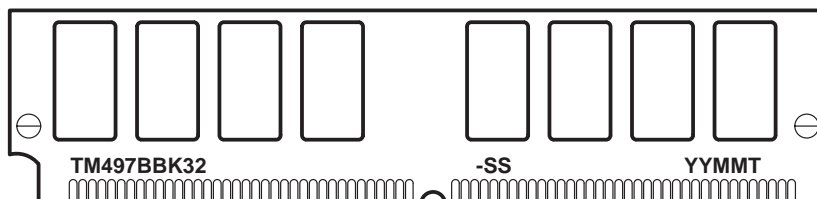


timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | '497BBK32-60 | | '497BBK32-70 | | '497BBK32-80 | | UNIT |
|---|--------------|-----|--------------|-----|--------------|-----|------|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{CAH} Hold time, column address after $\overline{\text{CAS}}$ low | 10 | | 15 | | 15 | | ns |
| t _{RHCP} Hold time, $\overline{\text{RAS}}$ high from $\overline{\text{CAS}}$ precharge | 35 | | 40 | | 45 | | ns |
| t _{DH} Hold time, data after $\overline{\text{CAS}}$ low | 10 | | 15 | | 15 | | ns |
| t _{RAH} Hold time, row address after $\overline{\text{RAS}}$ low | 10 | | 10 | | 10 | | ns |
| t _{RCH} Hold time, $\overline{\text{W}}$ high after $\overline{\text{CAS}}$ high (see Note 9) | 0 | | 0 | | 0 | | ns |
| t _{RRH} Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ high (see Note 9) | 0 | | 0 | | 0 | | ns |
| t _{WCH} Hold time, $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ low | 10 | | 15 | | 15 | | ns |
| t _{WRH} Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ low (CBR refresh only) | 10 | | 10 | | 10 | | ns |
| t _{CHR} Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only) | 10 | | 10 | | 10 | | ns |
| t _{CRP} Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low | 5 | | 5 | | 5 | | ns |
| t _{CSH} Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high | 60 | | 70 | | 80 | | ns |
| t _{CSR} Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only) | 5 | | 5 | | 5 | | ns |
| t _{RAD} Delay time, $\overline{\text{RAS}}$ low to column address (see Note 10) | 15 | 30 | 15 | 35 | 15 | 40 | ns |
| t _{RAL} Delay time, column address to $\overline{\text{RAS}}$ high | 30 | | 35 | | 40 | | ns |
| t _{CAL} Delay time, column address to $\overline{\text{CAS}}$ high | 30 | | 35 | | 40 | | ns |
| t _{RCD} Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 10) | 20 | 45 | 20 | 52 | 20 | 60 | ns |
| t _{RPC} Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR only) | 0 | | 0 | | 0 | | ns |
| t _{RSH} Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high | 15 | | 18 | | 20 | | ns |
| t _{REF} Refresh time interval | | 32 | | 32 | | 32 | ms |
| t _T Transition time | 3 | 30 | 3 | 30 | 3 | 30 | ns |

9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.

device symbolization



- YY = Year Code
- MM = Month Code
- T = Assembly Site Code
- SS = Speed Code

NOTE: The location of the part number may vary.

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