



FEATURES

- **Two matched-delay outputs:**
 - Bank A: undivided pass-through (QA)
 - Bank B: programmable divide by 2, 4, 8, 16 (QB0, QB1)
- **Matched delay:** all outputs have matched delay, independent of divider setting
- **Guaranteed AC performance:**
 - >2.5GHz f_{MAX}
 - <250ps t_r/t_f
 - <670ps t_{pd} (matched delay)
 - <15ps within-device skew
- **Low jitter design**
 - <1ps_{rms} cycle-to-cycle jitter
 - <10ps_{pp} total jitter
- **Power supply 3.3V or 2.5V**
- **Unique patent-pending input termination and VT pin for DC-coupled and AC-coupled inputs:** any differential inputs (LVPECL, LVDS, CML, HSTL)
- **TTL/CMOS inputs for select and reset**
- **100K EP compatible LVPECL outputs**
- **Parallel programming capability**
- **Wide operating temperature range: -40°C to +85°C**
- **Available in 16-pin (3mm x 3mm) MLF™ package**



Precision Edge™

DESCRIPTION

The SY89871U is a 2.5V/3.3V LVPECL output precision clock divider capable of accepting a high-speed differential clock input (AC or DC-coupled) CML, LVPECL, HSTL or LVDS clock input signal and dividing down the frequency using a programmable divider ratio to create a frequency-locked lower speed version of the input clock (Bank B). Available divider ratios are 2, 4, 8 and 16. In a typical 622MHz clock system this would provide availability of 311MHz, 155MHz, 77MHz, or 38MHz auxiliary clock components.

The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

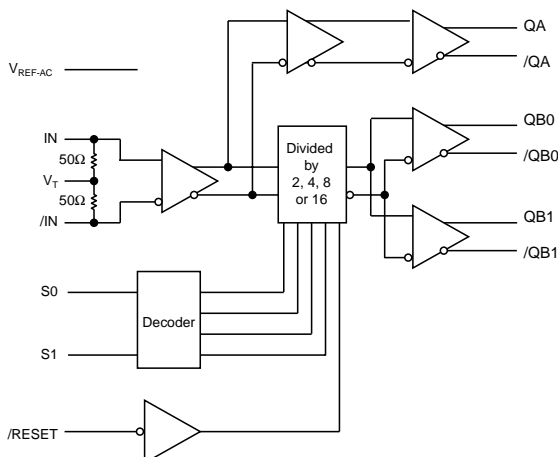
The SY89871U includes two phase-matched output banks. Bank A (QA) is a frequency-matched copy of the input. Bank B (QB0, QB1) is a divided down output of the input frequency. Bank A and Bank B maintain a matched delay independent of the divider setting.

All support documentation can be found on Micrel's web site at www.micrel.com.

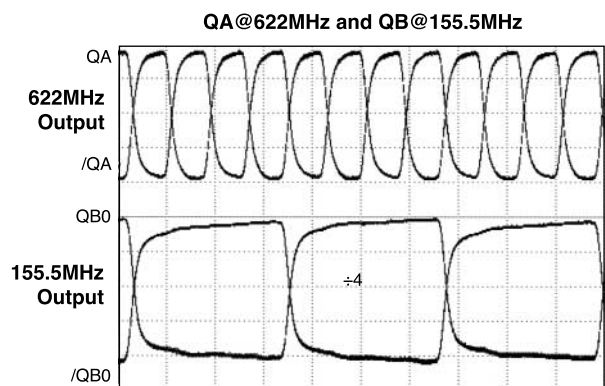
APPLICATIONS

- OC-3 to OC-192 SONET/SDH applications
- Transponders
- Oscillators
- SONET/SDH line cards

FUNCTIONAL BLOCK DIAGRAM

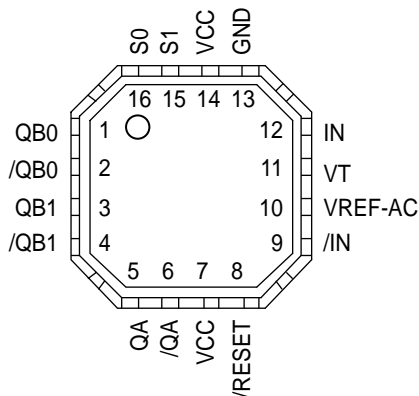


TYPICAL PERFORMANCE



Precision Edge is a trademark of Micrel, Inc.
MicrdLeadFrame and MLF are trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



16-Pin MLF™ (MLF-16)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY89871UMI	MLF-16	Industrial	871U
SY89871UMITR ⁽¹⁾	MLF-16	Industrial	871U

Note:

- 1. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 2, 3, 4	QB0, /QB0 QB1, /QB1	Differential Buffered Output Clocks: This differential output is a divided-down version of the input frequency and has a matched output delay with Bank A. Divided by 2, 4, 8, or 16. See "Truth Table." Unused output pairs may be left floating.
5, 6	QA, /QA	Differential Buffered Undivided Output Clock.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF 0.01µF low ESR capacitors.
8	/RESET	Output Reset: Internal 25kΩ pull-up. Logic LOW will reset the divider select. See "Truth Table." Input threshold is $V_{CC}/2$.
12, 9	IN, /IN	Differential Input: Internal 50Ω termination resistors to VT input. See "Input Interface Applications" section.
10	VREF-AC	Reference Voltage: Equal to $V_{CC}-1.4V$ (approx.), and used for AC-coupled applications. Maximum sink/source current is 0.5mA. See "Input Interface Applications" section.
11	VT	Termination Center-Tap: For CML and LVDS inputs, leave this pin floating. Otherwise, see "Input Interface Application" section.
13	GND	Ground.
15, 16	S1, S0	Select Pins: See "Truth Table." LVTTTL/CMOS logic levels. Internal 25kΩ pull-up resistor. Logic HIGH if left unconnected (divided by 16 mode). S0 = LSB. Input threshold is $V_{CC}/2$.

TRUTH TABLE

/RESET	S1	S0	Bank A Output	Bank B Outputs
1	0	0	Input Clock	Input Clock +2
1	0	1	Input Clock	Input Clock +4
1	1	0	Input Clock	Input Clock +8
1	1	1	Input Clock	Input Clock +16
0	X	X	Input Clock	QB = LOW, /QB = HIGH

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	-0.5V to +4.0V
Input Voltage (V_{IN})	-0.5V to $V_{CC} + 0.3V$
PECL Output Current (I_{OUT})		
Continuous	50mA
Surge	100mA
V_T Current (I_{VT})	$\pm 100mA$
Input Current I_N , /IN (I_{IN})	$\pm 50mA$
V_{REF-AC} Sink/Source Current ($I_{VREF-AC}$) ⁽³⁾	$\pm 2mA$
Lead Temperature (soldering, 10 sec.)	220°C
Storage Temperature (T_S)	-65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC})	+2.375V to +3.63V
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance ⁽⁴⁾		
MLF™ (θ_{JA})		
Still-Air	60°C/W
500lfpm	54°C/W
MLF™ (ψ_{JB})		
Junction-to-board	32°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

$T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		2.37		3.60	V
I_{CC}	Power Supply Current	No load, max V_{CC} .		50	75	mA
R_{IN}	Differential Input Resistance, (IN, /IN)		80	100	120	Ω
V_{IH}	Input HIGH Voltage, (IN, /IN)	Note 6	0.1		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage, (IN, /IN)	Note 6	-0.3		$V_{CC} + 0.2$	V
V_{IN}	Input Voltage Swing	Notes 6, 7	0.1		3.6	V
V_{DIFF_IN}	Differential Input Voltage Swing	Notes 6, 7, 8	0.2			V
$ I_{IN} $	Input Current, (IN, /IN)	Note 6			45	mA
V_{REF-AC}	Reference Voltage	Note 9	$V_{CC} - 1.525$	$V_{CC} - 1.425$	$V_{CC} - 1.325$	V

Notes:

1. Permanent device damage may occur if ratings in the "Absolute Maximum Ratings" section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Due to the internal termination (see "Input Structure Buffer") the input current depends on the applied voltages at IN, /IN and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.
7. See "Timing Diagram" for V_{IN} definition. V_{IN} (max.) is specified when V_T is floating.
8. See "Typical Operating Characteristics" section for V_{DIFF} definition.
9. Operating using V_{IN} is limited to AC-coupled PECL or CML applications only. Connect directly to VT pin.

(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS⁽¹⁰⁾

$V_{CC} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$; $T_A = -40^\circ C$ to $+85^\circ C$, $R_L = 50\Omega$ to $V_{CC} - 2V$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		$V_{CC} - 1.145$	$V_{CC} - 1.020$	$V_{CC} - 0.895$	V
V_{OL}	Output LOW Voltage		$V_{CC} - 1.945$	$V_{CC} - 1.820$	$V_{CC} - 1.695$	V
V_{OUT}	Output Voltage Swing		550	800	1050	mV
V_{DIFF_OUT}	Differential Output Voltage Swing		1.10	1.6	210	V

LVTTL/LVCMOS DC ELECTRICAL CHARACTERISTICS⁽¹⁰⁾

$V_{CC} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$; $T_A = -40^\circ C$ to $+85^\circ C$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		20	μA
I_{IL}	Input LOW Current				-300	μA

Note:

10. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. Parameters are for $V_{CC} = 2.5V$. They vary 1:1 with V_{CC} .

AC ELECTRICAL CHARACTERISTICS(11)

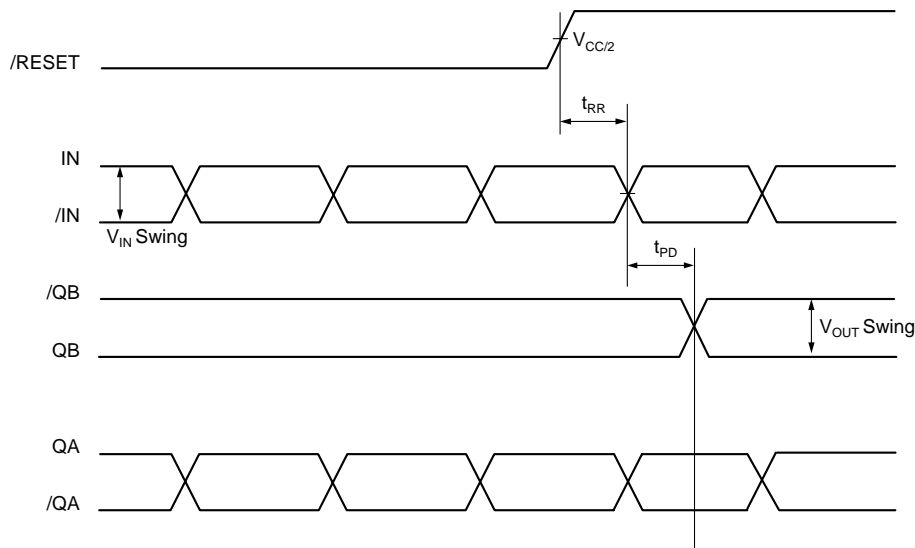
$V_{CC} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Output Toggle Frequency	Output Swing $\geq 400mV$	2.5			GHz
	Maximum Input Frequency	Note 12	3.2			GHz
t_{PLH} t_{PHL}	Differential Propagation Delay IN-to-QA or QB	Input Swing $< 400mV$ Input Swing $\geq 400mV$	460 420	580 550	710 670	ps
t_{SKEW}	Within-Device Skew (Differential) QB0-to-QB1	Note 13		7	15	ps
	Within-Device Skew (Differential) QA-to-QB	Note 13		12	30	ps
	Part-to-Part Skew (Differential)	Note 13			250	ps
T_{jitter}	Cycle-to-Cycle Jitter	Note 14			1	ps _{rms}
	Total Jitter	Note 15			10	ps _{pp}
t_{RR}	Reset Recovery Time		600			ps
t_r, t_f	Output Rise/Fall Times (20% to 80%)		70	150	250	ps

Notes:

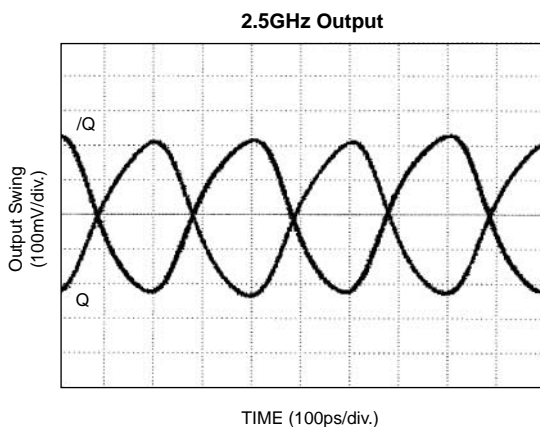
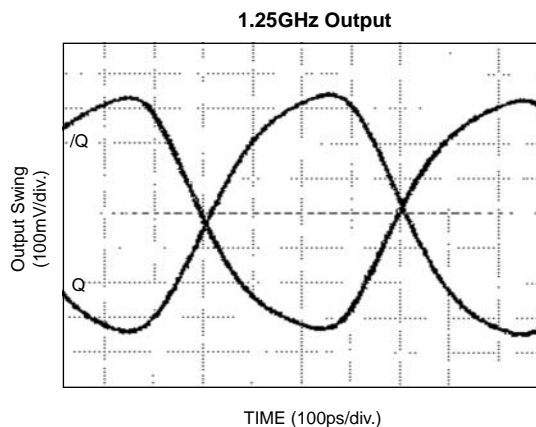
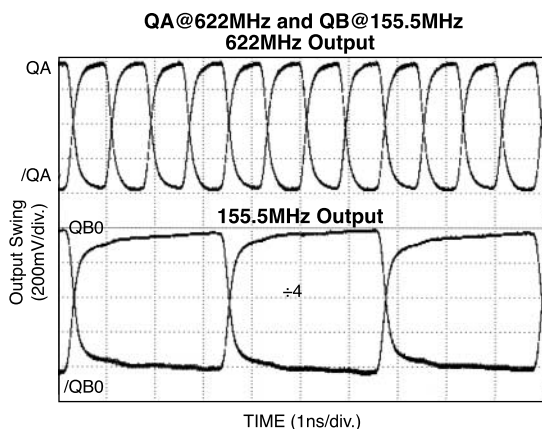
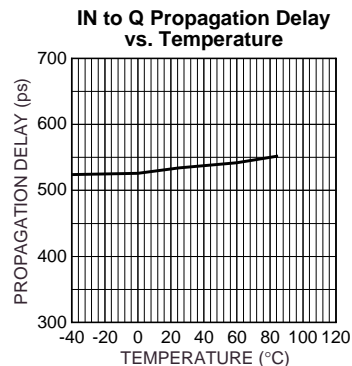
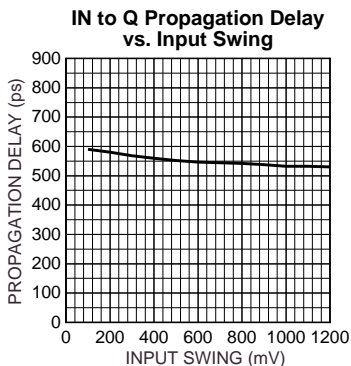
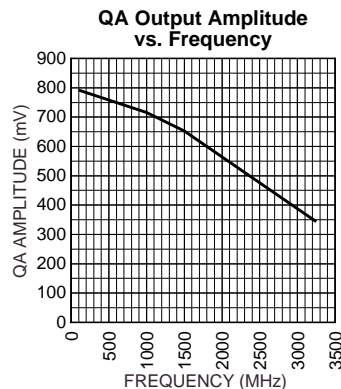
11. Measured with 400mV input signal, 50% duty cycle, all loading with 50Ω to $V_{CC}-2V$, unless otherwise stated.
12. Bank A (pass-through) maximum frequency is limited by the output stage. Bank B (input-to-output +2, +4, +8, +16) can accept an input frequency $>3GHz$, while Bank A will be slew rate limited.
13. Skew is measured between outputs under identical transitions.
14. Cycle-to-cycle jitter definition: the variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{jitter_cc} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
15. Total jitter definition: with an ideal clock input, of frequency $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TIMING DIAGRAM



TYPICAL OPERATING CHARACTERISTICS

$V_{CC} = 3.3V$, $V_{IN} = 400mV$, $T_A = 25^{\circ}C$, unless otherwise stated.



DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING

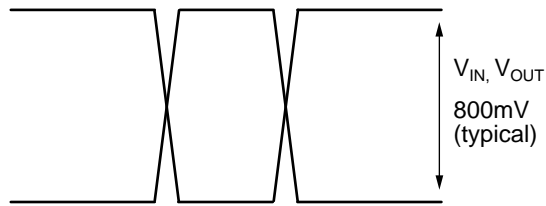


Figure 1a. Single-Ended Swing

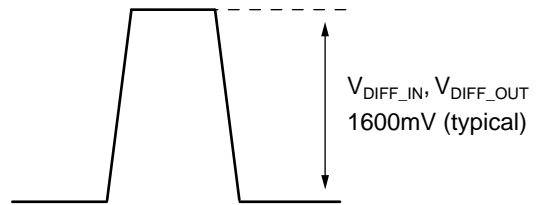


Figure 1b. Differential Swing

INPUT BUFFER STRUCTURE

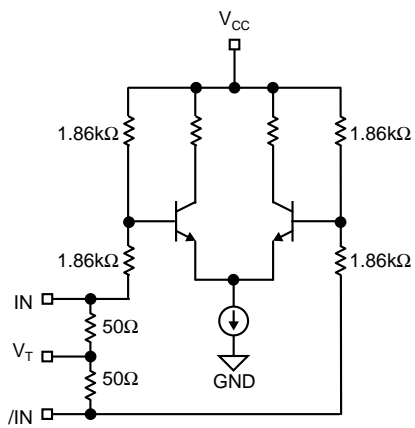


Figure 2a. Simplified Differential Input Buffer

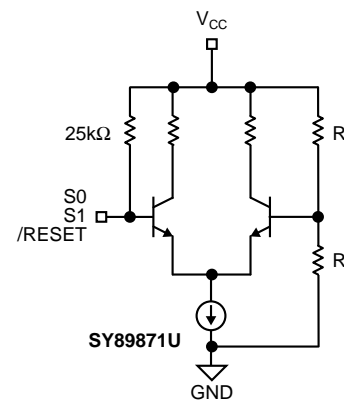


Figure 2b. Simplified TTL/CMOS Input Buffer

INPUT INTERFACE APPLICATIONS

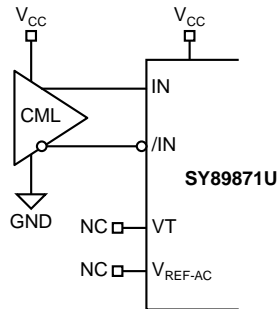


Figure 3a. DC-Coupled CML Input Interface

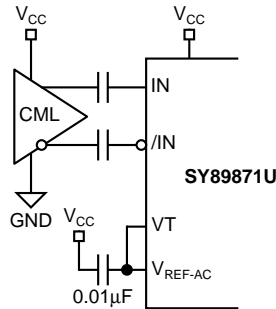


Figure 3b. AC-Coupled CML Input Interface

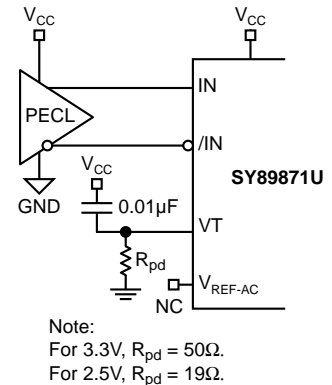


Figure 3c. DC-Coupled PECL Input Interface

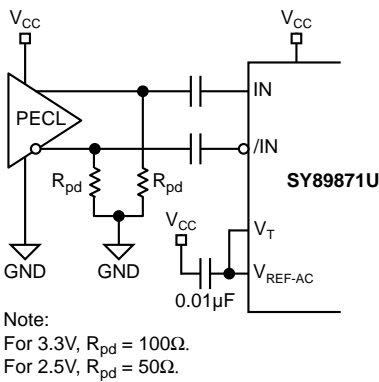


Figure 3d. AC-Coupled PECL Input Interface

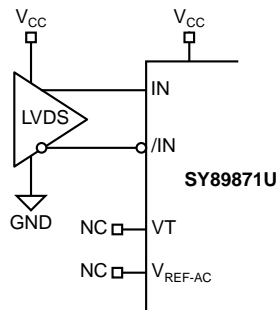


Figure 3e. LVDS Input Interface

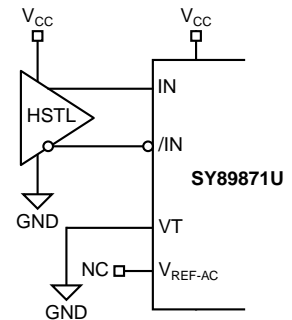


Figure 3f. HSTL Input Interface

RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89874U	2.5GHz Any Diff. In-to-LVPECL Programmable Clock Divider and 1:2 Fanout Buffer w/Internal Termination	http://www.micrel.com/product-info/products/sy89874u.shtml
	MLF™ Application Note	http://www.amkor.com/products/notes_papers/mlf_appnote.pdf
HBW Solutions	New Products and Applications	http://www.micrel.com/product-info/products/solutions.shtml

LVPECL OUTPUT TERMINATION RECOMMENDATIONS

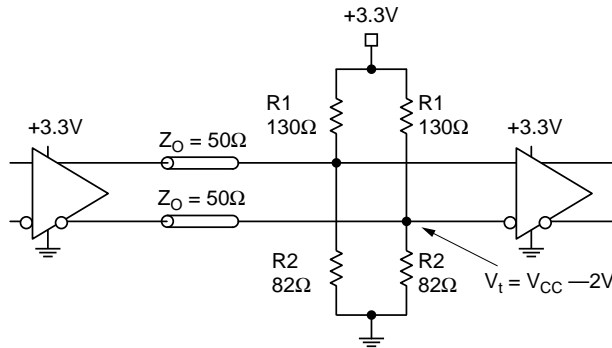


Figure 4a. Parallel Termination-Thevenin Equivalent

Note:

1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

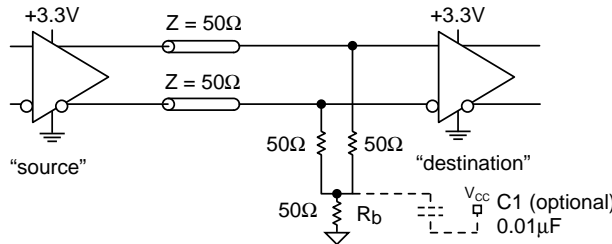


Figure 4b. Three-Resistor "Y-Termination"

Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_T. For +3.3V systems R_b = 46Ω to 50Ω. For +2.5V systems R_b = 19Ω.
4. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

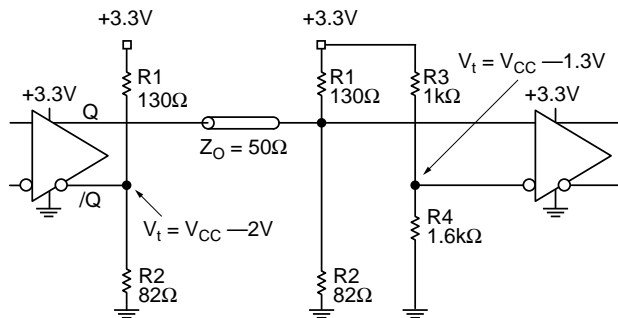
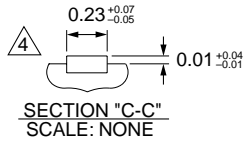
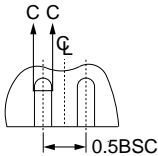
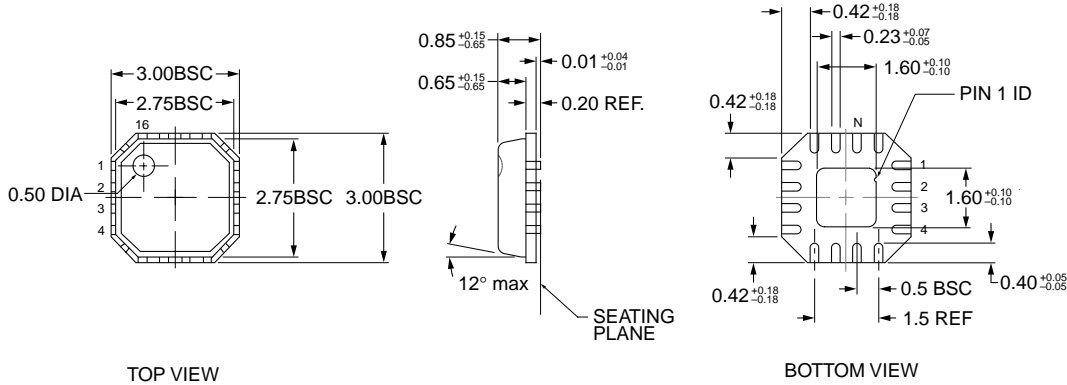


Figure 4d. Terminating Unused I/O

Notes:

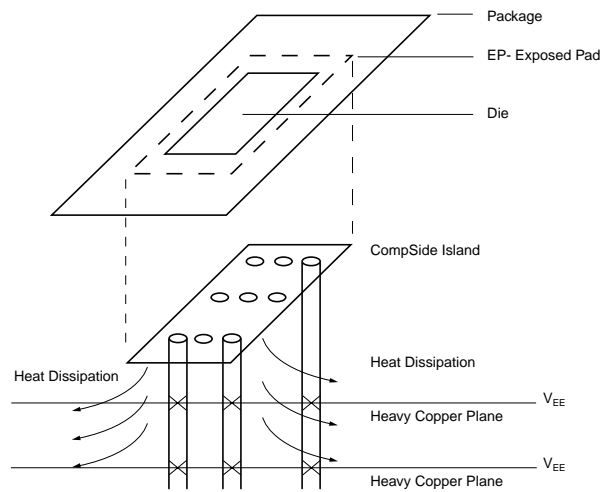
1. Unused output (/Q) must be terminated to balance the output.
2. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.

16 LEAD MicroLeadFrame™ (MLF-16)



1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

FOR EVEN TERMINAL/SIDE



Rev. 02

**PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)**

Package Notes:

1. Package meets Level 2 moisture sensitivity classification, and is shipped in dry-pack form.
2. Exposed pads must be soldered to a ground for proper thermal management.

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