FEATURES

- DVD-Video, VCD, VCD 2.0, SVCD, CD, and other popular standards
- DVD-Audio including CPPM and Verance™ watermark protection
- MPEG-1, MPEG-2, and leading edge MPEG-4 audio and video decoding
- Kodak Picture CD
- Flexible ATAPI or AV bus DVD loader support with no additional logic
- Dual 32-bit RISC processors, supported by RTOS, C / C++ compilers, and source level debuggers
- 32-bit DSP capable of running AC-3, MPEG, DTS, MP3, WMA, and AAC audio decode algorithms
- High quality integrated video encoder with six 10-bit video D / A converters
- Component (RGB or YUV) or composite & S-Video output
- Interlaced (PAL / NTSC) or progressive (480p) output, with Macrovision™ copy protection
- CCIR656 video I / O for video capture, PVR and DVR type applications, picture-in-picture support
- IEC60958 / 937 (S / PDIF) & simultaneous PCM output
- 5.1 downmix, karaoke echo mix, pitch shift, and many other effects
- PAL / NTSC transcoding
- Dual 16550 compatible UARTs
- ATAPI / IDE interface for hard disk, audio server, and Personal Video Recorder (PVR) applications
- 240-pin MQFP package

ORDERING INFORMATION:

CS98200-CM

See ordering information legend on page 60.

New Highly-Integrated Processor for Tomorrow's DVD Players and DVD Receivers

OVERVIEW

CS98200 is a highly-integrated processor that provides all of the audio and video processing functions needed for the next generation of feature-rich DVD players, DVD receivers and Internet DVD applications. Tomorrow's features available today in a single chip solution are DVD-Audio, MP3, WMA®, MPEG-2 / 4: AAC, Kodak Picture CD™, Dolby Digital™, Dolby ProLogic II™, and DTS Digital Surround™ decoding. It supports most popular CD formats, DVD navigation, disk control, video decoding and up to eight channels of audio output. An extension of Cirrus' CS98000 DVD product line, the CS98200 integrates six 10-bit video digital-to-analog converters (DACs) and TV encoding with progressive scan functionality. Progressive scan video provides high resolution and eliminates the "flickering" effect present in traditional video playback. Other features enabled by this integrated chip include karaoke functionality and video special effects. Its extended feature set makes it ideal for your next innovative DVD application … today.

Need to get your product to market quickly? Cirrus' Total Entertainment platform solutions include DVD front-end controllers, MPEG encoders, audio DSPs, and digital power amplifiers … everything you need to launch your product before the competition. CS98200 is a Cirrus Total Entertainment Total-E™ IC solution specifically designed for consumer entertainment electronics.

(cont.)

Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

OVERVIEW *(cont.)*

Here is a summary of the CS98200 features.

System Characteristics

- Dual 32-bit (180 MHz) RISC processors
- 32-bit DSP processor ~ 180 MIPS
- 240-pin MQFP package
- All I/O pins are 3 V with 5 V tolerance
- Advanced 0.18 µ CMOS technology
- Low power modes and clock shutoff

Memory Controller

- Up to 120 MHz SDRAM from 4 MB to 32 MB
- FLASH databus isolated from SDRAM bus to allow faster SDRAM access
- 32-bit data bus for DRAM, 8-bit data bus for ROM data flow engine
- Two DMA controllers — local memory based and direct memory-to-memory
- DMA to/from main RAM into local SRAM

MPEG Video Decoder

- DVD, VCD, VCD 2.0 and SVCD
- MPEG-1, MPEG-2, and MPEG-4 simple profile
- Anti-tearing logic controls picture decode and presentation
- Advanced error concealment hardware

Audio Interface

- 8 channels PCM output at 24-bits/192 kHz output rate
- 2 channels I2S input at 24-bits/96 kHz
- IEC 60958/61937 capabilities

External Interface

- Serial master/slave ports for controlling DVD device
- ATAPI/IDE interface can also control hard disk drives for PVR features
- Programmable bidirectional I/O pins
- All pins not used for other functions can be reassigned as general purpose I/O pins
- Hardware assisted support for infrared remote devices, such as remote control, infrared keyboard, mouse, printer, and more
- Programmable parallel host master interface supports formats including ATAPI, ISA, and more
- I/O channel interface supports all DVD loader protocols

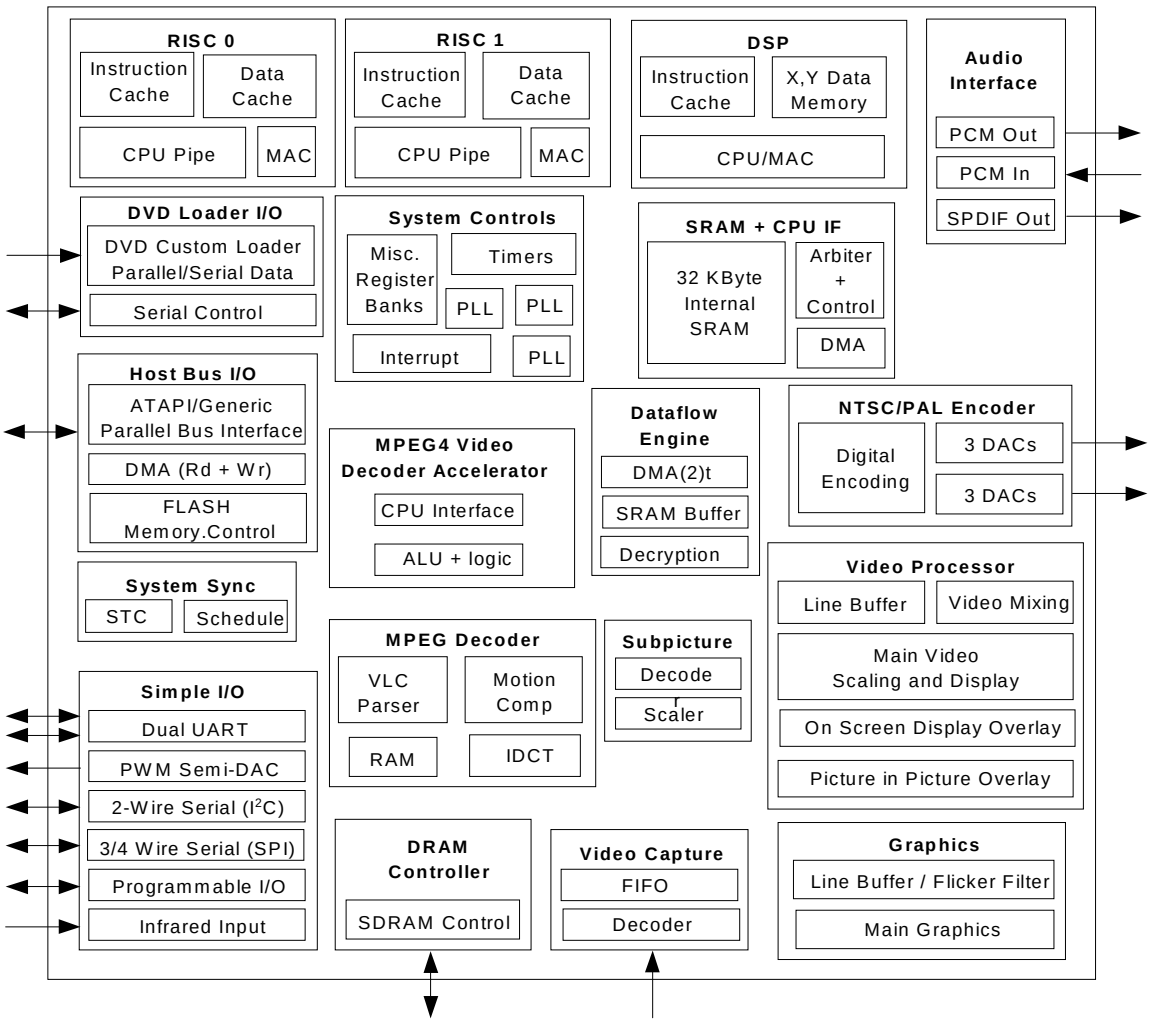
Video Processor

- OSD module with multiple regions and transparencies
- Full screen graphics module, with 16 bit true-color graphics plane
- High quality video scaling using multi-tap programmable vertical and horizontal filters

Video Encoder

- Six 10-bit video DAC's, drives 37.5 Ω load directly
- Progressive (480p) or interlaced PAL (B, D, G, H, I, N, M, 60) and NTSC mode output
- Component (RBG or YUV) or composite + S-Video output
- Macrovision™ 7.1 support (interlaced) and Macrovision™ 1.03 support (progressive)
- Wide-screen signaling support (interlaced and progressive) and CGMS
- Closed captioning support

BLOCK DIAGRAM



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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find one nearest you go to **http://www.cirrus.com/corporate/contacts/sales.cfm**

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1. CHARACTERISTICS AND SPECIFICATIONS

1.1 AC AND DC PARAMETRIC SPECIFICATIONS

(AGND, DGND=0 V, all voltages with respect to 0 V)

1.1.1 ABSOLUTE MAXIMUM RATING

Symbol	Description	Min	Max	Unit
VDD_{IO}	Power Supply Voltage on analog core and I/O ring	-0,5	4.6	Volts
VDD_{CORE}	Power Supply Voltage on core logic and PLL	-0.5	2.5	Volts
V_I	Digital Input Applied Voltage (power applied)	-0.5	5.5	Volts
I_I	Digital Input Forced Current	-10	10	mA
I_O	Digital Output Forced Current	-50	50	mA
T_{SOL}	Lead Soldering Temperature	-	260	^oC
T_{VSOL}	Vapor Phase Soldering Temperature	-	235	^oC
T_{STOR}	Storage Temperature (no power applied)	-40	125	^oC
T_{AMB}	Ambient Temperature (power applied)	0	70	^oC
P_{total}	Total Power consumption	-	2.2	W

CAUTION: Operating beyond these Minimum and Maximum limits can result in permanent damage to the device. Cirrus Logic recommends that CS98200 devices operate at the settings described in the next table.

1.1.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage, Analog and IO	V_{IO} & V_{AA}	3.0	3.3	3.6	Volts
Supply Voltage, Core Logic and PLL	V_{PLL} &V_{DD}	1.62	1.8	1.98	Volts
Ambient Temperature (power applied)	T_{AMB}	0	25	70	^oC

1.1.3 ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current, IO	I_{DD}	Normal Operating		65		mA
Supply Current, Core Logic and PLL	I_{DD}	Normal Operating		210		mA
Input Voltage, High	V_{IH}		2.0	-		Volts
Input Voltage, Low	V_{IL}		-	-	0.8	Volts
Input Current	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS}	-1	-	1	µA
Input Pull up/down resistor	R_I		-	75	-	KΩ
Output Voltage, High	V_{OH}	@ buffer rating	2.2	-	-	Volts
Output Voltage, Low	V_{OL}	@ buffer rating	-	-	0.4	Volts
High-Z-state Leakage	I_{OZ}	$V_{OUT} = V_{SS}$ or V_{DD}	-1	-	1	µA
Video DACs[1]		R_{SET} = 174Ω				
DAC Resolution					10	bits
DAC to DAC matching[2]	MAT			2		%
Output Voltage Range	V_{out}	R_{LOAD} = 37.5Ω[3]		1.28		Volts

Differential Gain	DG			1		%
Differential Phase	DP			0.5		%
Signal to Noise	SNR			74		dB
Chrominance AM Noise	AM			80		dB
Chrominance PM Noise	PM			75		dB

1. Video parameters guaranteed only with 1% tolerance resistors or better for Rset and RLoad.
2. Only applies to each set of three DACs.
3. RLoad is a double terminated load, which includes a 75 Ω resistor at the video DAC and a 75 Ω resistor at the video monitor.

2. TIMINGS

2.1 Timing Diagram Conventions

This data sheet contains timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labeled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

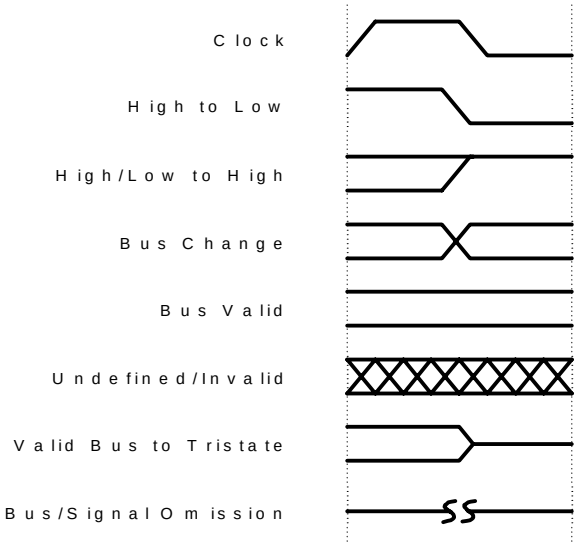


Figure 1. Legend for Timing Diagrams

2.2 DC CHARACTERISTICS

(T_A= 25° C; V_{PLL}=V_{DD}=1.8V±10%, V_{IO}=V_{AA}=3.3 V±10%)

2.2.1 ATAPI Interface

CS98200 can interface with a ATAPI-type slave loader gluelessly. Figure 2 illustrates a read ATAPI transaction and a write ATAPI transaction.

Symbol	Description	Min	Typ	Max	Unit
t_{acyc}[1]	Cycle Time	87			ns
t_{aavr}	Address Valid to HMRD-/HMWR- Setup	7			ns
t_{ah}	Address Hold from HMRD-/HMWR Setup	11			ns
t_{arww}	H_RD/H_WR Pulse Width	63			ns
t_{arec}	H_RD/H_WR Recovery Time	21			ns
t_{awsu}	H_WR Data Setup	30			ns
t_{awh}	H_WR Data Hold	8			ns
t_{ardsu}	H_RD Data Setup	20			ns
t_{arddh}	H_RD Data hold	0			ns
t_{ardts}	H_RD Data High-Z-state			8	ns
t_{arsu}	H_RDY Setup Time	14			ns
t_{arh}[1]	H_RDY Hold Time	0			ns

Table 1. ATAPI Interface Characteristics

1. Values are guaranteed by design only

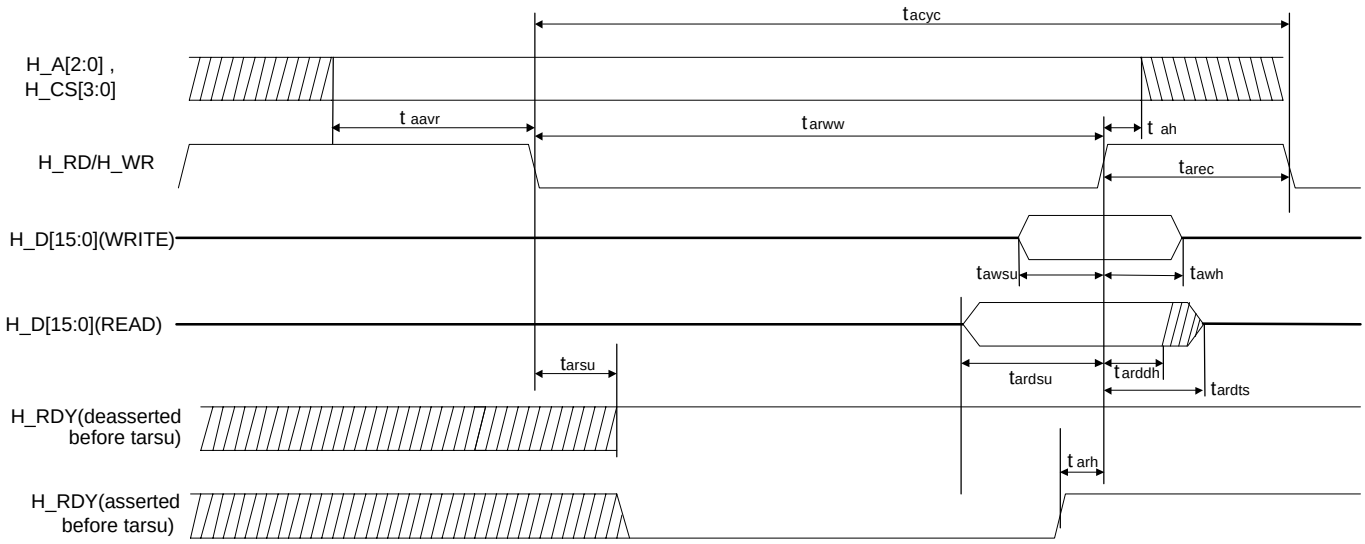


Figure 2. ATAPI Interface Timing Diagram

2.2.2 DVD Loader Interface

Symbol	Description	Min	Typ	Max	Unit
$t_{dlckper}$	DVDL_CK Period	400			ns
t_{dldisu}	DVDL_DI Setup Time	5			ns
t_{dldih}	DVDL_DI Hold Time	10			ns
t_{dldod}	DVDL_DO Output Delay from Falling Edge			5	ns
$t_{dlstbwd}$	DVD_STB Width	250			ns
t_{dlstbl}	DVD_STB Low Time	40			%
t_{dlstbh}	DVD_STB High Time	40			%
$t_{dlreqod}$	DVD_RDY Output Delay			90	ns
t_{dlensu}	DVD_ENA Setup Time	5			ns
t_{dlenh}	DVD_ENA Hold Time	5			ns
t_{dldsu}	DVD_D[7:0] Setup Time	5			ns
t_{dldh}	DVD_D[7:0] Hold Time	5			ns
$t_{dlsossu}$	DVD_SOS Setup Time	5			ns
t_{dlsosh}	DVD_SOS Hold Time	5			ns
t_{lrcksu}	CD_LRCK Setup Time	5			ns
t_{cddsu}	CD_DATA Setup Time	5			ns
t_{cddh}	CD_DATA Hold Time	5			ns
t_{cdcpsu}	CD_C2PO Setup Time	5			ns
t_{cdcph}	CD_C2PO Hold Time	5			ns

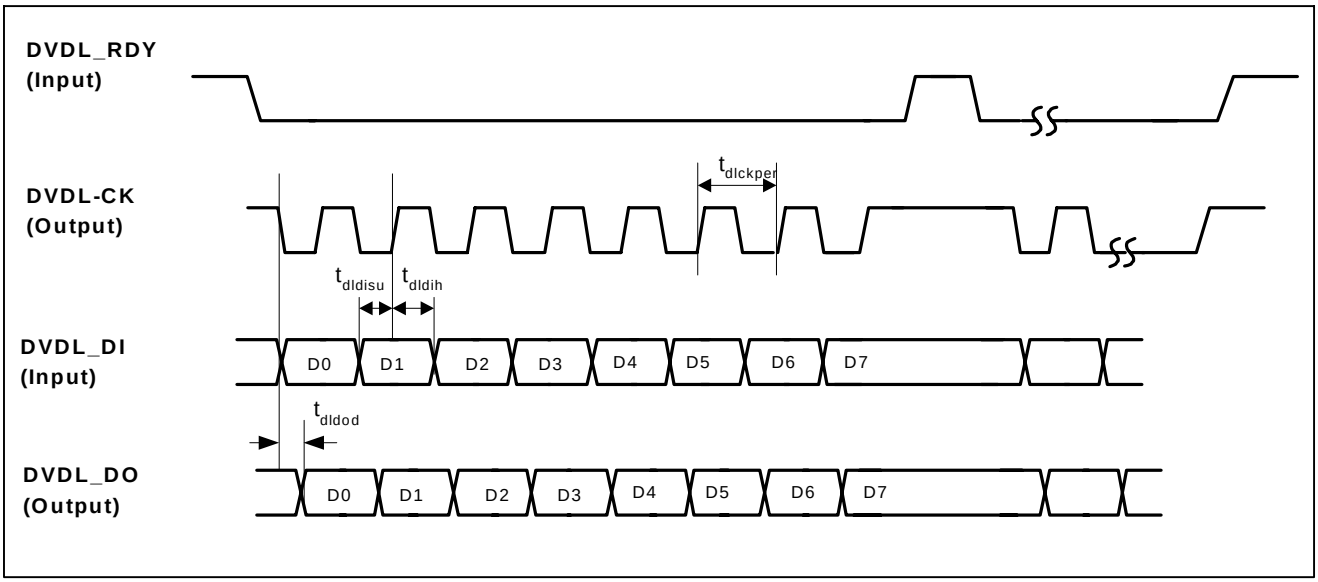


Figure 3. DVD Loader Host Interface

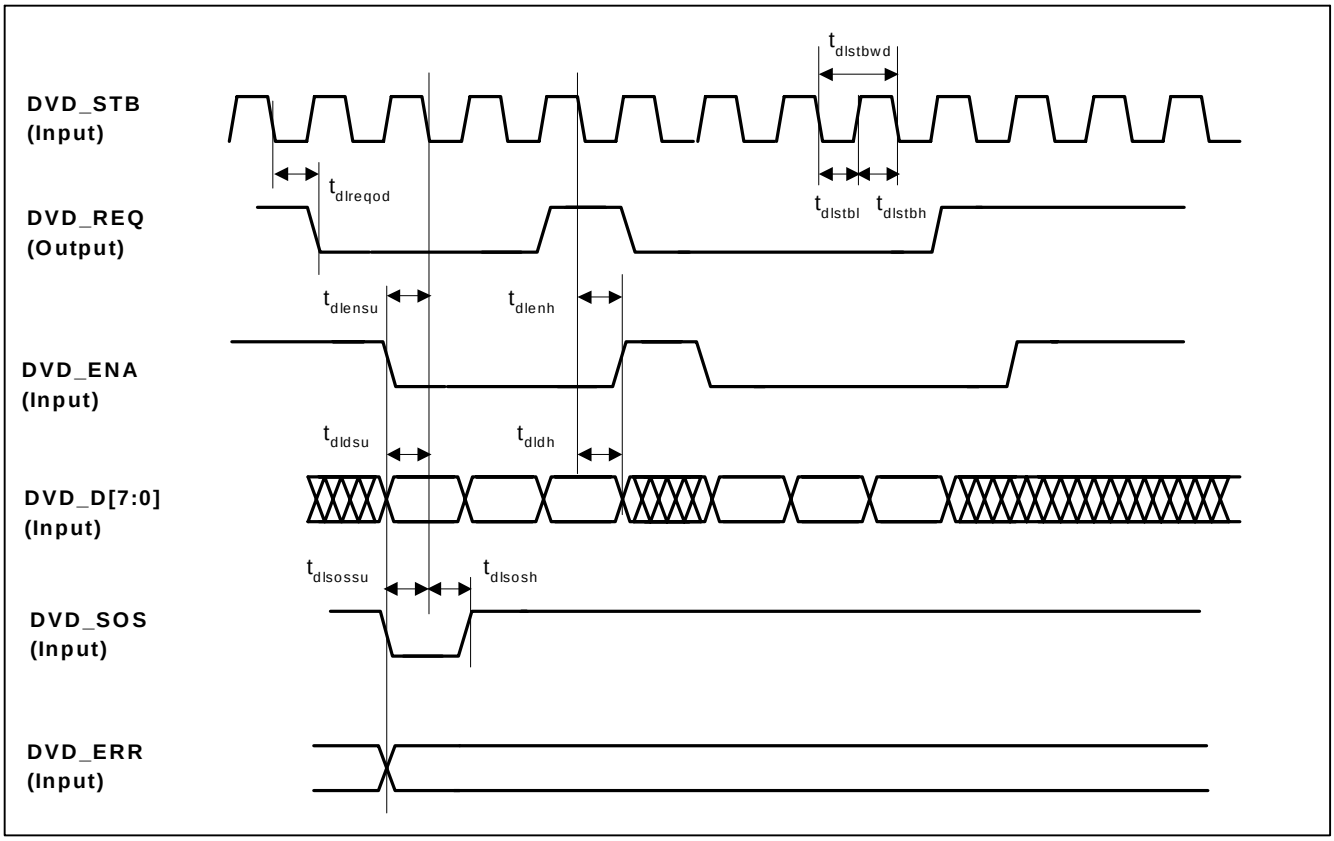


Figure 4. DVD Loader Data Interface

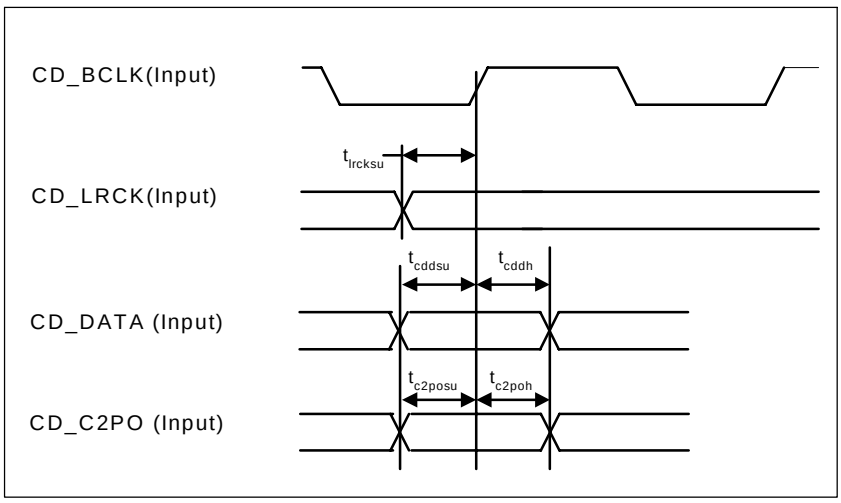
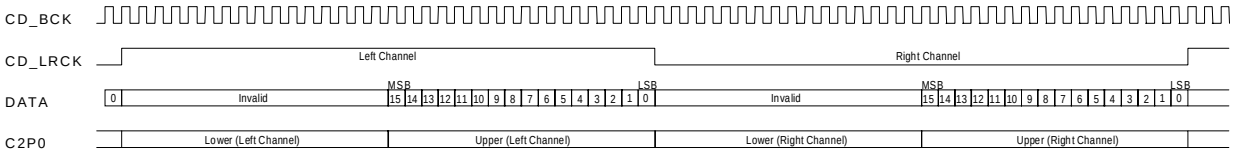
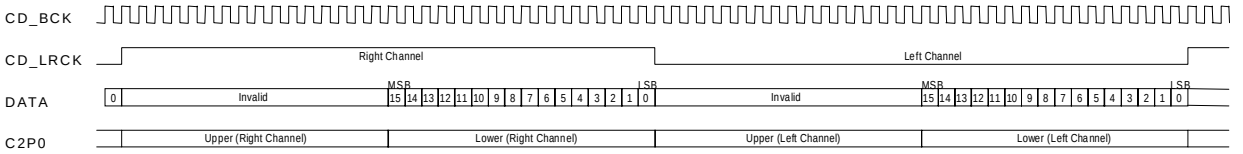


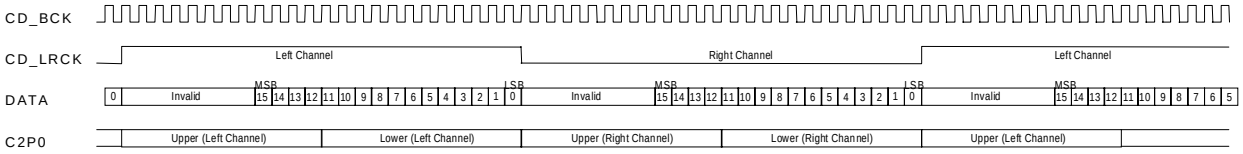
Figure 5. DVD Loader CD Interface



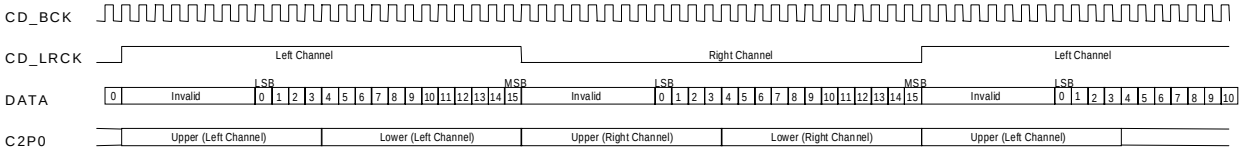
32-bit BCK, MSB First, Right Channel Low, C2P0 LSB First, Data latch timing high



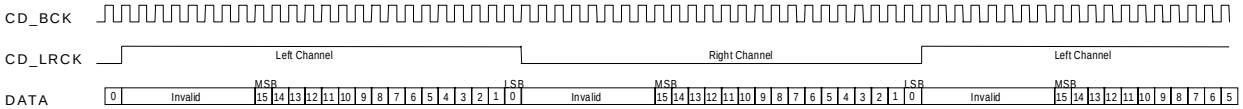
32-bit BCK, MSB First, Left Channel Low, C2P0 MSB First, Data latch timing low



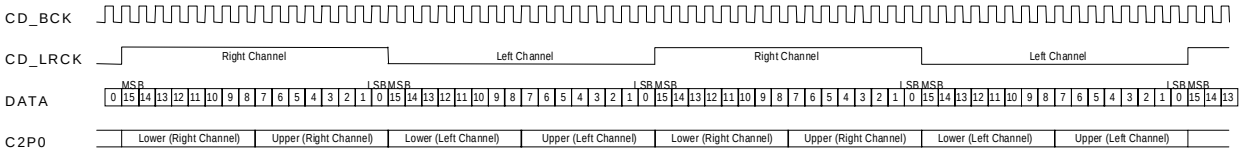
24-bit BCK, MSB First, Right Channel Low, C2P0 MSB First, Data latch timing high



24-bit BCK, LSB First, Right Channel Low, C2P0 MSB First, Data latch timing low



24-bit BCK, MSB First, Right Channel Low, Data latch timing high (Note: no C2P0 for this format)



16-bit BCK, MSB First, Left Channel Low, C2P0 LSB First, Data latch timing high

Figure 6. DVD Loader CD Interface Formats

2.2.3 DVD Serial Interface Timing

Symbol	Description	Min	Typ	Max	Unit
tdsckper[1]	DVDS_CLK Period	33			ns
tdsckl[1]	DVDS_CLK Low Time	40	50		%
tdsckh[1]	DVDS_CLK High Time	40	50		%
tdsdsu	DVDS_DATA Setup to DVDS_CLK active edge	5			ns
tdsdhd	DVDS_DATA Hold after DVDS_CLK active edge	5			ns
tdscdsu	DVDS_VLD, DVDS_SOS Setup to DVDS_CLK	5			ns
tdscdhd	DVDS_VLD, DVDS_SOS Hold after DVDS_CLK	5			ns

1. Values are guaranteed by design only

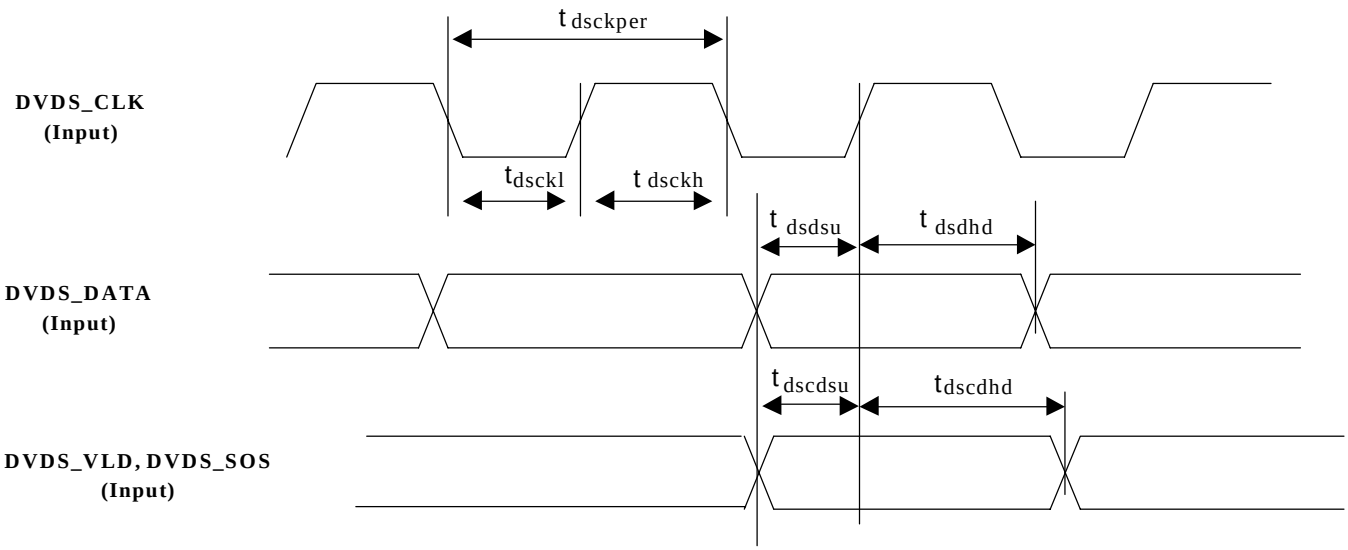


Figure 7. DVD Serial Interface Timing

2.2.4 SDRAM Interface

CS98200 interfaces with either SDRAM or SGRAM for high data bandwidth transfer. Figure 8 shows the refresh cycle performed by CS98200.

Symbol	Description	Min	Typ	Max	Unit
t_{mco}	Output Delay from M_CKO active edge			9	ns
t_{mper}	M_CKO Period	8			ns
t_{mdow}	M_D[31:0] delay from M_CKO			9	ns
t_{msur}	M_D[31:0] setup to M_CKO	3			ns
t_{mhr}	M_D[31:0] hold time after M_CKO	2.5			ns

Table 2. SDRAM Interface Characteristics

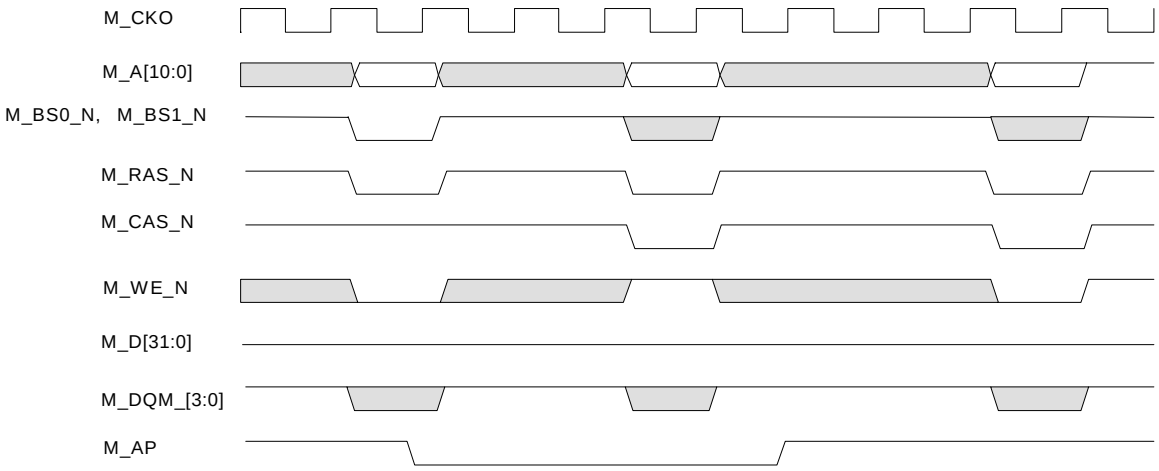


Figure 8. SDRAM Refresh Transaction

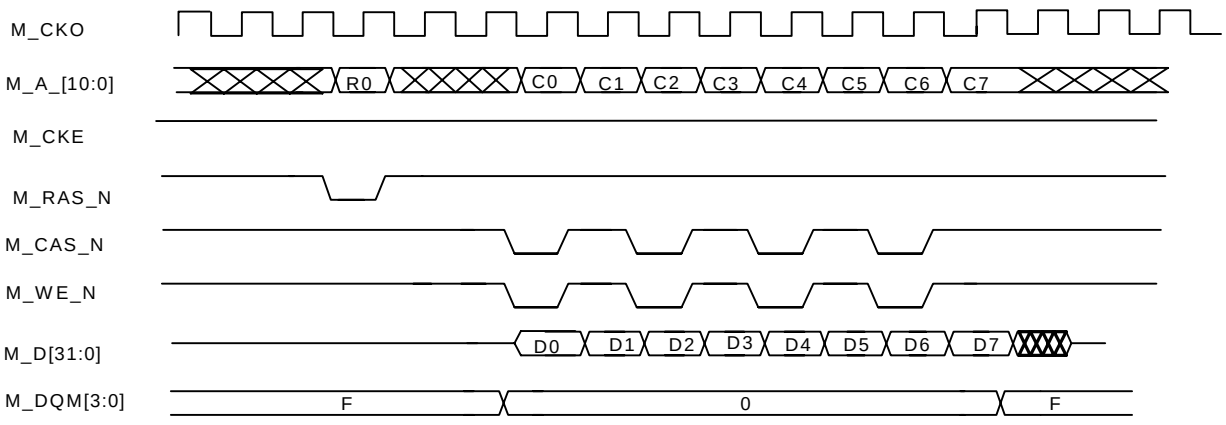


Figure 9. SDRAM Burst Write Transaction

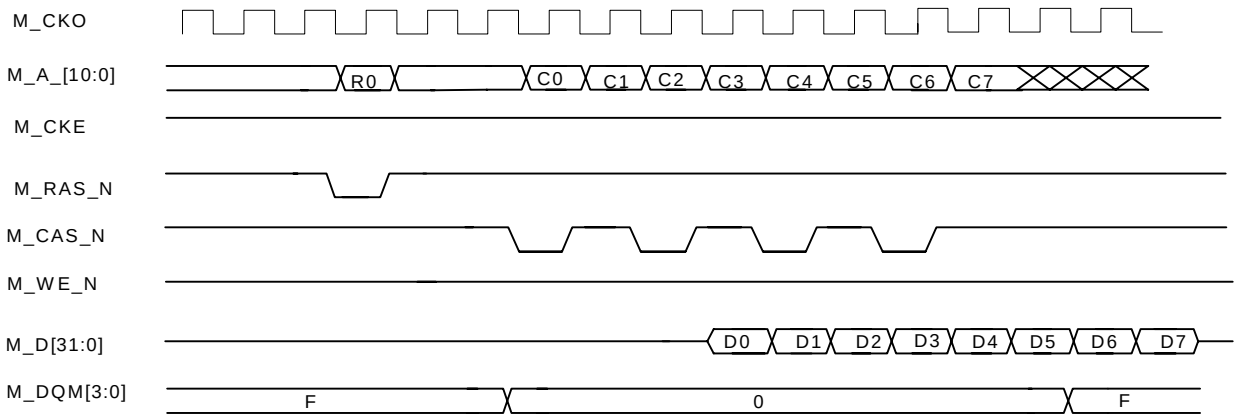


Figure 10. SDRAM Burst Read Transaction

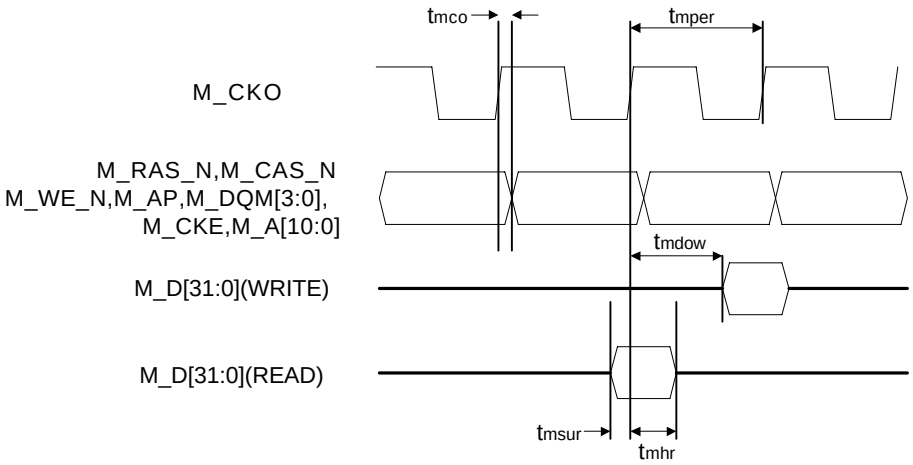


Figure 11. SDRAM Timing

2.2.5 ROM/NVRAM Interface

Symbol	Description	Min	Typ	Max	Unit
t_{rc}	Read Cycle Time	75			ns
t_{cds}	CE to Data Setup			80	ns
t_{ods}	OE to Data Setup			70	ns
t_{ads}	Address to Data Setup			80	ns
t_{aws}	Address to WE setup (Write)	64			ns
t_{cws}	CE to WE setup (Write)	64			ns
t_{wp}	WE Pulse Width (Write)	160			ns
t_{cdo}	CE to Data Output (Write)		0		ns
t_{dh}	WE to Data Hold (Write)	10			ns

Table 3. RAM/NVROM Characteristics

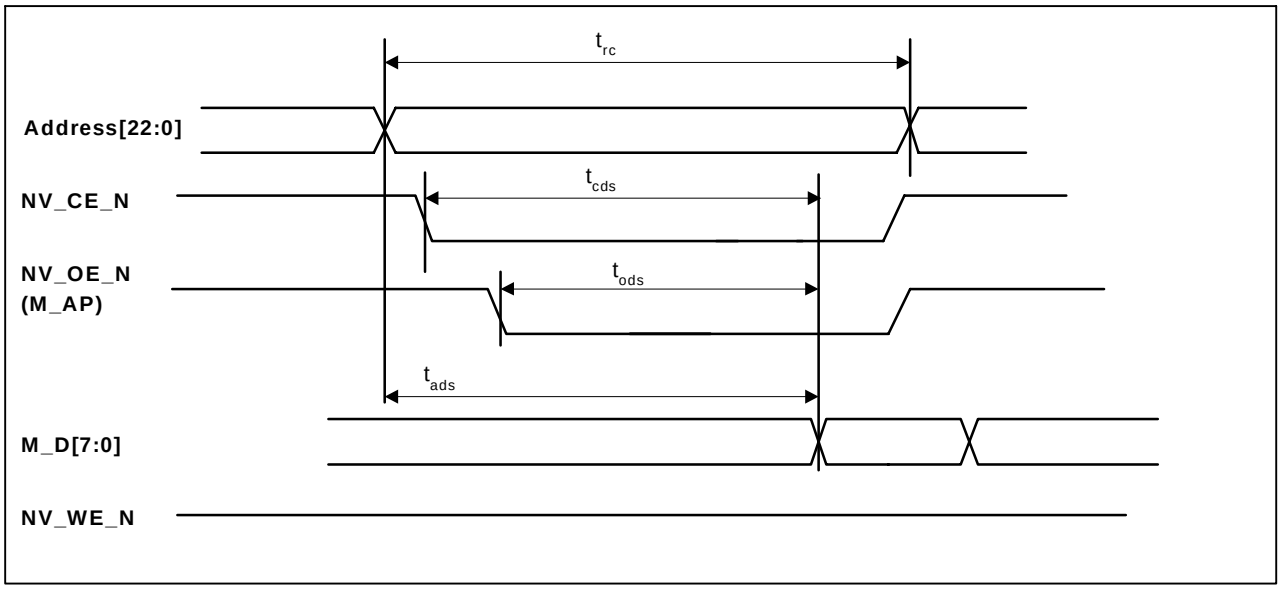


Figure 12. ROM/NVRAM Reading Timing

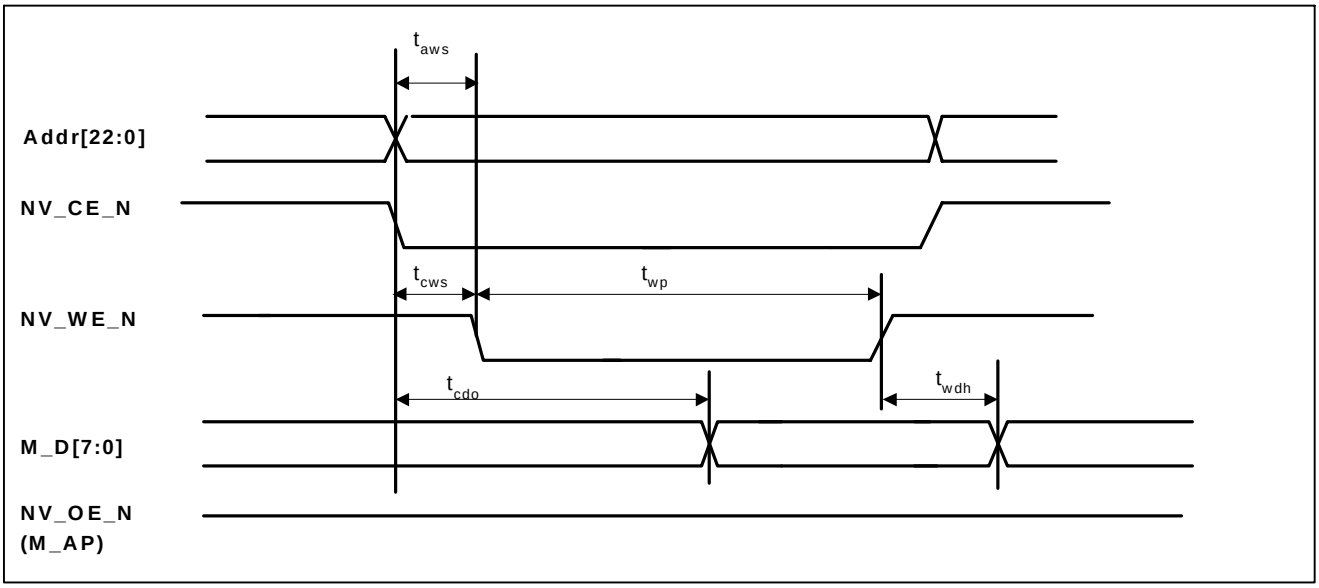


Figure 13. ROM/NVRAM Write Timing

2.2.6 Digital Video Output Interface

Figure 14 illustrates the signal timing for the digital video interface pins.

Symbol	Description	Min	Typ	Max	Unit
t_{vocper}[1]	XTLCLK period		37.037		ns
t_{covo1}[2]	VDAT[7:0] delay from XTLCLK	-10		10	ns
t_{covo2}[2]	Vsync/Hsync delay from XTLCLK	-10		10	ns

Table 4. CS98200 Digital Video Interface Characteristics

1. Values are guaranteed by design only
2. It is recommanded that the output data should be taken at the opposite edge of the CLK27_O.

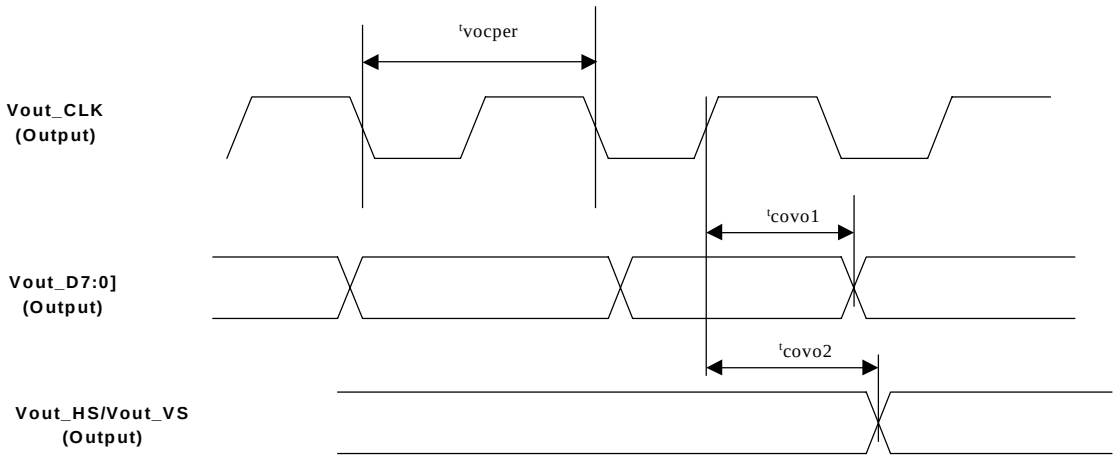


Figure 14. CS98200 Digital Video Interface Timing Diagram

2.2.7 Video Input Interface

Symbol	Description	Min	Typ	Max	Unit
t_{vicper}	Video Clock input period		37.037		ns
t_{sutc1}	VIN_D[7:0] setup time	5			ns
t_{hvi}	VIN_D[7:0] hold time	5			ns
t_{sutc2}	VIN_HS/VS setup time	5			ns

Table 5. Video Input Interface Symbols and Characterization Data

.

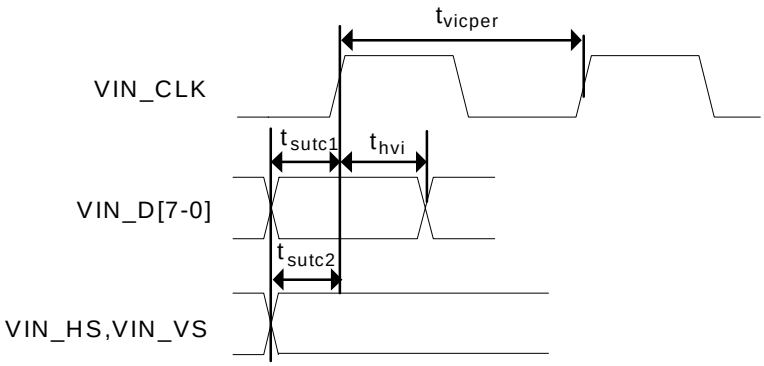


Figure 15. Video Input Timing

2.2.8 Audio Input Interface Timing

Symbol	Description	Min	Typ	Max	Units
t_{aicl}	AUDI_BCK Low Time[1, 2]	40	50		%
t_{aich}	AUDI_BCK High Time[1, 2]	40	50		%
t_{aiper}	AUDI_BCK period[1, 2]	80			ns
t_{lrts}	AUDI_LR setup time	5		-	ns
t_{sdsus}	AUDI_D setup time	5		-	ns
t_{sdhs}	AUDI_D hold time	5		-	ns

Table 6. Audio Input Interface Symbols and Characterization Data

1. Values are guaranteed by design only
2. Active clock edge is programmable. Timing is referenced from active edge

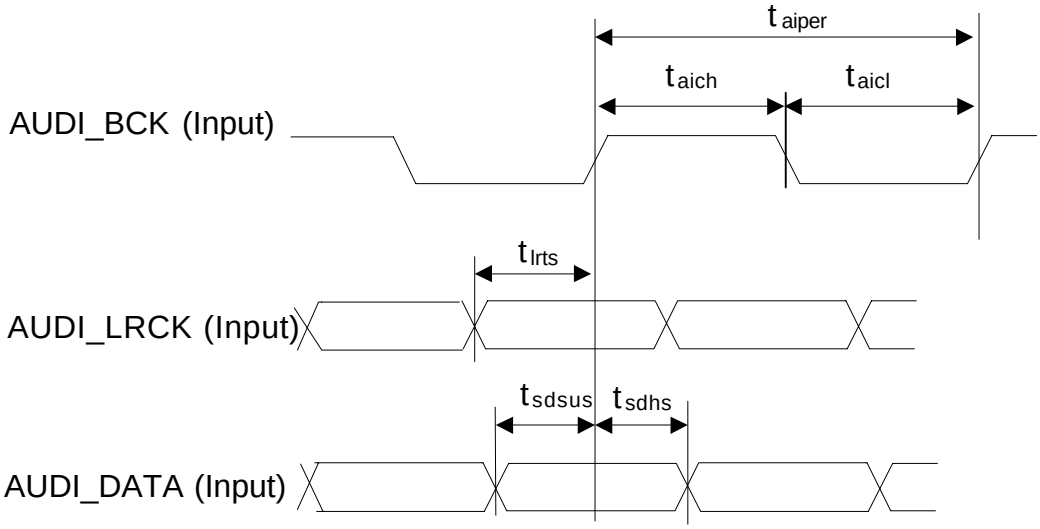


Figure 16. Audio Input Timings

2.2.9 Audio Output Interface Timing

Figure 17 and Figure 16 illustrate the signal timing for the digital audio pins.

Symbol	Description	Min	Typ	Max	Unit
t_{axper}	AUD_XCLK period (Input/Output)[1, 2]	13		-	ns
t_{axch}	AUD_XCLK High Time (Input/Output)[1, 2]	40	50		%
t_{axcl}	AUD_XCLK Low Time (Input/Output)[1, 2]	47	50		%
t_{sdmo}	AUDO_BCK delay from AUD_XCLK output rise			10	
t_{sdmi}	AUDO_BCK delay from AUD_XCLK input rise			20	
t_{aoper}	AUDO_BCK period (Output)[1, 2]	104			
t_{lrds}	AUDO_LR delay from AUDO_BCK output rise	-10		10	ns
t_{adsm}	AUDO_D[3:0] delay from AUDO_BCK output rise	-10		10	ns

Table 7. Digital Audio Out Characteristics

1. Values are guaranteed by design only
2. Active clock edge is programmable. Timing is referenced from active edge

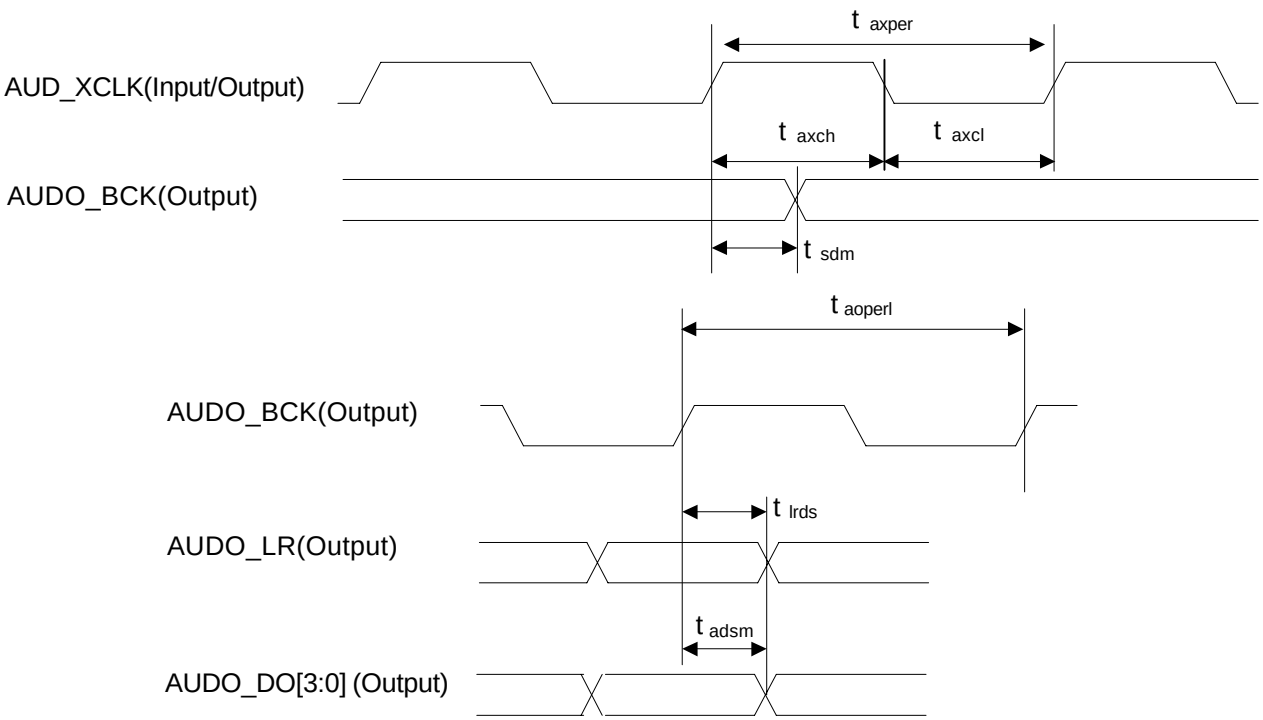


Figure 17. Digital Audio Out Timing Diagram

2.2.10 Miscellaneous Timings

Symbol	Description	Min	Typ	Max	Unit
t_{xccper}[1]	XTLCLK period		37.037		ns
t_{rstl}	RST_N Low Pulse Width	1000			ns
t_{gph}	GPIO PW High	50			ns
t_{gpl}	GPIO PW Low	50			ns

Table 8. Miscellaneous Timing Characteristics

1. XTLCLK must meet the requirement of external the video encoder for correct chroma (27 MHz ± 1 KHz).

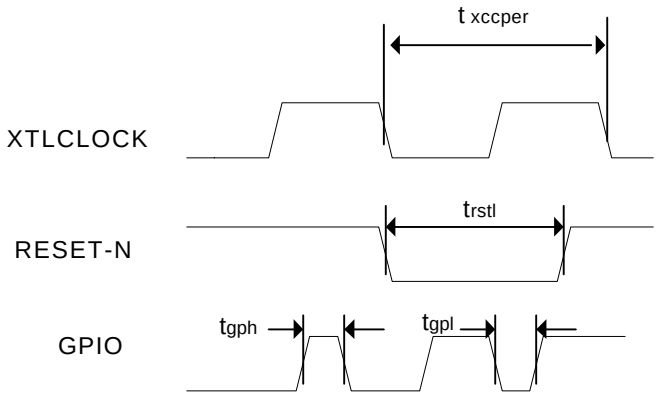


Figure 18. Miscellaneous Timings

3. TYPICAL APPLICATION

The Figure 19 shows a typical example of a complete DVD Receiver solution using the CS98200.

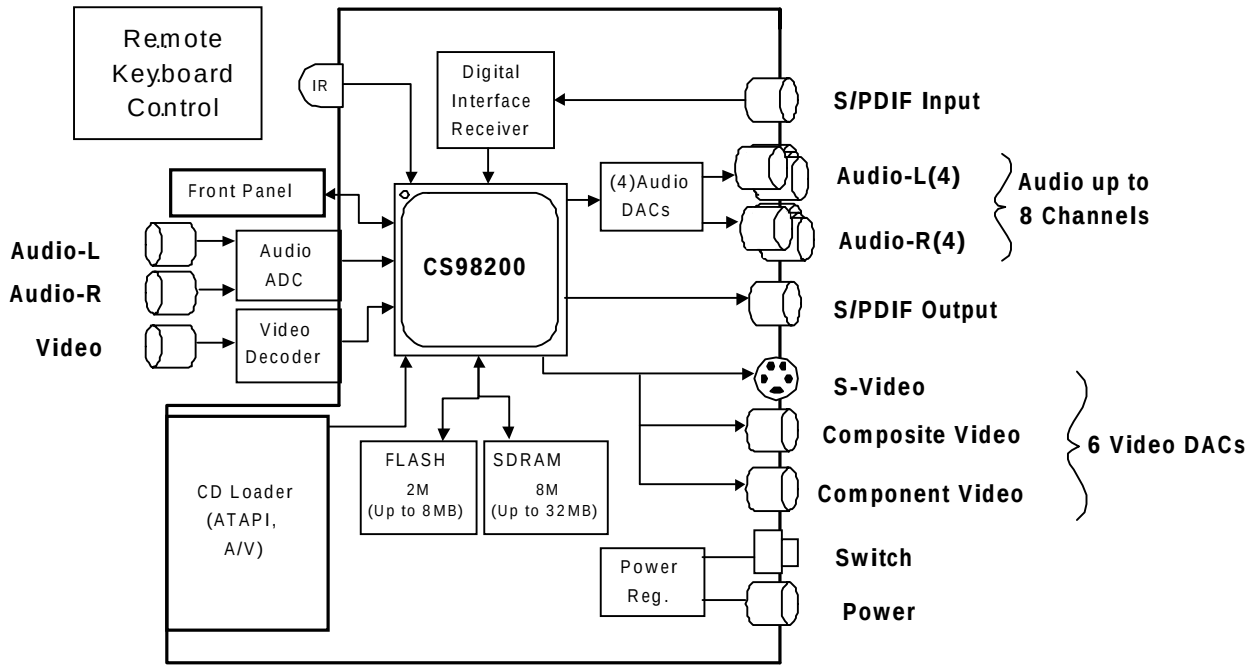


Figure 19. CS98200 Typical Application

4. CS98200 DEVICE SUMMARY

4.1 Block Diagram

The CS98200 block diagram is shown in Figure 20.

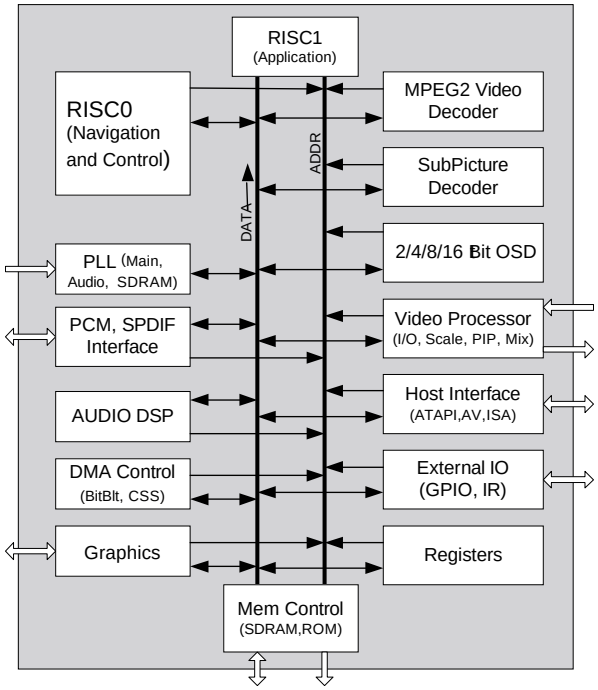


Figure 20. CS98200 Block Diagram

4.2 CS98200 Device Details

4.2.1 RISC-32 Processors

- Two Powerful 32-bit RISC processors (RISC0 and RISC1), Generation III
- Virtual memory support
- Optimizing C compiler
- Big or little endian data formats support
- MAC multiply/accumulate in 2 cycles with C support
- 4 Kbyte instruction cache, 2 Kbyte data cache
- Single cycle instructions, runs at 180 Mhz

4.2.2 Powerful 24/32-Bit DSP

- Powerful 24/32-bit DSP processor
- 24-bit fixed point logic, with 54-bit accumulator
- Single-cycle throughput, 2-cycle latency multiply accumulate, 32-bit simple integer logic. 8-Kbyte instruction cache
- Single cycle instructions, runs at 180 Mhz
- Expanded 4 Kbyte X + 16 KByte Y paged program visible local memory, Total data RAM = 20 KBytes

4.2.3 System Controls

- Includes several hardware lockable semaphore registers
- General-purpose register for inter-processor communication
- 32-bit timers for I/O and other uses, with programmable interval rates
- Both hardware and software interrupts on data or debug
- Built in PLLs generate all required clocks from 27 Mhz input clock

4.2.4 Memory Controller

- Supports standard SDRAM and SGRAM, 32-bit data mode only, from 4 MByte to 32 MByte
- Includes a separate dedicated DRAM clock, so memory can run asynchronous to the system clock

- High speed, can handle up to 120 MHz DRAM speeds
- Supports 8-bit parallel ROM or FLASH, up to 8 MB
- Single bank of SDRAM only. Single bank of ROM / FLASH only
- Separate data bus for ROM, reduces loading for improved speed, Also handles 5 V easier.

4.2.5 Data Flow Engine

- 2432 bytes of internal memory
- DMA to / from main RAM into local SRAM
- Supports endian conversion and byte, short, long data formats on DMA
- Supports block transfers for graphics bit blits

4.2.6 MPEG Video Decoder

- Supports VCD, VCD 2.0, DVD video standards
- Supports trick features, including smooth 2x play and reverse play
- Special anti-tearing logic controls picture decode and presentation
- Advanced error concealment hardware
- New acceleration modules for MPEG-4 Simple Profiles support

4.2.7 System Synchronization

- System time clock (STC) for audio / video synchronization
- Flexible interrupt structure for controlling decode and presentation times
- Hardware scheduling of subpicture and highlight events

4.2.8 Audio Interface

- Supports 8 channels PCM output at up to 24 bits and 192 kHz output rate.
- Supports 2 channels I^2S input at up to 24 bits and 96 kHz input rate.
- Simultaneous IEC-958 (SPDIF) output with programmable channel status and user data.
- SPDIF, PCM input, and PCM output can all have different XCLK dividers.
- Supports simultaneous 192 Khz front and 96 Khz surround, for DVD audio

4.2.9 Video Input

- NTSC / PAL video decoder input interface
- Video input image can be displayed in small window, or as main picture

4.2.10 External Interface

- Serial I^2C® master and slave port
- 29 independent fully programmable bi-directional I / O pins
- 8 edge or level detection interrupt pins
- Hardware assisted support for infrared remote devices, such as remote control, infrared keyboard
- Dual UART

4.2.11 Video Processor

- Supports 24-bit 4:2:0 and 4:2:2 video modes and 16-bit true color graphics modes.
- Picture-in-picture module includes horizontal and vertical downscaling with programmable output sizes, positions, and borders
- Overlay mixer with RGB to YUV conversion and output formatting
- Supports 4:2:0, 4:2:2, YUV655, RGB565 and RGB555 frame buffer inputs
- Outputs 4:2:2 video in CCIR-601 or CCIR-656 format
- High quality scaling using a vertical and a horizontal 16 taps polyphase programmable filter and supports any size image up to 768x576
- 3 taps adaptative anti-flicker filtering
- Master or Slave video sync configuration
- Multiple video plains overlay (main video / video input / picture_in_picture / picture / on-screen / display)
- Gamma correction

4.2.12 Sub-Picture Processor

- Run-length decode DVD sub-pictures
- Hardware vertical scaling supports NTSC-PAL format conversion
- 16-level alpha blending

4.2.13 Graphics Engine

- 16 bit true color
- Progressive and interlaced mode support

- Supports gamma correction
- Color-key type transparency support
- Global blending support
- Frame buffer wrap around support for scrolling
- 3 tap horizontal and vertical filtering

4.2.14 On Screen Display Module

- Supports 2-bit and 4-bit pixel modes
- 3 separate regions support
- 16 transparency overlay levels support

4.2.15 DVD Loader Interface

- 4-pin serial interface to low-cost DVD loaders
- Loader control via separate 2-wire serial master control port
- IO channel interface supports standard 8 bit DVD loader protocols

4.2.16 CPU Interface and SRAM Controller

- Internal SRAM of 32 KByte, and controller, synchronous with the CPUs at 180 Mhz
- Fast interfaces to RISCs and DSP
- Asynchronous interfaces to the main system clock
- Special DMA engine, with multiple software clients, and command FIFO
- Special interface to MPEG-4 video module

4.2.17 Host Bus Interface

- Programmable parallel host master interface supports formats including ATAPI, ISA, and more
- Internal DMA module, for I/O type reads and writes on the host bus
- Extra chip selects, for more external devices

4.2.18 Video Encoder

- Six 10-bit video DACs, drive 37.5 W load directly without external buffering
- Supports PAL (B, D, G, H, I, N, M, 60) and NTSC
- Component (RBG or YUV) or composite + S-Video output
- Progressive or interlaced mode output
- Macrovision 7.1 support (interlaced) and Macrovision 1.03 support (progressive)
- Wide-screen signalling support (interlaced and progressive) and CGMS support
- Closed captioning support

4.2.19 System Functions

- 240-pin MQFP package
- All I/O pins are 3 V with 5V tolerance
- Advanced 0.18 micron CMOS technology
- Internal processors run at 180 MHz
- Supports Low Power modes and clock shut-off

5. FUNCTIONAL DESCRIPTION

5.1 RISC Processor

The CS98200 includes two powerful, third-generation proprietary 32-bit RISC processors, RISC0 and RISC1, with optimizing C compiler support and source level debugger. The RISC processors fully support many Real Time Operation Systems (RTOS). The DVD application user interface resides on RISC1 and is customer programmable. The real time control of low level DVD functions is performed by RISC0. RISC1 gains access to system resources controlled by RISC0 via calls through an Applications Programming Interface, See the *CS98200 Software API*. All RISC0 firmware, API and sample application code are supplied with the CS98200.

The RISC processors also have a MAC engine, which performs multiply/accumulate in 2 cycles in a pipelined fashion with C support, effectively achieving single cycle throughout. The RISC0 processor coordinates on-chip multithreaded tasks, as well as system activities such as remote control and front panel control. The DVD application end-user interface resides on RISC1, and any modifications to that interface occur through the CS98200 API.

5.2 DSP Processor

The CS98200 contains a proprietary digital signal processor (DSP), which is optimized for audio applications. The DSP performs 32-bit simple integer operations, and has a 24-bit fixed point logic unit, with a 54-bit accumulator. The multiply-accumulator has single-cycle throughput, with two cycle latency. The DSP is optimized for bit packing and unpacking operations. The interface to main memory is designed for handling flexible block sizes and skip counts.

5.3 Memory Control

The DRAM Interface performs the SDRAM control and arbitration functions for all the other modules in the CS98200. The DRAM interface services and arbitrates a number of clients and stores their code and/or data within the local memory. This arbitration and scheduling guarantees the allocation of sufficient bandwidth to the various clients. The DRAM Interface supports up to 32 Mbytes. For a typical DVD player application, CS98200 requires 8 Mbytes memory space.

Sharing the same interface, CS98200 also supports FLASH ROM, OTP, or mask ROM interface. Code is stored in ROM. After the system is booted, the code is shadowed inside SDRAM for execution. The FLASH ROM interface is provided so that the code can be upgraded in the field once the communications channel is established. Utility software will be provided to debug and upgrade code for the system manufacturer.

5.4 Dataflow Control (DMA)

The DMA controller moves data between the external memory and internal memory. The external memory address can be specified using a register, or in FIFO mode, using start and end address registers. Separate start/end address registers are used for DMA read and write operations. The DMA interface also has a block transfer function, which allows for the transfer of one block of data from one external memory location to another external memory location. In effect, this feature combines a DMA read and write into one operation. In addition, the DMA write operation allows for byte, short, word, and other types of masking.

5.5 System Control Functions

The system control functions are used to coordinate the activities of the multiple processors, and to provide the supporting system operations. Eight 32-bit communication registers are available for inter-processor communication, and 32 semaphore registers are used for resource locking. Timers are available for general-purpose functions, as well as more specialized

functions such as watchdog timers and performance monitoring.

The large number of general purpose I/Os offers flexibility in system configurations. An I^2C master allows for control of other I^2C devices, such as a video encoder. An I^2C slave port shares the same pins, and can be used for debug functions. Interrupts can be generated on specific or generic events. Infrared inputs can be filtered to make them free of glitches or stored unfiltered into memory. Control of all the internal clocks is also possible. There are two separate PLLs that are clocked by the 27 MHz clock input. One PLL generates the main clock and DRAM interface clock, and the second generates the Audio 256X/384X clock.

5.6 DVD/ATAPI Interface

The CS98200 has a programmable interface port which can be configured to connect to industry standard CD/DVD loaders without external glue logic. The CD/DVD interface fully supports many popular CD/DVD loaders. The interface consists of DVD control and data ports and an optional CD control/data port.

The CS98200 hardware manages the DVD interface and moving data to an arbitrary size input FIFO in DRAM. The same interface pins can be optionally configured as a generic 16-bit host master port. In this mode, the CS98200 can control up to four devices (using 4 chip select outputs), each of which may use different protocol and timing. The interface can be set up in ATAPI mode, to connect directly to any
ATAPI DVD loader (using two chip selects). Simultaneously, the other two chip selects can be configured to connect to other devices, such as a super I/O chip or hard disk.

A third option is to configure the interface for micro-less DVD loader operation, which may also be configured to connect without external glue logic.

5.7 Serial DVD Interface

The CS98200 has a 4-pin serial port which interfaces to the data port of popular low-cost DVD loaders. This type of loader provides for low system cost by eliminating the track buffer, interface FIFO, and flow control logic. The CS98200 contains a large internal SRAM to handle high burst data rates, without requiring reverse flow control. The CS98200 performs error detection, sector number tracking, and interrupt generation.

5.8 MPEG Video Decoding

Compressed MPEG data is read from the DVD disk into an input FIFO in DRAM. The data flow (DMA) controller moves Video packets from the input FIFO into the MPEG decoder's input FIFO (also in DRAM). The DMA controller can also perform advanced functions such as start code search, relieving the RISC processors. The System Synchronization function is used to control the timing of MPEG picture decoding. The MPEG Video decoder processes I, B, and P frames, and writes to video frame buffers in DRAM for output to the display. Special anti-tearing logic ensures that currently displayed frame buffers are not overwritten.

5.9 Audio Processing

Compressed Audio data is read from the DVD disk into an input FIFO in DRAM. The data is decompressed, then written to a PCM output FIFO, also in DRAM. Presentation time stamps (PTS) are extracted from the stream to update the STC, in order to maintain audio/video synchronization.

The DMA and decompression stages of audio processing can be done with a combination of the DMA unit, DSP, and RISC processors. The DSP is optimized for audio processing, so most common formats can be handled by the DSP alone, including AC-3, DTS, MPEG2 audio, and MP3. The DSP has enough reserve bandwidth

to handle the Karaoke echo-mix and pitch shift, and AC-3 down-mix functions.

The audio output data is written into a DRAM FIFO in 16-, 18-, 20- or 24-bit PCM format. A flexible audio output stage can simultaneously output 8 channels of PCM data to audio DACs up to 192 KHz sample rate, plus an IEC-958 encoded output at up to 48 KHz. The audio interface also includes a flexible audio input interface, which can input a wide range of protocols from an audio ADC or an IEC-958 receiver at up to 96 KHz.

5.10 Video Encoder with Progressive Video DACs

The CS98200 incorporates an enhanced video encoder with six 10-bit video DACs that drive double terminated 75 Ω directly without external buffering. These termination resistors should be located as close as possible to the CS98200. All analog video outputs should be connected through filters to video connectors (TV / Monitor). The video filters should be located as close as possible to the video connectors. Two schottky diodes should be connected to each output in order to protect the CS98200 from surges caused by being connected and disconnected to the external devices. Figure 21 shows the video DAC connections.

Six 10-bit DACs provide two channels for an S-Video output port, one composite video output, and three RGB or Y, Pb, Pr outputs. Video output can be formatted to be compatible with NTSC (M,J), PAL (B, D, G, H, I, M, 60), and 480P. The video encoder is compliant with both Macrovision 7.1 for the interlaced video (NTSC, PAL) and 1.03 for the progressive scan (480p).

The video encoder also supports WSS (Wide-Screen Signaling), CGMS (Copy Generation Management System), and Closed Caption.

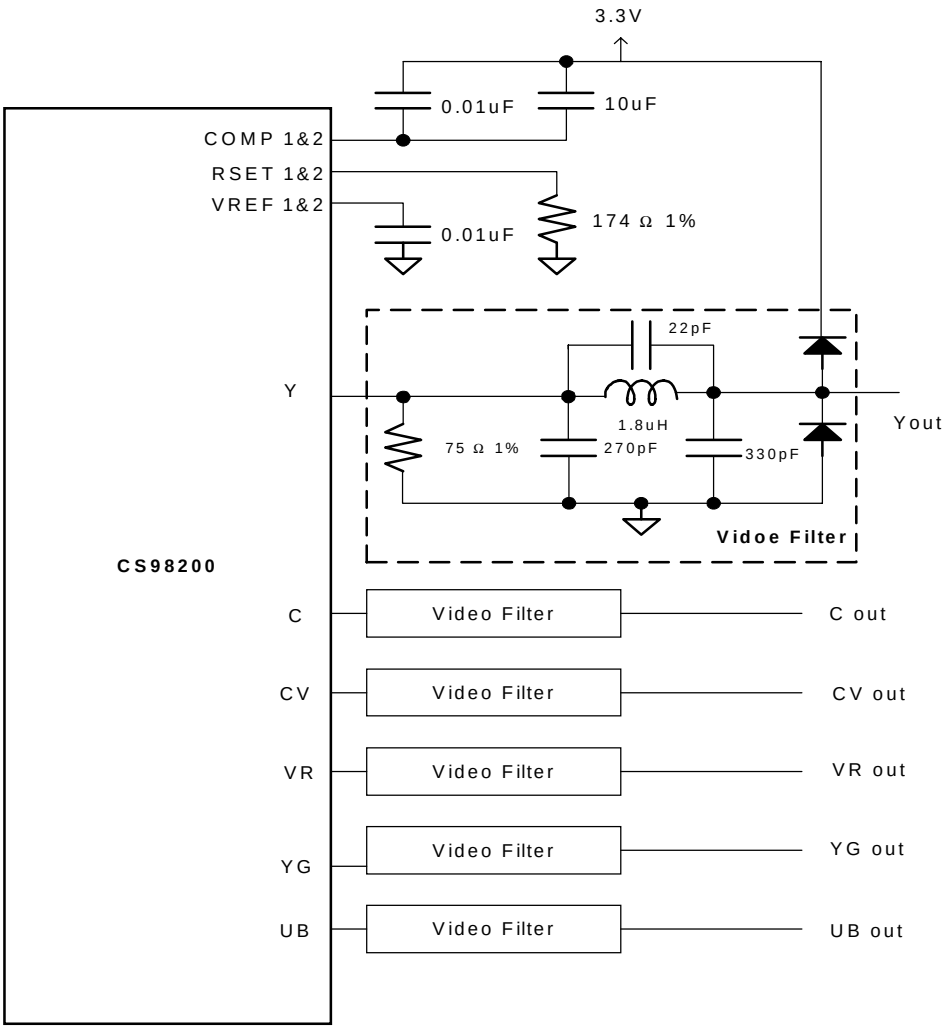


Figure 21. Video DAC Connections

5.11 Video Input/Output Interface

In addition to the six 10-bit video DACs, the CS98200 provides a separate Digital Video Interface that will give you flexible and powerful means of outputting digital video data to external devices in CCIR601/3 and CCIR656 formats. The interface directly supports NTSC/PAL video encoding, in both master and slave synchronization configurations. The internal frame buffer format could be 4:2:0, 4:2:2, YUV655, RGB565 and RGB555.

The CS98200 also features an NTSC/PAL video decoder input interface. The interface accepts CCIR601, CIF, and QCIF formats, out of many TV decoders on the market. The video processor also allows overlay of multiple video planes (main video / video input / picture_in_picture / on-screen display).

The Video Input Scaler (VIS) module inputs 8-bit digital video data from a camera or PAL/NTSC decoder and simply dump all the data to DRAM. The scaled image, with a border, can be overlaid anywhere on the screen into a ½ or ¼-screen sized window by the Picture in Picture (PIP) module.

An alternate method of using the Video Input function is to input a full sized picture and present it on the screen full size (bypass mode). In this mode, the PIP module can place full motion DVD images in the small window. An internal glitch-free mux can switch the video processor clock source from the internal clock to the Video Input clock, allowing the PIP mode to switch back and forth on the fly, with no drop-out.

5.12 Universal Asynchronous Receiver/Transmitters (UARTs)

The UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the host processor. Figure 22 shows RXD and TXD data transfers over the UART interface.

The CS98200 has 2 UART interfaces based on a NS16550-compatible design, which incorporates 16-byte transmit and receive FIFOs to enhance performance and throughput. As with the 16650, it can operate in both FIFO-mode (16550) or in the original non-FIFO mode (16450). The main registers are identical in structure to the NS16550, but some unused bits have been enabled for added functionality.

The standard features are:

- Compatible with 16450 UART
- 16-byte transmit and receive FIFOs reduce number of interrupts presented to CPU
- Generates and detects standard asynchronous communication bits (start, stop and parity) to and from serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud rate generator (16 bit divisor)
- Modem control interface (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial-interface characteristics:
  - 5, 6, 7 or 8 bit characters
  - Even, odd or no-parity bit generation / detection
  - 1, 1½, or 2 stop bit generation
- False start bit detection
- Complete status reporting capabilities
- Line break generation and detection
- Internal loopback diagnostic mode
- Programmable trigger levels for FIFOs
- Selectable DMA signaling mode
- Prioritized interrupts
- Transmitter and receiver FIFO time-out interrupts

Additional optimizations:

- Byte enable register allows transfer of up to 4 bytes in a single register write (only in FIFO mode).
- External loopback diagnostic mode
- Separate baud clock input available
- Additional receiver error information

Note: If using separate baud clock, it must be less than ½ frequency of the system clock, otherwise, you must use the system clock.

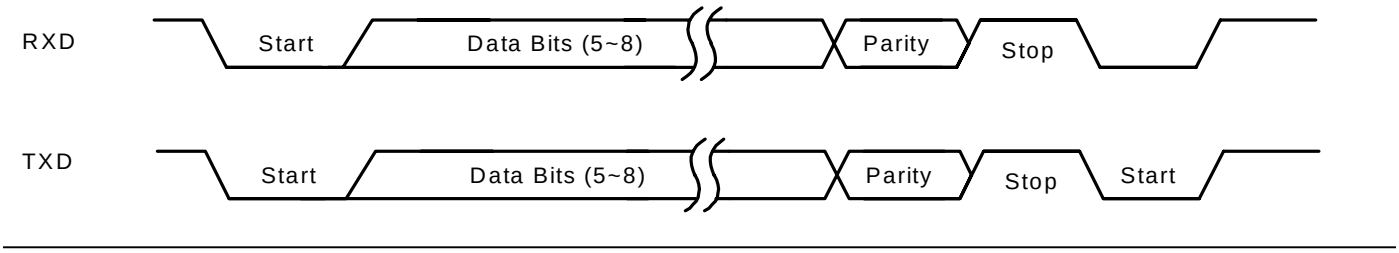


Figure 22. UART Data Transfer

6. MEMORY MAP

6.1 Processor Memory Map

The CS98200 externally supports up to 32 Mbytes DRAM and 16 Mbytes ROM / NVRAM. Table 9, Table 10, and Table 11 on the next page list the memory map as viewed by the RISC processors, and identifies whether each segment is mapped or cacheable.

For detailed information on programming CS98200 memory, see *CS98200 Memory Interface User's Manual* (DS525UMD1).

Address	Description	Cached
0x8000_0000 - 0x8000_7FFF	Internal SRAM (32 Kbytes)	Yes
0x8200_0000 - 0x83FF_FFFF	External DRAM (32 Mbytes)	Yes
0x9400_0000 - 0x97FF_FFFF	External DRAM w/ Dcache flush (32 Mbytes)	Yes
0x9800_0000 - 0x9BFF_FFFF	External ROM/NVRAM read/write (16 Mbytes)	Yes
0x9C00_0000 - 0x9FFF_FFFF	External ROM/NVRAM read only (16 Mbytes)	Yes
0xA000_0000 - 0xA000_7FFF	Internal SRAM (32 Kbytes)	No
0xA200_0000 - 0xA3FF_FFFF	External DRAM (32 Mbytes)	No
0xB000_0000 - 0xB003_FFFF	Internal registers and SRAMs	No
0xB400_0000 - 0xB7FF_FFFF	External DRAM w/ Dcache flush (32 Mbytes)	No
0xB800_0000 - 0xBBFF_FFFF	External ROM/NVRAM read/write (16 Mbytes)	No
0xBC00_0000 - 0xBFFF_FFFF	External ROM/NVRAM read only (16 Mbytes)	No

Table 9. Memory Map-RISC0 Processor

Host Byte Address	Description
0x0000_0000 - 0x0003_FFFF	Internal registers and SRAMs
0x1000_0000 - 0x11FF_FFFF	External DRAM (32 Mbytes)
0x1200_0000 - 0x13FF_FFF	Internal SRAM
0x1400_0000 - 0x14FF_FFFF	External ROM/NVRAM space (16 Mbytes)

Table 10. Host Debug Port Address Map

Byte Address Offset	Description
0x0000_0000 - 0x0003_FFFF (I/O space)	Internal Registers and SRAMs
0x0000_0000 - 0x01FF_FFFF (memory space)	External DRAM (32 Mbytes)
0x0200_0000 - 0x0200_7FFF (memory space)	Internal SRAM (32 Kbytes)

Table 11. DSP Address Map

7. 240-PIN MQFP PIN DESCRIPTION

7.1 240-Pin MQFP Pin Layout

Figure 23 shows the layout of all the pins for the 240-pin MQFP package. The direction of the arrow by each pin shows whether the pin is an input, output, or bidirectional.

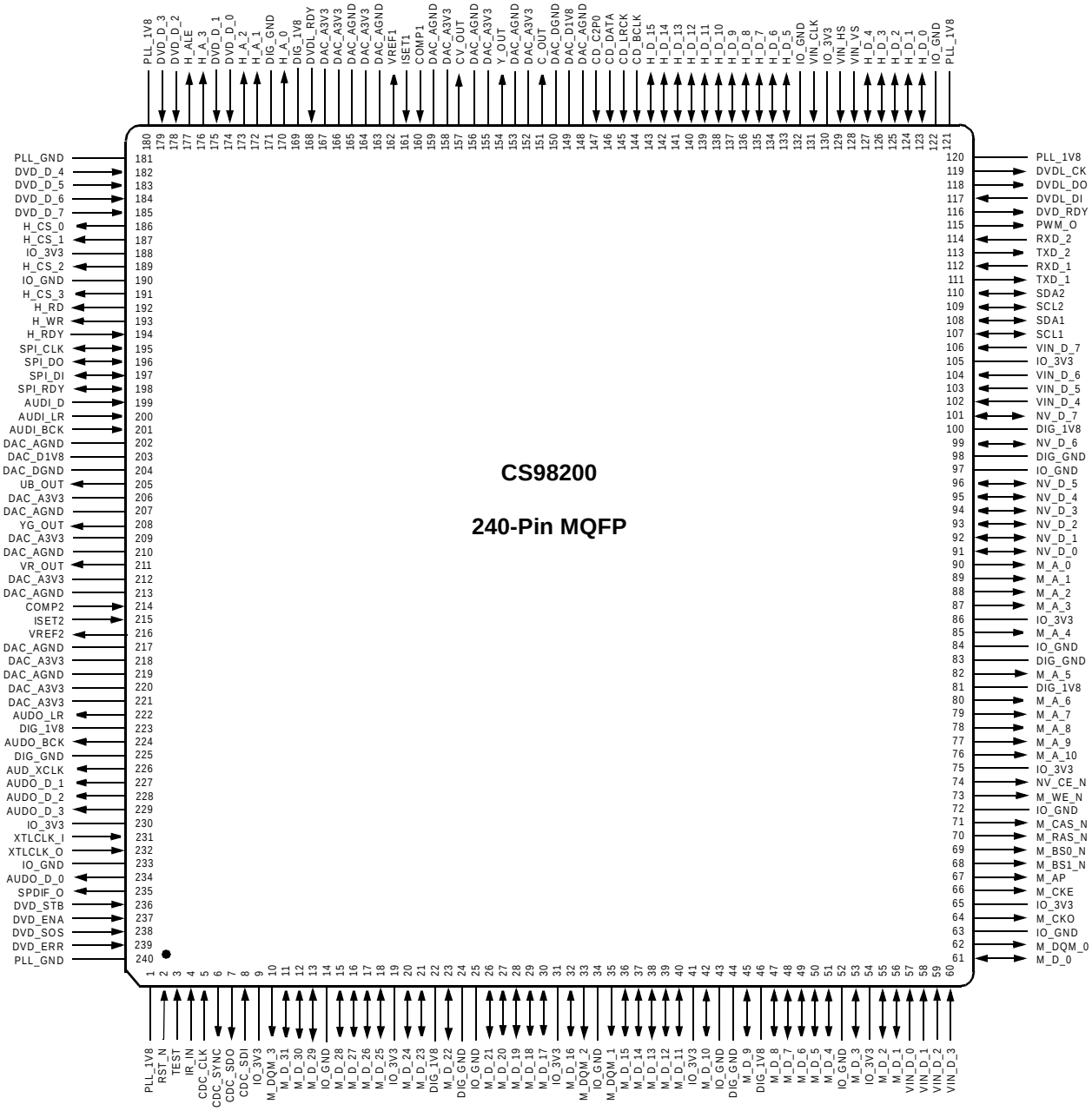


Figure 23. 240-Pin MQFP Pin Layout

7.2 240-Pin MQFP Pin Summary

Figure 24 shows the pin names associated with each type of CS98200 interface.

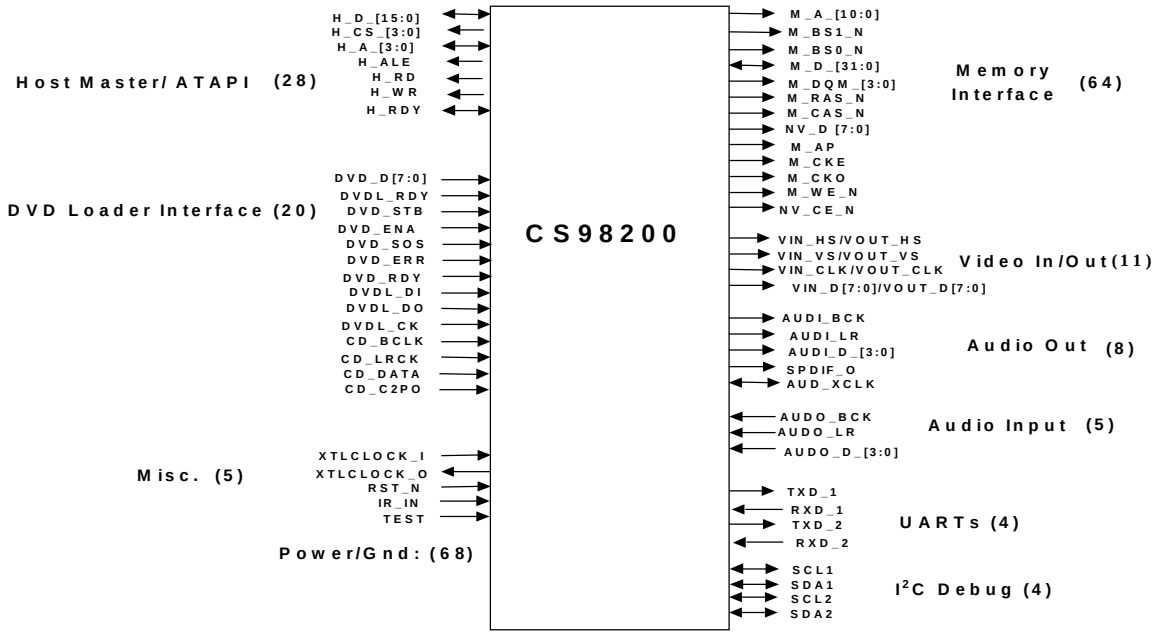


Figure 24. 240-Pin MQFP Pinout Summary

7.3 Pin Configuration Summary

The CS98200 has flexible pin functionality. Table 12 lists the different possible pin configurations and the settings required. The IO_Set value is programmed through a register, while the AUDO_D_0 and AUDO_LR values are set through pull up or pull down resistors on the pins.

IO_Set[1:0]	AUDO_D_0	AUDO_LR	Host/ATAPI Pins	Video In/Out Pins	DVD Pins
00	1	X	Host master mode	Video in mode	DVD mode
00	0	0	Host slave mode	Video in mode	DVD mode
00	0	1	Host master mode	Video in mode	Host slave mode
01	1	X	Host master mode	Video out mode	Video in mode
01	0	0	Host slave mode	Video out mode	Video in mode
01	0	1	Host master mode	Video out mode	Host slave mode
10	1	X	DVD mode	Video in mode	GPIO mode
10	0	0	Host slave mode	Video in mode	GPIO mode
10	0	1	DVD mode	Video in mode	Host slave mode
11	1	X	DVD mode	Video out mode	Video in mode
11	0	0	Host slave mode	Video out mode	Video in mode
11	0	1	DVD mode	Video out mode	Host slave mode

Table 12. Pin Configuration Summary

7.4 Explanation of Pin Types

Table 13 lists the conventions used to identify the pin type and direction.

Pin Type	Direction
I	Input
IS	Input, with schmitt trigger
ID	Input, with pull down resistor
IU	Input, with pull up resistor
O	Output
O4	Output – 4 mA drive
O8	Output – 8 mA drive
T4	High-Z Output – 4mA drive
B	Bi-direction
B4	Bi-direction – 4 mA drive
B4U	Bi-direction – 4 mA drive, with pull-up
B8U	Bi-direction – 8 mA drive, with pull-up
B4S	Bi-direction – 4 mA drive, with Schmitt trigger
B4SU	Bi-direction – 4 mA drive, with pull-up and Schmitt trigger
Pwr	+1.8 V or +3.3 V power supply voltage
Gnd	Power supply ground
Name_N	Low active

Table 13. Pin Type Legen d

7.5 240-Pin MQFP Pin Assignments

Table 14 lists the pin number, pin name, and pin type for the 240-pin CS98200 package. The primary function and pin direction is shown for all signal pins. For some signal pins, a secondary function (or functions) and direction are also shown. For pins having more than one function, the primary function is chosen when the chip is reset.

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
1	PLL_1V8	Pwr	PLL Power 1.8 V			
2	RST_N	ISU	Reset	I		
3	TEST	I	Manufacturing Test	I		
4	IR_IN	ISU	IR in	I		
5	CDC_CLK	B4S	GPIO_MIS[18]	B		
6	CDC_SYNC	B4S	GPIO_MIS[19]	B		
7	CDC_SDO	B4S	GPIO_MIS[20]	B		
8	CDC_SDI	B4S	GPIO_MIS[21]	B		
9	IO_3V3	Pwr	IO Power 3.3 V			
10	M_DQM_3	B8	DRAM Byte_Enable[3]	O		

Table 14. 240-Pin MQFP Pin Assignments

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
11	M_D_31	B8	DRAM Data[31]	B		
12	M_D_30	B8	DRAM Data[30]	B		
13	M_D_29	B8	DRAM Data[29]	B		
14	IO_GND	Gnd	IO Ground			
15	M_D_28	B8	DRAM Data[28]	B	NVRAM Address[23]	O
16	M_D_27	B8	DRAM Data[27]	B	NVRAM Address[22]	O
17	M_D_26	B8	DRAM Data[26]	B	NVRAM Address[21]	O
18	M_D_25	B8	DRAM Data[25]	B	NVRAM Address[20]	O
19	IO_3V3	Pwr	IO Power 3.3 V			
20	M_D_24	B8	DRAM Data[24]	B	NVRAM Address[19]	O
21	M_D_23	B8	DRAM Data[23]	B	NVRAM Address[18]	O
22	DIG_1V8	Pwr	Digital Power 1.8 V			
23	M_D_22	B8	DRAM Data[22]	B	NVRAM Address[17]	O
24	DIG_GND	Gnd	Digital Ground			
25	IO_GND	Gnd	IO Ground			
26	M_D_21	B8	DRAM Data[21]	B	NVRAM Address[16]	O
27	M_D_20	B8	DRAM Data[20]	B	NVRAM Address[15]	O
28	M_D_19	B8	DRAM Data[19]	B	NVRAM Address[14]	O
29	M_D_18	B8	DRAM Data[18]	B	NVRAM Address[13]	O
30	M_D_17	B8	DRAM Data[17]	B	NVRAM Address[12]	O
31	IO_3V3	Pwr	IO Power 3.3 V			
32	M_D_16	B8	DRAM Data[16]	B	NVRAM Address[11]	O
33	M_DQM_2	B8	DRAM Byte_Enable[2]	O		
34	IO_GND	Gnd	IO Ground			
35	M_DQM_1	B8	DRAM Byte_Enable[1]	O		
36	M_D_15	B8	DRAM Data[15]	B		
37	M_D_14	B8	DRAM Data[14]	B		
38	M_D_13	B8	DRAM Data[13]	B		
39	M_D_12	B8	DRAM Data[12]	B		
40	M_D_11	B8	DRAM Data[11]	B		
41	IO_3V3	Pwr	IO Power 3.3 V			

Table 14. 240-Pin MQFP Pin Assignments (Continued)

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
42	M_D_10	B8	DRAM Data[10]	B		
43	IO_GND	Gnd	IO Ground			
44	DIG_GND	Gnd	Digital Ground			
45	M_D_9	B8	DRAM Data[9]	B		
46	DIG_1V8	Pwr	Digital Power 1.8 V			
47	M_D_8	B8	DRAM Data[8]	B		
48	M_D_7	B8	DRAM Data[7]	B		
49	M_D_6	B8	DRAM Data[6]	B		
50	M_D_5	B8	DRAM Data[5]	B		
51	M_D_4	B8	DRAM Data[4]	B		
52	IO_GND	Gnd	IO Ground			
53	M_D_3	B8	DRAM Data[3]	B		
54	IO_3V3	Pwr	IO Power 3.3 V			
55	M_D_2	B8	DRAM Data[2]	B		
56	M_D_1	B8	DRAM Data[1]	B		
57	VIN_D_0	B4	Primary Video_In Data[0]	I	(1.) Secondary Video_Out Data[0] (2.) GPIO_VIS[0]	O B
58	VIN_D_1	B4	Primary Video_In Data[1]	I	(1.) Secondary Video_Out Data[1] (2.) GPIO_VIS[1]	O B
59	VIN_D_2	B4	Primary Video_In Data[2]	I	(1.) Secondary Video_Out Data[2] (2.) GPIO_VIS[2]	O B
60	VIN_D_3	B4	Primary Video_In Data[3]	I	(1.) Secondary Video_Out Data[3] (2.) GPIO_VIS[3]	O B
61	M_D_0	B8	DRAM Data[0]	B		
62	M_DQM_0	B8	DRAM Byte_En[0]	O		
63	IO_GND	Gnd	IO Ground			
64	M_CKO	O8	DRAM Clock	O	Drc_Clock Eternal Input	I
65	IO_3V3	Pwr	IO Power 3.3 V			
66	M_CKE	B8	DRAM Clock Enable	O		
67	M_AP	B8	DRAM Auto Precharge	O	NVRAM_OE_N	O
68	M_BS1_N	B8	DRAM BankSel[1]	O		
69	M_BS0_N	B8	DRAM BankSel[0]	O		
70	M_RAS_N	B8	DRAM Row Strobe	O		

Table 14. 240-Pin MQFP Pin Assignments (Continued)

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
71	M_CAS_N	B8	DRAM Col. Strobe	O		
72	IO_GND	Gnd	IO Ground			
73	M_WE_N	B8	DRAM Write Enable	O	NVRAM_WE_N	O
74	NV_CE_N	O4	ROM Chip Enable	O		
75	IO_3V3	Pwr	IO Power 3.3 V			
76	M_A_10	B8	DRAM Address[10]	O	NVRAM Address[10]	O
77	M_A_9	B8	DRAM Address[9]	O	NVRAM Address[9]	O
78	M_A_8	B8	DRAM Address[8]	O	NVRAM Address[8]	O
79	M_A_7	B8	DRAM Address[7]	O	NVRAM Address[7]	O
80	M_A_6	B8	DRAM Address[6]	O	NVRAM Address[6]	O
81	DIG_1V8	Pwr	Digital Power 1.8 V			
82	M_A_5	B8	DRAM Address[5]	O	NVRAM Address[5]	O
83	DIG_GND	Gnd	Digital Ground			
84	IO_GND	Gnd	IO Ground			
85	M_A_4	B8	DRAM Address[4]	O	NVRAM Address[4]	O
86	IO_3V3	Pwr	IO Power 3.3 V			
87	M_A_3	B8	DRAM Address[3]	O	NVRAM Address[3]	O
88	M_A_2	B8	DRAM Address[2]	O	NVRAM Address[2]	O
89	M_A_1	B8	DRAM Address[1]	O	NVRAM Address[1]	O
90	M_A_0	B8	DRAM Address[0]	O	NVRAM Address[0]	O
91	NV_D_0	B8	NVRAM Data[0]	B		
92	NV_D_1	B8	NVRAM Data[1]	B		
93	NV_D_2	B8	NVRAM Data[2]	B		
94	NV_D_3	B8	NVRAM Data[3]	B		
95	NV_D_4	B8	NVRAM Data[4]	B		
96	NV_D_5	B8	NVRAM Data[5]	B		
97	IO_GND	Gnd	IO Ground			
98	DIG_GND	Gnd	Digital Ground			
99	NV_D_6	B8	NVRAM Data[6]			
100	DIG_1V8	Pwr	Digital Power 1.8 V			
101	NV_D_7	B8	NVRAM Data[7]			

Table 14. 240-Pin MQFP Pin Assignments (Continued)

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
102	VIN_D_4	B4	Primary Video_In Data[4]	I	(1.) Secondary Video_Out Data[4] (2.) GPIO_VIS[4]	O B
103	VIN_D_5	B4	Primary Video_In Data[5]	I	(1.) Secondary Video_Out Data[5] (2.) GPIO_VIS[5]	O B
104	VIN_D_6	B4	Primary Video_In Data[6]	I	(1.) Secondary Video_Out Data[6] (2.) GPIO_VIS[6]	O B
105	IO_3V3	Pwr	IO Power 3.3 V			
106	VIN_D_7	B4	Primary Video_In Data[7]	I	(1.) Secondary Video_Out Data[7] (2.) GPIO_VIS[7]	O B
107	SCL1	B4SU	I^2C Debug Slave	B		
108	SDA1	B4SU	I^2C Debug Slave	B		
109	SCL2	B4SU	I^2C Master/Simple Slave	B	GPIO_MIS[0]	B
110	SDA2	B4SU	I^2C Master/Simple Slave	B	GPIO_MIS[1]	B
111	TXD_1	B4	UART1 Tx Data	O	GPIO_MIS[6]	B
112	RXD_1	B4	UART1 Rx Data	I	GPIO_MIS[7]	B
113	TXD_2	B4	UART2 Tx Data	O	GPIO_MIS[8]	B
114	RXD_2	B4	UART2 Rx Data	I	GPIO_MIS[9]	B
115	PWM_O	B4	PWM Output	O	GPIO_MIS[10]	B
116	DVD_RDY	B4	Prim. DVD Loader data Request	O	GPIO_DVD[12]	B
117	DVDL_DI	B4	Primary DVD Control Data In	I	(1.) Secondary Video_In Vsync (2.) GPIO_DVD[13] (3.) Secondary Host Slave Read	I B I
118	DVDL_DO	B4	Primary DVD Control Data Out	O	(1.) Secondary Video_In Hsync (2.) GPIO_DVD[14] (3.) Secondary Host Slave Write	I B I
119	DVDL_CK	B4S	Primary DVD Control Clock	O	(1.) Secondary Video_In Clock (2.) GPIO_DVD[15] (3.) Secondary Host Slave Ready	I B O
120	PLL_1V8	Pwr	PLL Power 1.8 V			
121	PLL_GND	Gnd	PLL Ground			
122	IO_GND	Gnd	IO Ground			
123	H_D_0	B4	Host Master Data[0]	B	(1.) Secondary DVD Data[0] (2.) GPIO_HST[0] (3.) Primary Host Slave Data[0] (4.) Primary Video_Out Data[0]	I B B O

Table 14. 240-Pin MQFP Pin Assignments (Continued)

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
124	H_D_1	B4	Host Master Data[1]	B	(1.) Secondary DVD Data[1] (2.) GPIO_HST[1] (3.) Primary Host Slave Data[1] (4.) Primary Video_Out Data[1]	I B B O
125	H_D_2	B4	Host Master Data[2]	B	(1.) Secondary DVD Data[2] (2.) GPIO_HST[2] (3.) Primary Host Slave Data[2] (4.) Primary Video_Out Data[2]	I B B O
126	H_D_3	B4	Host Master Data[3]	B	(1.) Secondary DVD Data[3] (2.) GPIO_HST[3] (3.) Primary Host Slave Data[3] (4.) Primary Video_Out Data[3]	I B B O
127	H_D_4	B4	Host Master Data[4]	B	(1.) Secondary DVD Data[4] (2.) GPIO_HST[4] (3.) Primary Host Slave Data[4] (4.) Primary Video_Out Data[4]	I B B O
128	VIN_VS	B4	Primary Video_In Vsync	I	(1.) Secondary Video_Out Vsync (2.) GPIO_VIS[8] (3.) Host Master Chip Select[4]	O B O
129	VIN_HS	B4	Primary Video_In Hsync	I	(1.) Secondary Video_Out Hsync (2.) GPIO_VIS[9] (3.) Host Master Chip Select[5]	O B O
130	IO_3V3	Pwr	IO Power 3.3 V			
131	VIN_CLK	B4S	Primary Video_In Clock	I	(1.) Secondary Video_Out Clock (2.) GPIO_VIS[10]	O B
132	IO_GND	Gnd	IO Ground			
133	H_D_5	B4	Host Master Data[5]	B	(1.) Secondary DVD Data[5] (2.) GPIO_HST[5] (3.) Primary Host Slave Data[5] (4.) Primary Video_Out Data[5]	I B B O
134	H_D_6	B4	Host Master Data[6]	B	(1.) Secondary DVD Data[6] (2.) GPIO_HST[6] (3.) Primary Host Slave Data[6] (4.) Primary Video_Out Data[6]	I B B O
135	H_D_7	B4	Host Master Data[7]	B	(1.) Secondary DVD Data[7] (2.) GPIO_HST[7] (3.) Primary Host Slave Data[7] (4.) Primary Video_Out Data[7]	I B B O
136	H_D_8	B4	Host Master Data[8]	B	(1.) Secondary DVD Control Clock (2.) GPIO_HST[8]	O B
137	H_D_9	B4	Host Master Data[9]	B	(1.) Secondary DVD Control Ready (2.) GPIO_HST[9]	I B
138	H_D_10	B4	Host Master Data[10]	B	(1.) Secondary DVD Control Data Out (2.) GPIO_HST[10]	O B
139	H_D_11	B4	Host Master Data[11]	B	(1.) Secondary DVD Control Data In (2.) GPIO_HST[11]	I B

Table 14. 240-Pin MQFP Pin Assignments (Continued)

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
140	H_D_12	B4	Host Master Data[12]	B	(1.) Secondary CD C2P0 (2.) GPIO_HST[12] (3.) Secondary DVDS_VLD	I B I
141	H_D_13	B4S	Host Master Data[13]	B	(1.) Secondary CD_BCLK (2.) GPIO_HST[13] (3.) Secondary DVDS_CLK	I B I
142	H_D_14	B4	Host Master Data[14]	B	(1.) Secondary CD_LRLK (2.) GPIO_HST[14] (3.) Secondary DVDS_SOS	I B I
143	H_D_15	B4	Host Master Data[15]	B	(1.) Secondary CD_Data (2.) GPIO_HST[15] (3.) Secondary DVDS_DATA	I B I
144	CD_BCLK	B4S	Primary CD Bit Clock	I	(1.) Primary DVDS_CLK (2.) GPIO_DVD[17] (3.) Secondary Host Slave Address[0]	I B I
145	CD_LRCK	B4	Primary CD L/R Clock	I	(1.) Primary DVDS_SOS (2.) GPIO_DVD[18] (3.) Secondary Host Slave Address[1]	I B I
146	CD_DATA	B4	Primary CD Data	I	(1.) Primary DVDS_DATA (2.) GPIO_DVD[19] (3.) Secondary Host Slave Address[2]	I B I
147	CD_C2P0	B4	Primary CD C2P0	I	(1.) Primary DVDS_VLD (2.) GPIO_DVD[20] (3.) Secondary Host Slave Address[3]	I B B
148	DAC_AGND	Gnd	Analog Ground			
149	DAC_D1V8	Pwr	Digital Power 1.8 V			
150	DAC_DGND	Gnd	Digital Ground			
151	C_OUT	Anlg	C_OUT			
152	DAC_A3V3	Pwr	Analog Power 3.3 V			
153	DAC_AGND	Gnd	Analog Ground			
154	Y_OUT	Anlg	Y_OUT			
155	DAC_A3V3	Pwr	Analog Power 3.3 V			
156	DAC_AGND	Gnd	Analog Ground			
157	CV_OUT	Anlg	CV_OUT			
158	DAC_A3V3	Pwr	Analog Power 3.3 V			
159	DAC_AGND	Gnd	Analog Ground			
160	COMP1	Anlg	Compensation			
161	ISET1	Anlg	Current Set			
162	VREF1	Anlg	Voltage Ref			

Table 14. 240-Pin MQFP Pin Assignments (Continued)

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
163	DAC_AGND	Gnd	Analog Ground			
164	DAC_A3V3	Pwr	Analog Power 3.3 V			
165	DAC_AGND	Gnd	Analog Ground			
166	DAC_A3V3	Pwr	Analog Power 3.3 V			
167	DAC_A3V3	Pwr	Analog Power 3.3 V			
168	DVDL_RDY	B4	Primary DVD Control Ready	I	(1.)GPIO_DVD[16] (2.) Secondary Host Slave Chip_Select	B I
169	DIG_1V8	Pwr	Digital Power 1.8 V			
170	H_A_0	B4	Host Master Address[0]	O	(1.) GPIO_HST[16] (2.) Primary Host Slave Address[0]	B I
171	DIG_GND	Gnd	Digital Ground			
172	H_A_1	B4	Host Master Address[1]	O	(1.) GPIO_HST[17] (2.) Primary Host Slave Address[1]	B I
173	H_A_2	B4	Host Master Address[2]	O	(1.) GPIO_HST[18] (2.) Primary Host Slave Address[2]	B I
174	DVD_D_0	B4	Primary DVD Data[0]	I	(1.) Secondary Video_In Data[0] (2.) GPIO_DVD[0] (3.) Secondary Host Slave Data[0]	I B B
175	DVD_D_1	B4	Primary DVD Data[1]	I	(1.) Secondary Video_In Data[1] (2.) GPIO_DVD[1] (3.) Secondary Host Slave Data[1]	I B B
176	H_A_3	B4	Host Master Address[3]	O	(1.) GPIO_HST[19] (2.) Primary Host Slave Address[3]	B I
177	H_ALE	B4	Host Master Address Latch	O	GPIO_HST[20]	B
178	DVD_D_2	B4	Primary DVD Data[2]	I	(1.) Secondary Video_In Data[2] (2.) GPIO_DVD[2] (3.) Secondary Host Slave Data[2]	I B B
179	DVD_D_3	B4	Primary DVD Data[3]	I	(1.) Secondary Video_In Data[3] (2.) GPIO_DVD[3] (3.) Secondary Host Slave Data[3]	I B B
180	PLL_1V8	Pwr	PLL Power 1.8 V			
181	PLL_GND	Gnd	PLL Ground			
182	DVD_D_4	B4	Primary DVD Data[4]	I	(1.) Secondary Video_In Data[4] (2.) GPIO_DVD[4] (3.) Secondary Host Slave Data[4]	I B B
183	DVD_D_5	B4	Primary DVD Data[5]	I	(1.) Secondary Video_In Data[5] (2.) GPIO_DVD[5] (3.) Secondary Host Slave Data[5]	I B B

Table 14. 240-Pin MQFP Pin Assignments (Continued)

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
184	DVD_D_6	B4	Primary DVD Data[6]	I	(1.) Secondary Video_In Data[6] (2.) GPIO_DVD[6] (3.) Secondary Host Slave Data[6]	I B B
185	DVD_D_7	B4	Primary DVD Data[7]	I	(1.) Secondary Video_In Data[7] (2.) GPIO_DVD[7] (3.) Secondary Host Slave Data[7]	I B B
186	H_CS_0	B4	Host Master Chip_Select[0]	O	(1.) Secondary DVD Start Sector (2.) GPIO_HST[21] (3.) Primary Host Slave Chip Select	I B I
187	H_CS_1	B4	Host Master Chip_Select[1]	O	(1) Secondary DVD Error (2.) GPIO_HST[22]	I B
188	IO_3V3	Pwr	IO Power 3.3 V			
189	H_CS_2	B4	Host Master Chip_Select[2]	O	GPIO_HST[23]	B
190	IO_GND	Gnd	IO Ground			
191	H_CS_3	B4	Host Master Chip_Select[3]	O	GPIO_HST[24]	B
192	H_RD	B4	Host Master Read	O	(1.) Secondary DVD Ready (2.) GPIO_HST[25] (3.) Primary Host Slave Read	O B I
193	H_WR	B4	Host Master Write	O	(1.) Secondary DVD Data Enable (2.) GPIO_HST[26] (3.) Primary Host Slave Write	I B I
194	H_RDY	B4S	Host Master Ready	I	(1.) Secondary DVD Data Strobe (2.) GPIO_HST[27] (3.) Primary Host Slave Ready	I B O
195	SPI_CLK	B4S	SPI Clock	B	GPIO_MIS[2]	B
196	SPI_DO	B4	SPI Data Out/InOut	B	GPIO_MIS[3]	B
197	SPI_DI	B4	SPI Data In	I	GPIO_MIS[4]	B
198	SPI_RDY	B4	SPI Ready / Chip Select	B	GPIO_MIS[5]	O
199	AUDI_D	B4	PCM Input Data	I	GPIO_MIS[15]	B
200	AUDI_LR	B4	PCM LR Clock	I	GPIO_MIS[16]	B
201	AUDI_BCK	B4S	PCM Input Clock	I	(1.) Aud_Pll_Aux_FIN[0] (2.) GPIO_MIS[17] (3.) AudioOut_Mute	I B O
202	DAC_AGND	Gnd	Analog Ground			
203	DAC_D1V8	Pwr	Digital Power 1.8 V			
204	DAC_DGND	Gnd	Digital Ground			
205	UB_OUT	Anlg	UB_OUT_1			
206	DAC_A3V3	Pwr	Analog Power 3.3 V			

Table 14. 240-Pin MQFP Pin Assignments (Continued)

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
207	DAC_AGND	Gnd	Analog Ground			
208	YG_OUT	Anlg	YG_OUT_1			
209	DAC_A3V3	Pwr	Analog Power 3.3 V			
210	DAC_AGND	Gnd	Analog Ground			
211	VR_OUT	Anlg	VR_OUT_1			
212	DAC_A3V3	Pwr	Analog Power 3.3 V			
213	DAC_AGND	Gnd	Analog Ground			
214	COMP2	Anlg	Compensation			
215	ISET2	Anlg	Current Set			
216	VREF2	Anlg	Voltage Ref			
217	DAC_AGND	Gnd	Analog Ground			
218	DAC_A3V3	Pwr	Analog Power 3.3 V			
219	DAC_AGND	Gnd	Analog Ground			
220	DAC_A3V3	Pwr	Analog Power 3.3 V			
221	DAC_A3V3	Pwr	Analog Power 3.3 V			
222	AUDO_LR	B4	PCM LR Clock	O	(1.) Clock_Monitor_CPU (2.) Host ParSlave_Set	O I
223	DIG_1V8	Pwr	Digital Power 1.8 V			
224	AUDO_BCK	B4	PCMO BCLK	O	(1.) Clock_Monitor_DRC (2.) GPIO_MIS[11]	O B
225	DIG_GND	Gnd	Digital Ground			
226	AUD_XCLK	B4S	PCM MCLK Output	O	PCM MCLK External Input	I
227	AUDO_D_1	B4	PCM Data Out[1]	O	(1.) System Clock External Input (2.) GPIO_MIS[12]	I B
228	AUDO_D_2	B4	PCM Data Out[2]	O	(1.) CPU clock External Input (2.) GPIO_MIS[13]	I B
229	AUDO_D_3	B4	PCM Data Out[3]	O	(1.) Aud_PLL_AUX_FIN[1] (2.) GPIO_MIS[14]	I B
230	IO_3V3	Pwr	IO Power 3.3 V			
231	XTLCLK_I	OSC	27 MHz Clock In	I		
232	XTLCLK_O	OSC	27 MHz Clock Out	O		
233	IO_GND	Gnd	IO Ground			
234	AUDO_D_0	B4	PCM Data Out[0]	O	(1.) Main_Clock_Monitor (2.) HostSlave_Par_I2C_Sel	O I

Table 14. 240-Pin MQFP Pin Assignments (Continued)

Pin #	Pin Name	Type	Primary Function	Dir	Secondary Function(s)	Dir
235	SPDIF_O	B4	SPDIF	O	Process_Monitor_Out	O
236	DVD_STB	B4S	Primary DVD Data Strobe	I	(1.) Host Master Address[4] (2.) GPIO_DVD[8]	O B
237	DVD_ENA	B4	Primary DVD Data Enable	I	(1.) Host Master Address[5] (2.) GPIO_DVD[9]	O B
238	DVD_SOS	B4	Primary DVD Start Sector	I	(1.) Host Master Address[6] (2.) GPIO_DVD[10]	O B
239	DVD_ERR	B4	Primary DVD Error	I	(1.) Host Master Address[7] (2.) GPIO_DVD[11]	O B
240	PLL_GND	Gnd	PLL Ground			

Table 14. 240-Pin MQFP Pin Assignments (Continued)

8. INTERFACE DESCRIPTIONS

8.1 SDRAM Interface Pins

These pins are used to interface the CS98200 with some external SDRAM. The CS98200 can interface with SDRAM of various sizes. Only 32-bit data width is supported. Follow the instructions in Table 15 on how to interface with any particular configuration of SDRAM.

Pin	Signal Name	Type	Description
11,12,13,15,16, 17,18,20,21,23, 26,27,28,29,30, 32,61, 56, 55, 53, 51, 50, 49, 48, 47, 45, 42, 40, 39, 38, 37, 36,	M_D[31:0]	B	Memory Data Bus. CS98200 uses all 32 bits.
90, 89, 88, 87, 85, 82, 80, 79, 78, 77, 76	M_A[10:0]	O	Memory Address Bus. Connect in order starting with M_A[0] to all RAM address pins not already connected to M_BS[1:0]_N or M_AP.
64	M_CKO	O	Memory Clock
66	M_CKE	O	Memory Clock Enable
69	M_BS0_N	O	Bank Selection. Always connect to RAM BS or BS0 pin.
68	M_BS1_N	O	Bank Selection. Always connect to RAM BS or BS0 pin.
67	M_AP	O	Memory Auto Pre-charge. Always connect to RAM AP pin.
70	M_RAS_N	O	Memory Row Address Strobe
71	M_CAS_N	O	Memory Column Address Strobe
73	M_WE_N	O	Memory Write Enable
62, 35, 33, 10	M_DQM[3:0]	O	IO Mask of Data Bus M_DQM[3] -> M_D[31:24]

Table 15. SDRAM Interface Pins

8.2 ROM/NVRAM Interface Pins

This is the interface to the non-volatile memory that contains the firmware. See Table 16. It could be either ROM, NVRAM – FLASH, or EEPROM, or any combination of these types of memory. This interface can also connect to SRAM that would emulate a ROM on a development system. The bus width is 8 bits.

Pin	Signal Name	Type	Description
91,92,93,94,95, 96,99,101	NV_D[7:0]	B	Memory Data Bus.
90, 89, 88, 87, 85, 82, 80, 79, 78, 77, 76	M_A[10:0]	O	Memory Address Bus[10:0]
32, 30, 29, 28, 27, 26, 23, 21, 20, 18, 17, 16	M_D[31:16]	O	Memory Address Bus[23:11]
67	M_AP	O	Output Enable
73	M_WE_N	O	Write Enable.

Table 16. ROM/NVRAM Interfa c e

74	NV_CE_N	O	ROM/NVRAM Chip Enable.

Table 16. ROM/NVRAM Interface (Continued)

8.3 Video Output Interface Pins

This is the interface to a video encoder chip that will send the CS98200 video signals to a TV. See Table 17. This interface uses the same pins of the Video Input Interface, so you are not able to use Video Input (primary) and Video Output (Secondary) at the same time. .

Pin	Signal Name	Type	Description
131s	VOUT_CLK	O	27 Mhz Clock Output.
129s	VOUT_HS	O	Horizontal Sync. Output when the CS98200 is the video master, input when the video encoder is master.
128s	VOUT_VS	O	Vertical Sync. Output when the CS98200 is the video master, input when the video encoder is master.
57s, 58s, 59s, 60s, 102s, 103s, 104s, 106s	VOUT_D[7:0]	O	Video Data Output[7:0] in Cb, Y, Cr, Y format.

Table 17. Video Output Interface

8.4 Video Input Interface Pins

See Table 18.

Pin	Signal Name	Type	Description
131	VIN_CLK	I	Video Input Clock.
128	VIN_VS	I	Video Input Vertical Sync.
129	VIN_HS	I	Video Input Horizontal Sync.
57, 58, 59, 60, 102, 103, 104, 106	VIN_D [7:0]	I	Video Data Input[7:0] in Cb, Y, Cr, Y format.

Table 18. Video Input Interface

8.5 Audio PCM Interface Pins

This is the audio PCM interface that connects to an audio CODEC. See Table 19. The sample rate and the size of the samples are programmable for both input and output direction.

Pin	Signal Name	Type	Description
226	AUD_XCLK	B	Audio 256x/384x Clock input or output to Serial DAC. When output, is generated from CS98200 internal PLL.
224	AUDO_BCK	O	Audio Bit Clock output to serial DAC.
222	AUDO_LR	O	Audio Out Left/Right Clock to serial DAC.
234	AUDO_D_0	O	Audio Serial Data Out[0].
227	AUDO_D_1	O	Audio Serial Data Out[1].
228	AUDO_D_2	O	Audio Serial Data Out[2].
229	AUDO_D_3	O	Audio Serial Data Out[3].
235	SPDIF_O	O	S/PDIF Output
201	AUDI_BCK	I	Audio Input Bit Clock. The CS98200 can be programmed to use the Audio Output function's internally generated bit clock, in which case this pin is not required.
200	AUDI_LR	I	Audio Input Left/Right Clock. The CS98200 can be programmed to use the Audio Output function's internally generated LR clock, in which case this pin is not required.
199	AUDI_D	I	Audio Input Data from Serial ADC.

Table 19. PCM Audio Interfa c e

8.6 Host Master/ATAPI Interface

Pin	Signal Name	Type	Description
186, 187, 189, 191	H_CS[3:0]	O	Host Chip Select[3:0]. The host master can be programmed to use a different protocol for each of the 4 chip selects
177	H_ALE	O	Host address latch enable. Used for modes which multiplex upper address information onto the data lines
192	H_RD	O	Host Read Request.
193	H_WR	O	Host Write Request.
194	H_RDY	I	Host Ready. Connect to pull-up or pull-down if host is not used.
170, 172, 173, 176	H_A[3:0]	O	Host Address[3:0].
123, 124, 125, 126, 127, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143	H_D[15:0]	B	Host Data Bus[15:0]. These pins can also output Host Address during the address phase for multiplexed address/data mode. Tie together to pull-up or pull-down if host is not used.

Table 20. Host Master/ATAPI Interface

8.7 DVD Loader Interface

This interface connects to standard DVD loaders, and consists of three parts: Control, DVD Data and CD Data. (See Table 21.) This interface shares CS98200 pins with the Host Master / ATAPI interface. (See Table 20 on page 52.) The definition of the pins is set via register programming, and the two modes are mutually exclusive.

Pin	Signal Name	Type	Description
174, 175, 178, 179, 182, 183, 184, 185	DVD_D[7:0]	I	Primary DVD Data
168	DVDL_RDY	I	Primary DVD Control Ready
236	DVD_STB	I	Primary DVD Data Strobe
237	DVD_ENA	I	Primary DVD Data Enable
238	DVD_SOS	I	Primary DVD Start Sector
239	DVD_ERR	I	Primary DVD Error
116	DVD_RDY	O	Primary DVD Data Request
117	DVDL_DI	I	Primary DVD Control Data In
118	DVDL_DO	O	Primary DVD Control Data Out
119	DVDL_CK	O	Primary DVD Control Clock
144	CD_BCLK	I	Primary CD Bit Clock
145	CD_LRCK	I	Primary CD L/R Clock
146	CD_DATA	I	Primary CD Data
147	CD_C2PO	I	Primary CD C2P0

Table 21. DVD I/O Channel Interface

8.8 DVD Serial Data Interface

This interface connects to the data port of low cost DVD loaders using a 4-wire serial interface. In this case, control for the loader will typically be done using the 2-wire serial interface master. The ATAPI/IO channel pins are then free to be used for a second DVD loader, a general purpose ATAPI, or as GPIOs.

Pin	Signal Name	Type	Description
144s /141s	DVDS_CLK	I	DVD Clock Input
146s/143s	DVDS_DATA	I	DVD serial data input (data can be input MSB or LSB first)
147s/140s	DVDS_VLD	I	DVD valid (a bit of data is clocked in when this pin is high)
145s/142s	DVDS_SOS	I	DVD start of sector input

8.9 SPI Interface

The SPI Interface supports industry standard 3-wire protocols. (See Table 22) In master mode, this interface can control a front panel or a small non-volatile memory. In slave mode, it can operate under control of an external processor, for example, in a combination unit.

Pin	Signal Name	Type	Description
195	SPI_CLK	B	SPI Clock
196	SPI_DO	B	SPI Data In/Out
197	SPI_DI	I	SPI Data In
198	SPI_RDY	B	SPI Ready / Chip Select

Table 22. SPI Interface

8.10 General Purpose Input/Output (GPIO)

The CS98200 provides enough GPIO pins, each with individual output High-Z-state controls. High-Z-state means that the output driver is turned off or placed in the high-impedance state. Table 23 describes the General Purpose I/O Interface. Additional pins may also be re-defined as GPIOs.

Pin	Signal Name	Type	Description
174s, 175s, 178s, 179s, 182s, 183s, 184s, 185s, 236s, 237s, 238s, 239s, 116s, 117s, 118s, 119s, 168s, 144s, 145s, 146s, 147s,	GPIO_DVD[20:0]	B	21 General purpose I/Os
123s, 124s, 125s, 126s, 127s, 133s, 134s, 135s, 136s, 137s, 138s, 139s, 140s, 141s, 142s, 143s, 170s, 172s, 173s, 176s, 177s, 186s, 187s, 189s, 191s, 192s, 193s, 194s	GPIO_HST[0:27]	B	28 General purpose I/Os
57s, 58s, 59s, 60s, 102s, 103s, 104s, 106s, 128s, 129s, 131s,	GPIO_VIS[0:10]	B	11 General purpose I/Os
109s, 110s, 125s, 126s, 127s, 198s, 111s, 112s, 113s, 114s, 115s, 224s, 227s, 228s, 229s, 199s, 200s, 201s, 5s, 6s, 7s, 8s	GPIO_MIS[0:21]	B	22 General purpose I/Os

Table 23. General Purpose I/O Interface

8.11 UART Interface Pins

The CS98200 has two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data.

Pin	Signal Name	Type	Description
111	TXD_1	O	UART1 Tx Data
112	RXD_1	I	UART1 Rx Data
113	TXD_2	O	UART2 Tx Data
114	RXD_2	I	UART2 Rx Data

Table 24. UART Interface Pins

8.12 I^2C Interface

The I^2C pins are used for both master and slave mode.

Pin	Signal Name	Type	Description
107	SCL1	B	I^2C Debug Slave
108	SDA1	B	I^2C Debug Slave
109	SCL2	B	I^2C Master/Simple Slave
110	SDA2	B	I^2C Master/Simple Slave

Table 25. I^2C Interface Pins

8.13 Miscellaneous Interface Pins

These pins are used for used for basic functions such as clock and reset input. See Table 26.

Pin	Signal Name	Type	Description
4	IR_IN	I	Infrared Input, from IR receiver.
231	XTLCLK_I	I	27 MHz Clock Input.
232	XTLCLK_O	O	27 MHz Clock Output.
2	RST_N	I	Reset Input, active low.
3	TEST	I	Manufacturing test pin, should always connect to ground.

Table 26. Miscellaneous Interface Pins

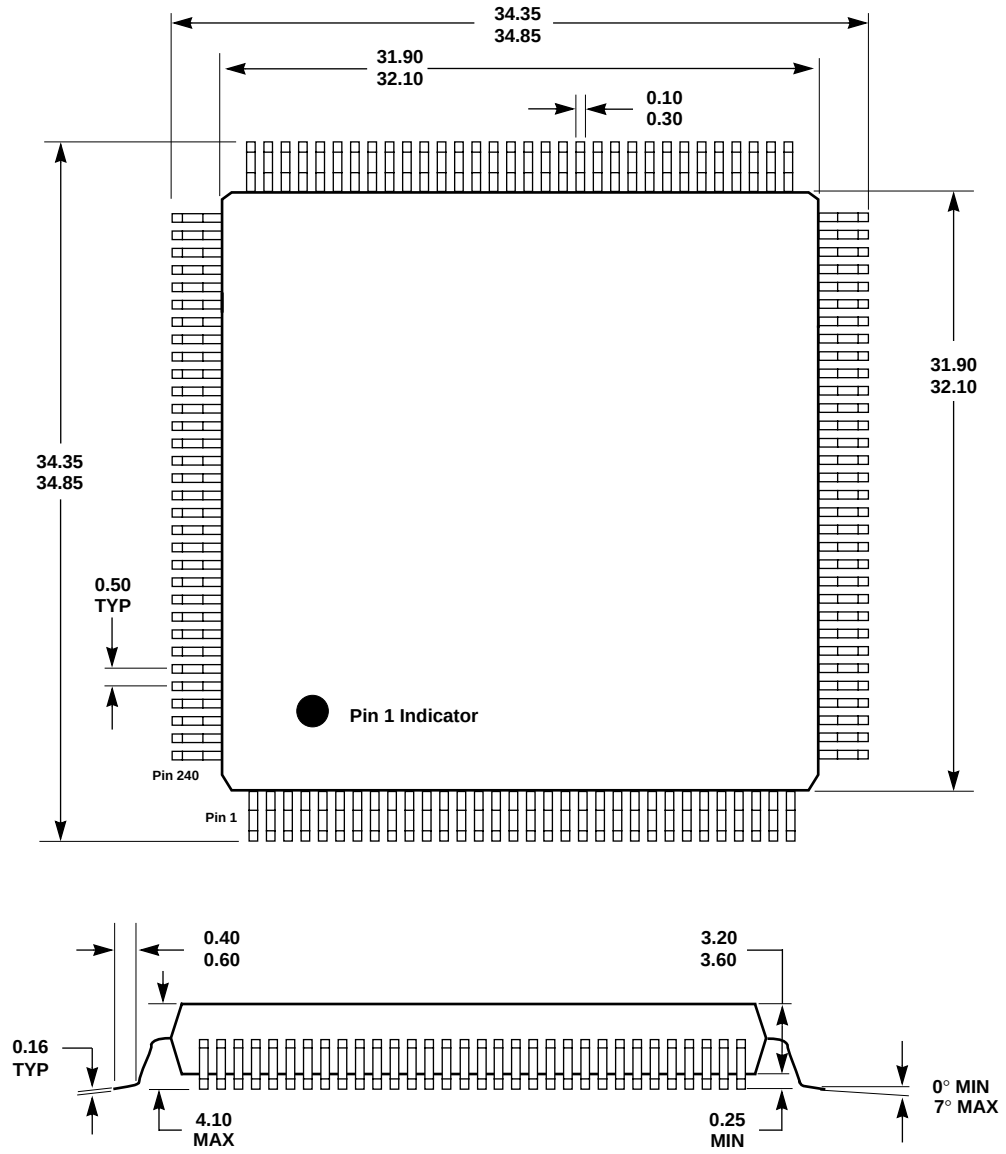
8.14 Power and Ground

The CS98200 requires 4 different types of power supplies – PLLs, digital, analog, and IO pins -. The PLLs and digital power use 1.8 V power supply. The IO pins and digital power use 3.3 V power supply, and are 5 V input tolerant. (See Table 27.)

Pin	Signal Name	Type	Description
1, 120, 180,	PLL_1V8		2.5 V for internal PLLs
149, 203	DAC_D1V8		Digital Power 1.8 V
152, 155, 158, 164, 166, 167, 206, 209, 212, 218, 220, 221	DAC_A3V3		Analog Power 3.3 V
9, 19, 31, 41, 54, 65, 75,86, 105, 130, 188, 230	IO_3V3		3.3 V for I/Os
22,46, 81, 100, 169, 223	DIG_1V8		Digital Power
150, 204	DAC_DGND		Digital Ground
148,153, 156, 159, 163, 165, 202, 207, 210, 213, 217, 219	DAC_AGND		Analog Ground
121, 181, 240	PLL_GND		Ground for internal PLLs
14, 25, 34, 43, 52, 63, 72, 84, 97, 122, 132, 190, 233	IO_GND		Ground for I/Os
24, 44, 83, 98, 171, 225	DIG_GND		Digital Ground

Table 27. Power and Ground

9. 240-PIN MQFP PACKAGE SPECIFICATIONS



NOTES:

1) Dimensions are in millimeters, and controlling dimension is millimeter.
2) Package body dimensions do not include mold protrusion, which is 0.25 mm (0.010 in).
3) Pin 1 identiÞcation may be either ink dot or dimple.
4) Package top dimensions can be smaller than bottom dimensions by 0.20 mm (0.008 in).
5) The Ôlead width with platingÕ dimension does not include a total allowable dambar protrusion of 0.08 mm (at maximum material condition).
6) Ejector pin marks in molding are present on every package.
7) Drawing above does not reßect exact package pin count.

Figure 25. 240-Pin MQFP Package Drawing

10. CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

10.1 Acronyms and Abbreviations

Table 28 lists abbreviations and acronyms used in this data sheet.

Acronym/ Abbreviation	Definition
A/D	analog-to-digital
ADC	analog-to-digital converter
CODEC	coder / decoder
D/A	digital-to-analog
DMA	direct-memory access
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in / first out
FIQ	fast interrupt request
GPIO	general purpose I/O
ICT	in circuit test
IR	infrared
IRQ	standard interrupt request
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	liquid crystal display
LED	light-emitting diode
MQFP	Medium profile quad flat pack
LSB	least significant bit
MIPS	millions of instructions per second
MMU	memory management unit
MSB	most significant bit
PBGA	plastic ball grid array
PCB	printed circuit board
PDA	personal digital assistant
PLL	phase locked loop
p/u	pull-up resistor
RISC	reduced instruction set computer
RTC	Real-Time Clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random access memory
SSI	synchronous serial interface

Table 28. Acronyms and Abbreviatio ns

Acronym/ Abbreviation	Definition
TAP	test access port
TLB	translation lookaside buffer
UART	universal asynchronous receiver

Table 28. Acronyms and Abbreviations (Continued)

10.2 Units of Measurement

Symbol	Unit of Measure
°C	degree Celsius
fs	sample frequency
Hz	hertz (cycle per second)
kbps	kilobits per second
KB	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilo Ohm
Mbps	megabits (1,048,576 bits) per second
MB	megabyte (1,048,576 bytes)
MBps	megabytes per second
MHz	megahertz (1,000 kilohertz)
µA	microampere
µF	microfarad
µW	microwatt
µs	microsecond (1,000 nanoseconds)
mA	milliampere
mW	milliwatt
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt

Table 29. Units of Measurement

10.3 General Conventions

Hexadecimal numbers are presented with all letters in uppercase and a lowercase “h” appended or with a 0x at the beginning. For example, 0x14 and 03CAh are hexadecimal numbers. Binary numbers are enclosed in single quotation marks when in text (for example, ‘11’ designates a binary number). Numbers not indicated by an “h”, 0x or quotation marks are decimal.

Registers are referred to by acronym, with bits listed in brackets separated by a colon (:) (for example, CODR[7:0]), and are described in the *CS98200 Registers* document. The use of “TBD” indicates values that are “to be determined,” “n/a” designates “not available,” and “n/c” indicates a pin that is a “no connect.”

10.4 Pin Description Conventions

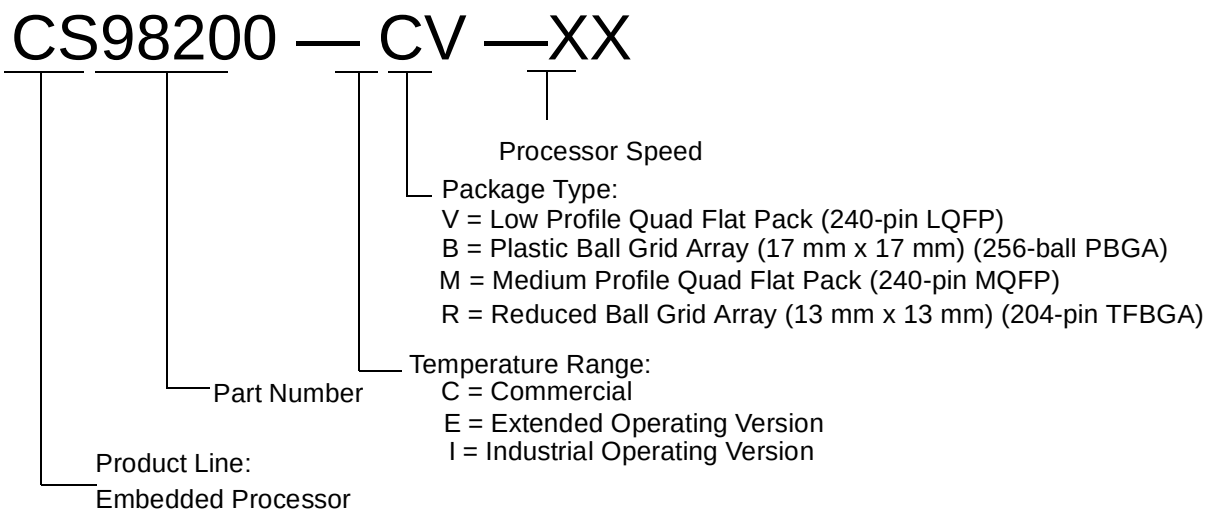
Abbreviations used for signal directions are listed in Table 30. Pin numbers that have an "s" after the pin number indicate that the pin is using a secondary function for that pin.

Abbreviation	Direction
I	Input
O	Output
B	Input or Output

Table 30. Pin Description Conventions

11. ORDERING INFORMATION LEGEND

Here is the legend for understanding the ordering information listed above.



Note: Go to the Cirrus Logic Internet site at http://cirrus.com/corporate/contacts to find contact information for your local sales representative.