HM62V8128 Series — Product Preview

131072-Word × 8-Bit High Speed CMOS Static RAM

Description

The Hitachi HM62V8128 is a CMOS static RAM organized 128 kword × 8 bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

- High Speed
  Fast access time: 120/150 ns (max)
- Low power
  Active: 18 mW (typ)
  Standby: 3 μW (typ) (L-/L-L/L-SL version)
- Single 3 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- All inputs and outputs CMOS compatible.
- Capability of battery back up operation (L-/L-L/L-SL version)
  2 chip selection for battery back up

Ordering Information

Type No.	Access time	Package
HM62V8128P-12	120 ns	600-mil 32-pin plastic DIP (DP-32)
HM62V8128P-15	150 ns	
HM62V8128LP-12	120 ns	
HM62V8128LP-15	150 ns	
HM62V8128LP-12SL	120 ns	
HM62V8128LP-15SL	150 ns	
HM62V8128FP-12	120 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62V8128FP-15	150 ns	
HM62V8128LFP-12	120 ns	
HM62V8128LFP-15	150 ns	
HM62V8128LFP-12SL	120 ns	
HM62V8128LFP-15SL	150 ns	
HM62V8128T-12	120 ns	8mm × 20mm 32-pin TSOP (normal type) (TFP-32D)
HM62V8128T-15	150 ns	
HM62V8128LT-12	120 ns	
HM62V8128LT-15	150 ns	
HM62V8128LT-12L	120 ns	
HM62V8128LT-15L	150 ns	

Note: Product Preview: This document contains information on a product under development. Hitachi reserves the right to change or discontinue the product without notice.

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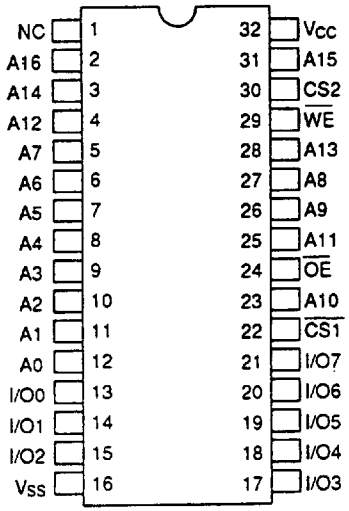
Ordering Information (cont)

Type No.	Access time	Package
HM62V8128R–12	120ns	
HM62V8128R–15	150ns	
HM62V8128LR–12	120 ns	8mm X 20mm 32-pin TSOP (reverse type) (TFP-32DR)
HM62V8128LR–15	150 ns	
HM62V8128LR–12L	120 ns	
HM62V8128LR–15L	150 ns	

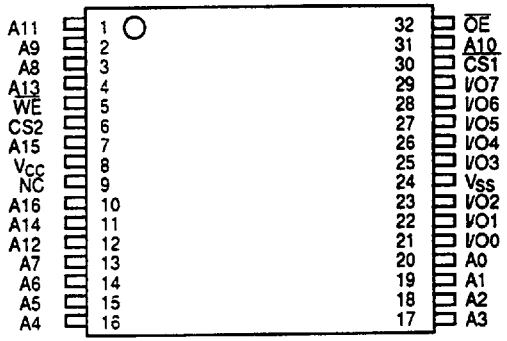
Pin Arrangement

HM62V8128P/FP Series



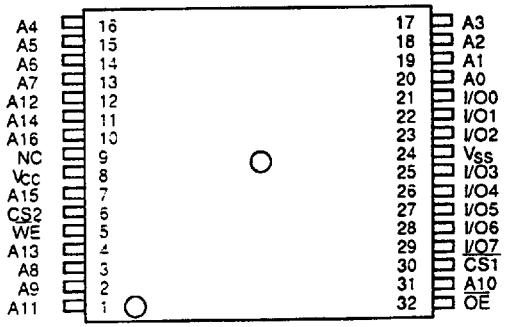
(Top View)

HM62V8128T Series



(Top View)

HM62V8128R Series

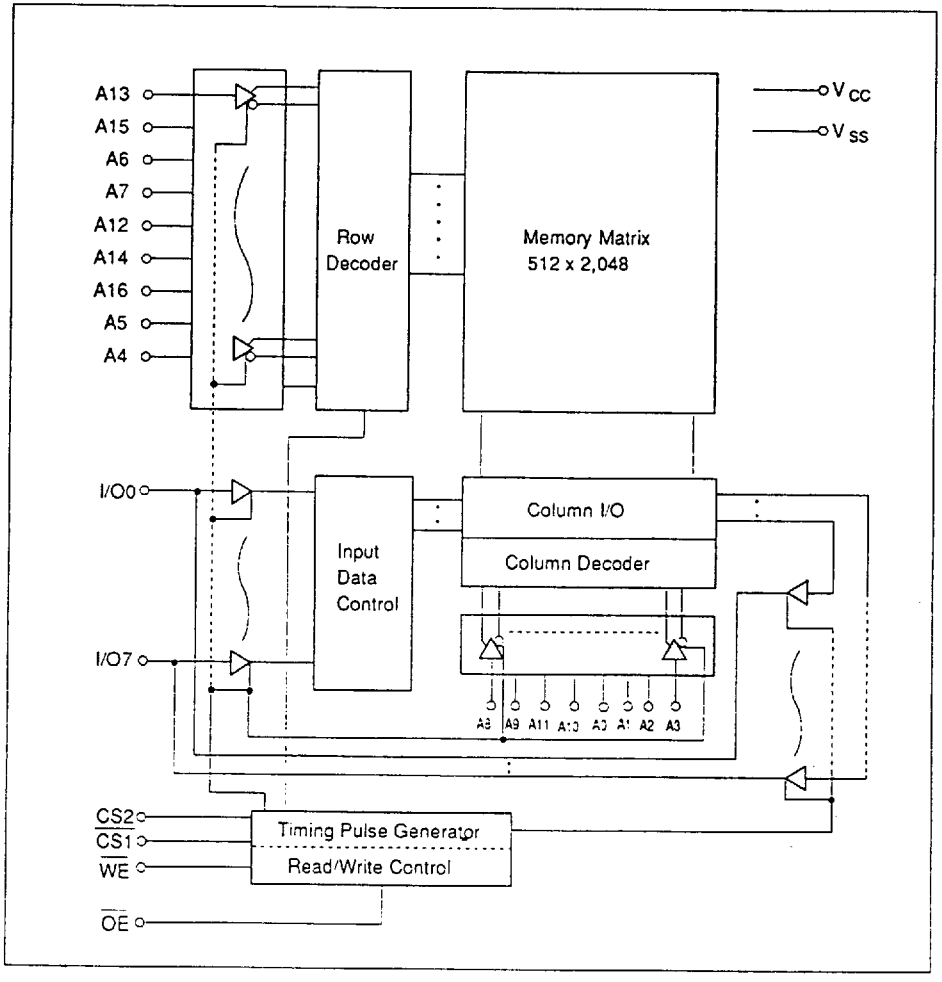


(Top View)

Pin Description

Pin name	Function	Pin name	Function
A0 – A16	Address	$\overline{WE}$	Write enable
I/O0 – I/O7	Input/output	$\overline{OE}$	Output enable
$\overline{CS1}$	Chip select 1	NC	No connection
CS2	Chip select 2	V_{CC}	Power supply
		V_{SS}	Ground

Block Diagram



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Function Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
X	L	X	X	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to + 5.5	V
Voltave on any pin relative to V_{SS}	V_T	−0.5*1 to V_{CC}+0.3	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	−55 to + 125	°C
Storage tremperature under bias	Tbias	−10 to 85	°C

Notes: 1. −1.2 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.3	—	V_{CC}+0.3	V
	V_{IL}	−0.3 *1	—	0.4	V

Note: 1. −1.2 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current: DC	I_{CC}	—	5	10	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
Operating power supply current	I_{CC1}	—	15	20	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA	
	I_{CC2}	—	6	10	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} - 0.2 V, V_{IH} ≥ V_{CC} - 0.2 V, V_{IL} ≤ 0.2 V	
Standby power supply current: DC	I_{SB}	—	0.5	2	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or CS2 = V_{IL}	
Standby power supply current (1): DC	I_{SB1}	—	0.01	1	mA	0 V ≤ Vin ≤ V_{CC}, $\overline{CS1}$ ≥ V_{CC} - 0.2 V, CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V	
		—	1	60	µA		L-version
		—	1	40	µA		L-L version
		—	1	20	µA		L-SL version
Output voltage	V_{OL}	—	—	0.1	V	I_{OL} = 100 µA	
	V_{OH}	2.6	—	—	V	I_{OH} = −100 µA	

Note: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

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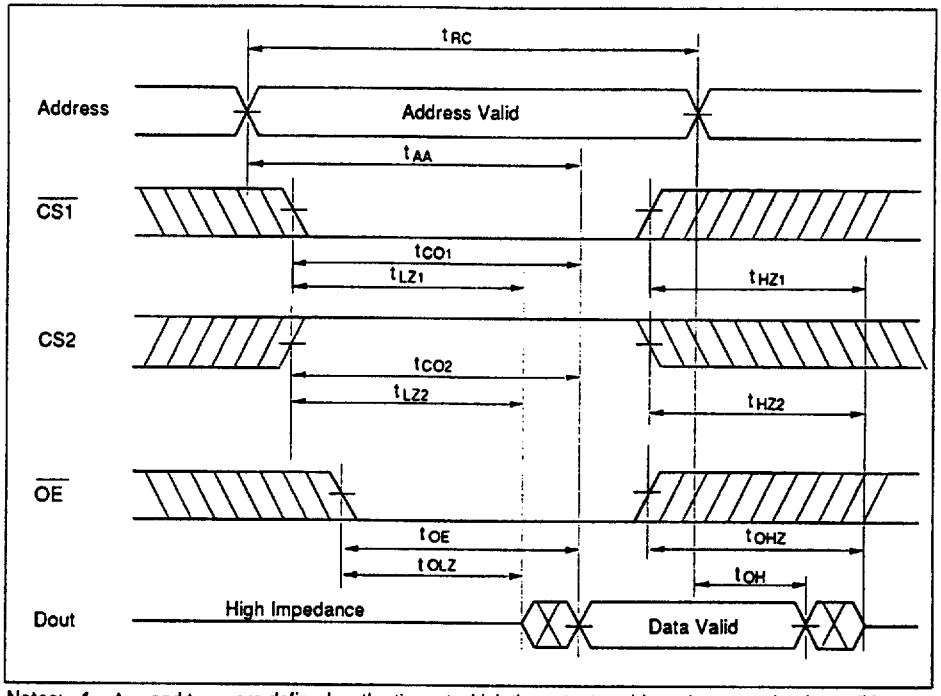
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3 V ± 10%, unless otherwise noted.)

Test Conditions
- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load:
  HM62V8128-12 1 TTL Gate and C_L (50 pF)
  HM62V8128-15 1 TTL Gate and C_L (100 pF)
  (Including scope & jig)

Read Cycle

		HM62V8128–12		HM62V8128–15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	120	—	150	—	ns	
Address access time	t_{AA}	—	120	—	150	ns	
Chip selection to output valid	t_{CO1}	—	120	—	150	ns	
	t_{CO2}	—	120	—	150	ns	
Output enable to output valid	t_{OE}	—	90	—	100	ns	
Chip selection to output in low-Z	t_{LZ1}	15	—	20	—	ns	1, 2, 3
	t_{LZ2}	15	—	20	—	ns	1, 2, 3
Output enable to output in low-Z	t_{OLZ}	10	—	10	—	ns	1, 2, 3
Chip deselection to output in high-Z	t_{HZ1}	0	50	0	60	ns	1, 2, 3
	t_{HZ2}	0	50	0	60	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	50	0	60	ns	1, 2, 3
Output hold from address change	t_{OH}	15	—	20	—	ns	1, 2, 3

Read Timing Waveform *4



Notes:
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. This parameter is sampled and not 100% tested.
4. $\overline{WE}$ is high for read cycle.

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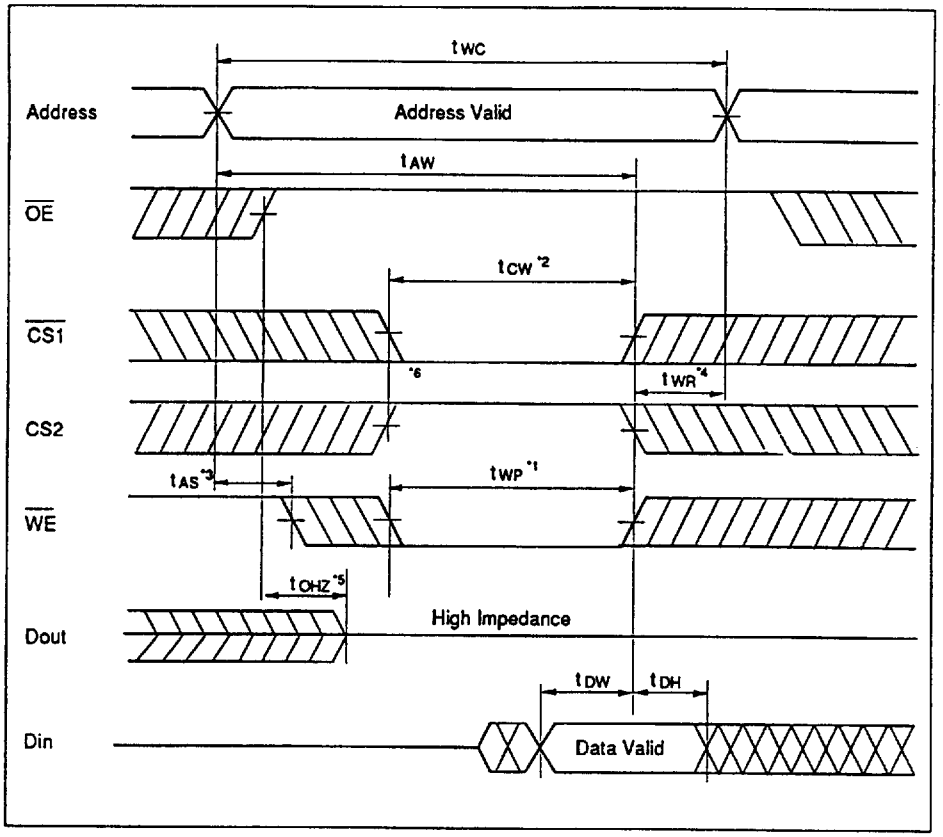
Write Cycle

Parameter	Symbol	HM62V8128-12 Min	HM62V8128-12 Max	HM62V8128-15 Min	HM62V8128-15 Max	Unit	Notes
Write cycle time	t_{WC}	120	—	150	—	ns	
Chip selection to end of write	t_{CW}	110	—	140	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	
Address valid to end of write	t_{AW}	110	—	140	—	ns	
Write pulse width	t_{WP}	100	—	130	—	ns	
Write recovery time	t_{WR}	0	—	0	—	ns	
		0	—	0	—	ns	11
Write to output in high-Z	t_{WHZ}	0	50	0	60	ns	10
Data to write time overlap	t_{DW}	60	—	80	—	ns	
Write hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	15	—	20	—	ns	10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



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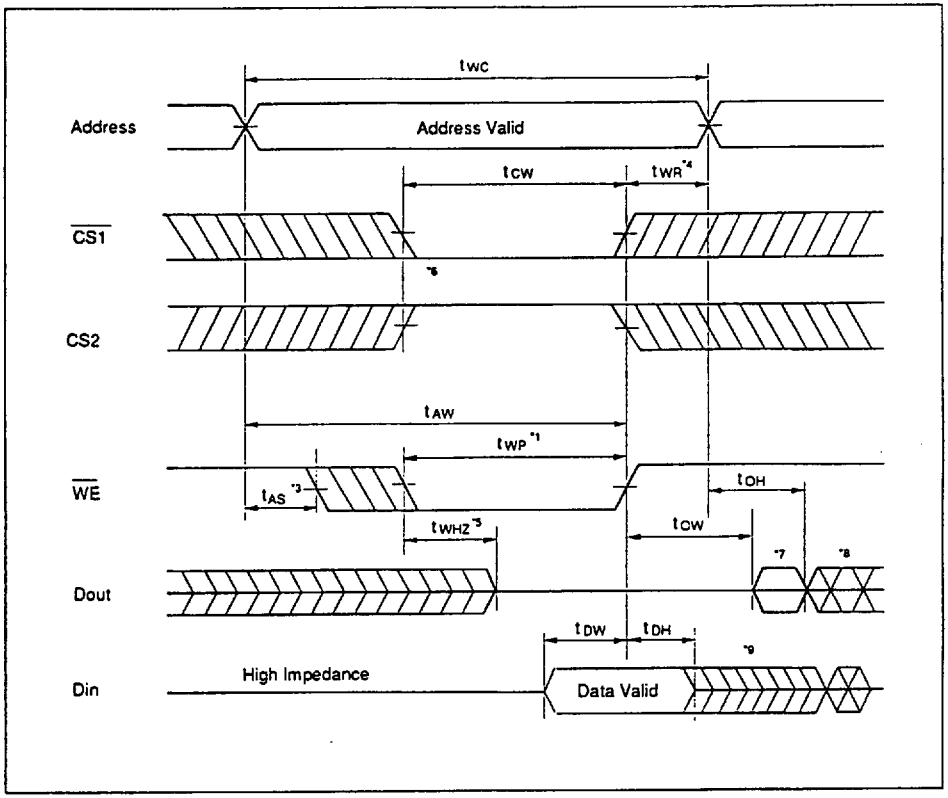
Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



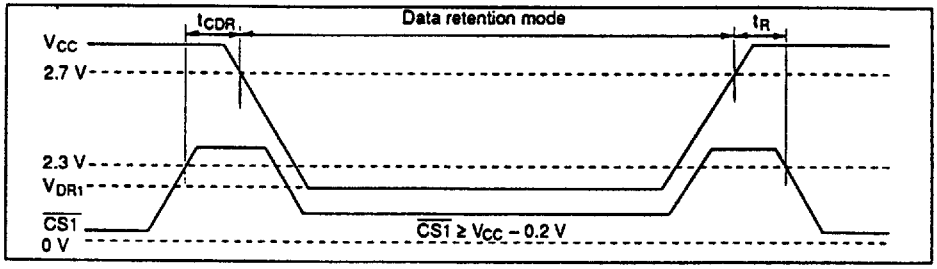
Notes:
1. A write occures during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in a high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100% tested.
11. This value is measured from CS2 going low to the end of write cycle.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

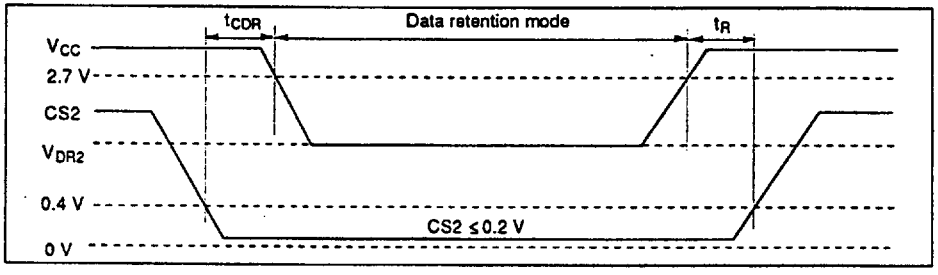
This characteristics is guaranteed only for L-, L-L, and L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 $\geq V_{CC} - 0.2$ V or 0 V $\leq$ CS2 $\leq$ 0.2 V, Vin $\geq$ 0 V	
Data retention current	I_{CCDR}	—	1	50*1	µA	V_{CC} = 3.0 V, Vin $\geq$ 0V, $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 $\geq V_{CC} - 0.2$ V or 0 V $\leq$ CS2 $\leq$ 0.2 V	Lversion
		—	1	30*2	µA		L-Lversion
		—	1	15*3	µA		L-SLversion
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform	
Operation recovery time	t_R	5	—	—	ms		

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: 1. 20 µA max at Ta = 0 to 40°C (Lversion).
2. 6 µA max at Ta = 0 to 40°C (L-Lversion).
3. 3 µA max at Ta = 0 to 40°C (L-SLversion).
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 $\geq V_{CC} - 0.2$ V or 0 V $\leq$ CS2 $\leq$ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

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