

FAN8000D (KA9268D)

4-CH Motor Driver

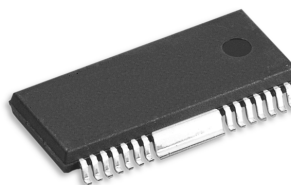
Features

- Built in 4-CH balanced transformerless(BTL) driver
- Output gain adjustable
- Built in normal OP-amp
- Built in mute function
- Built in level shift circuit
- Built in thermal shutdown function
- Operating range 4.5~13.2V

Description

The FAN8000D is a monolithic integrated circuit, suitable for 4-CH motor driver which drives tracking actuator, focus actuator, sled motor and tray motor of CD/CD-ROM/DVD system.

28-SSOPH-375



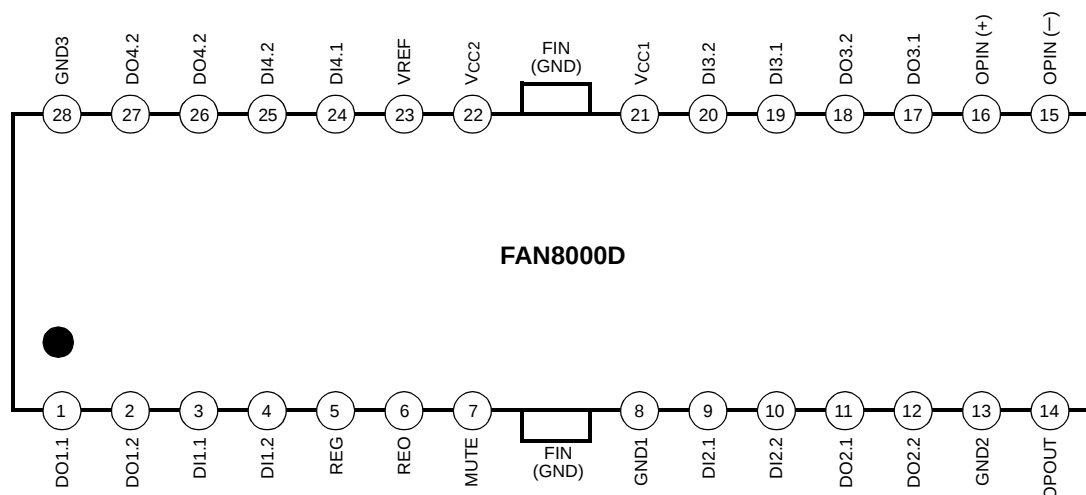
Target Application

- Compact disk player
- Video compact disk player
- Digital Video Disk Player
- Car compact disk player

Ordering Information

Device	Package	Operating Temp.
FAN8000D	28-SSOPH-375	-40°C ~ +85°C
FAN8000DTF	28-SSOPH-375	-40°C ~ +85°C

Pin Assignments



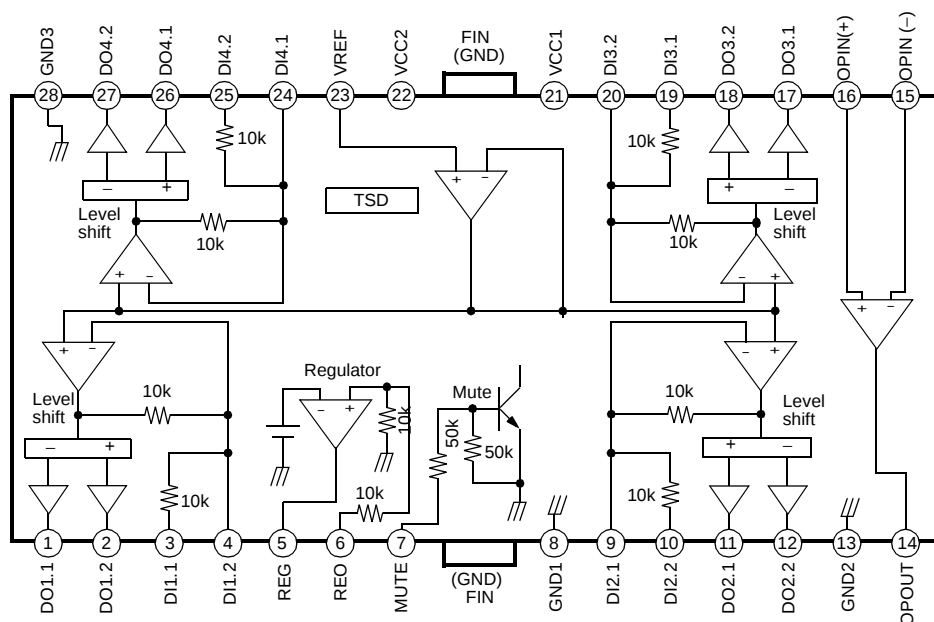
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	DO1.1	O	Drive output
2	DO1.2	O	Drive output
3	DI1.1	I	Drive input
4	DI1.2	I	Drive input
5	REG	-	Regulator
6	REO	O	Regulator output
7	MUTE	I	Mute
8	GND1	-	Ground 1
9	DI2.1	I	Drive input
10	DI2.2	I	Drive input
11	DO2.1	O	Drive output
12	DO2.2	O	Drive output
13	GND2	-	Ground 2
14	OPOUT	O	Op-amp output
15	OPIN(-)	I	Op-amp input (-)
16	OPIN(+)	I	Op-amp input (+)
17	DO3.1	O	Drive output
18	DO3.2	O	Drive output
19	DI3.1	I	Drive input
20	DI3.2	I	Drive input
21	VCC1	-	Supply voltage
22	VCC2	-	Supply voltage
23	VREF	I	2.5V bias voltage
24	DI4.1	I	Drive input

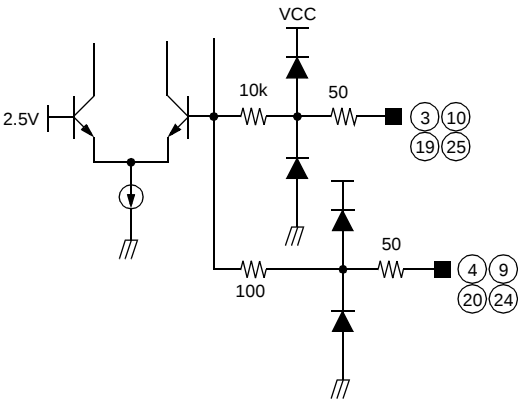
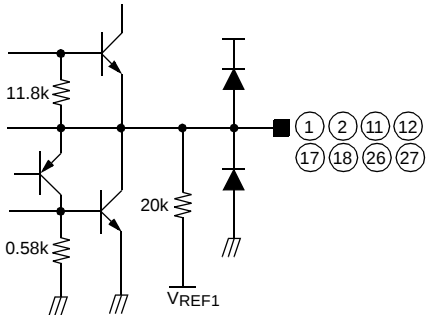
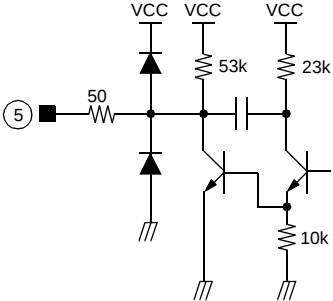
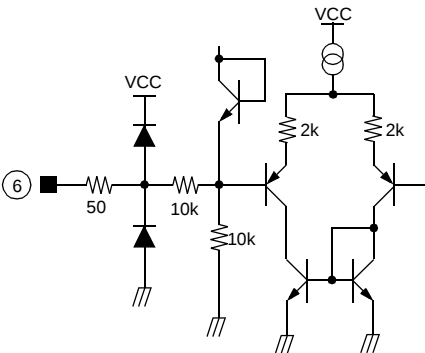
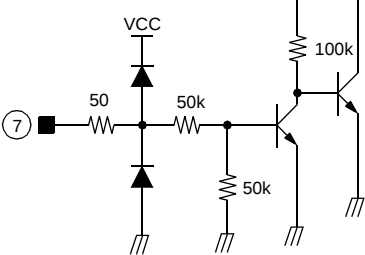
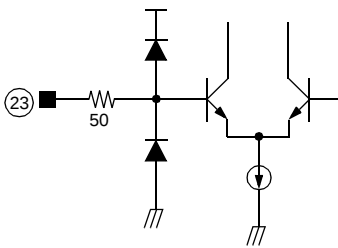
Pin Definitions (Continued)

Pin Number	Pin Name	I/O	Pin Function Description
25	DI4.2	I	Drive input
26	DO4.1	O	Drive output
27	DO4.2	O	Drive output
28	GND3	-	Ground 3

Internal Block Diagram



Equivalent Circuits

Driver input	Driver output
 The Driver input circuit diagram shows a 2.5V source connected to a differential pair of transistors. The gates of these transistors are connected to a common node that is biased by a VCC source through a 10k resistor and a 50 resistor. The gates are also connected to a 100 resistor to ground. The drains of the transistors are connected to a 50 resistor to a VCC source and a 50 resistor to a 100 resistor to ground. The output nodes are labeled with pin numbers: (3), (10), (19), (25) for the top output and (4), (9), (20), (24) for the bottom output.	 The Driver output circuit diagram shows a differential pair of transistors. The gates are connected to a common node that is biased by a VREF1 source through a 20k resistor. The gates are also connected to a 11.8k resistor to VCC and a 0.58k resistor to ground. The drains are connected to a 50 resistor to VCC and a 50 resistor to ground. The output nodes are labeled with pin numbers: (1), (2), (11), (12), (17), (18), (26), (27).
Regulator	Regulator output
 The Regulator circuit diagram shows a differential pair of transistors. The gates are connected to a common node that is biased by a VCC source through a 50 resistor and a 53k resistor. The gates are also connected to a 23k resistor to VCC and a 10k resistor to ground. The drains are connected to a 50 resistor to VCC and a 50 resistor to ground. The output nodes are labeled with pin numbers: (5), (10), (19), (25).	 The Regulator output circuit diagram shows a differential pair of transistors. The gates are connected to a common node that is biased by a VCC source through a 50 resistor and a 10k resistor. The gates are also connected to a 10k resistor to VCC and a 10k resistor to ground. The drains are connected to a 50 resistor to VCC and a 50 resistor to ground. The output nodes are labeled with pin numbers: (6), (10), (19), (25).
Mute input	Bias input
 The Mute input circuit diagram shows a differential pair of transistors. The gates are connected to a common node that is biased by a VCC source through a 50 resistor and a 50k resistor. The gates are also connected to a 100k resistor to VCC and a 50k resistor to ground. The drains are connected to a 50 resistor to VCC and a 50 resistor to ground. The output nodes are labeled with pin numbers: (7), (10), (19), (25).	 The Bias input circuit diagram shows a differential pair of transistors. The gates are connected to a common node that is biased by a VCC source through a 50 resistor. The gates are also connected to a 50 resistor to ground. The drains are connected to a 50 resistor to VCC and a 50 resistor to ground. The output nodes are labeled with pin numbers: (23), (10), (19), (25).

Electrical Characteristics

(Unless otherwise specified, Ta = 25 °C, VCC = 8V, RL=8Ω)

REGULATOR CIRCUIT

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Regulator output voltage	VREG	IL=100mA	4.75	5	5.25	V
Load regulation	ΔVRL	IL=0 ~ 200mA	-40.0	0	10.0	mV
Line regulation	ΔVCC	IL=200mA, VCC=6 ~ 9V	-10.0	0	20.0	mV

DRIVE CIRCUIT

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Quiescent circuit current	ICCQ	VI=0	5.5	9.5	13.5	mA
Input offset voltage	VOF	-	-5.0	0	5.0	mV
Output offset voltage	VOO	-	-30	0	30	mV
Maximum sink current	ISINK	RL=4Ω, VCC	0.5	0.8	-	A
Maximum source current	ISOURCE	RL=4Ω, GND	0.5	0.8	-	A
Maximum output voltage	VOM	VI=2VRMS, 1kHz	2.5	3.0	-	V
Closed loop voltage gain	AVF	VI=0.1VRMS, 1kHz	10.5	12.0	13.5	dB
Ripple rejection ratio	RR	VI=-20dB, 120Hz	60.0	80.0	-	dB
Slew rate	SR	100Hz, Square wave	1.0	2.0	-	V / μs

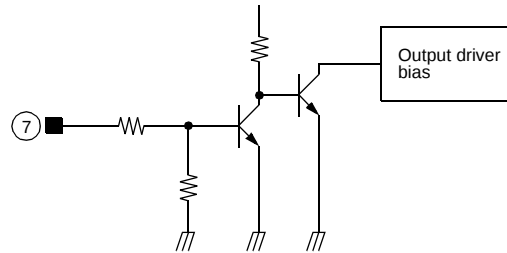
OP AMP CIRCUIT

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input offset voltage	VOF1	-	-5	-	+5	mV
Input bias current	IB1	-	-	-	300	nA
High level output voltage	VOH1	-	6	-	-	V
Low level output voltage	VOL1	-	-	-	1.8	V
Output sink current	ISINK1	RL=50Ω, GND	10	40	-	mA
Output source current	ISOURCE1	RL=50Ω, VCC	10	50	-	mA
Open loop voltage gain	GVO1	VIN=-75dB, f=1kHz	65	78	-	dB
Ripple rejection ratio	RR1	VIN=-20dB, f=120kHz	50	70	-	dB
Slew Rate	SR1	Square, VOUT=2Vp-p, f=120kHz	0.5	1	-	V / μs
Common mode rejection ratio	CMRR1	VIN=-20dB, f=1kHz	70	84	-	dB

Application Information

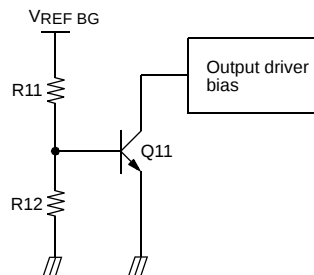
1. MUTE

Pin #7	Mute circuit
High	Turn-off
Low	Turn-on
Open	Turn-on



- When the pin7 is open or the voltage of the pin7 is below 0.5V, the mute circuit is activated so that the output circuit is muted.
- When the voltage of the pin7 is above 2V, the mute circuit is deactivated and the output circuit operates normally.
- If the chip temperature rises above 175°C, then the TSD (Thermal Shutdown) circuit is activated and the output circuit is muted.

2. TSD (THERMAL SHUTDOWN)

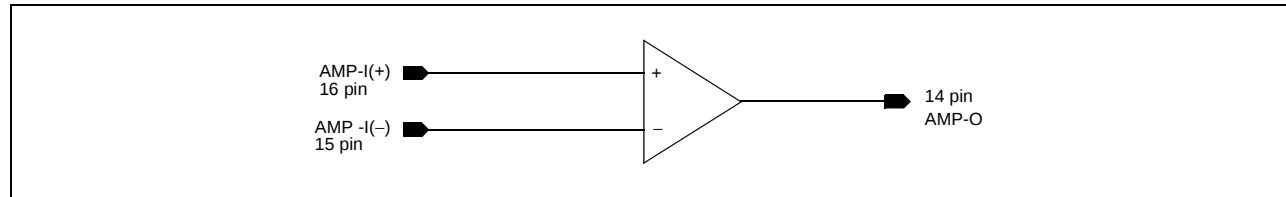


- The $V_{REF\ BG}$ is the output voltage of the band-gap-referenced biasing circuit and acts as the input voltage of the TSD circuit.
- The base-emitter voltage of the TR, Q11 is designed to turn-on at below voltage.

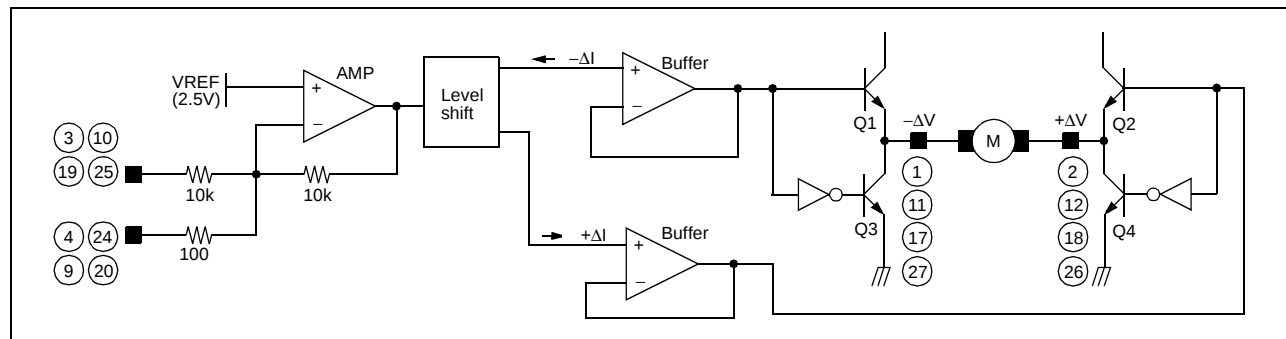
$$V_{BE} = V_{REF\ BG} \times R12 / (R11 + R12) = 460mV$$
- When the chip temperature rises up to 175°C, then the turn-on voltage of the Q11 would drop down to 460mV. (Hysteresis: 25°C)
 Hence, the Q11 would turn on so the output circuit will be muted.

3. OP-AMP

OP-amp is integrated in the IC for user's convenience.

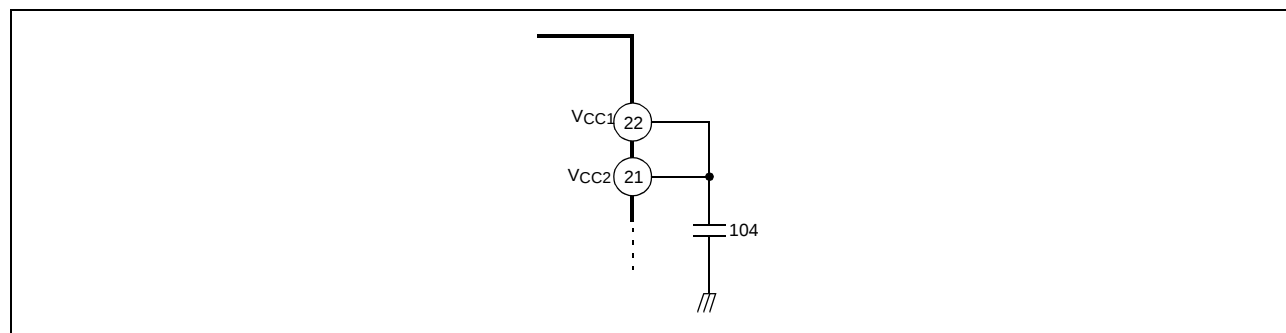


4. DRIVER



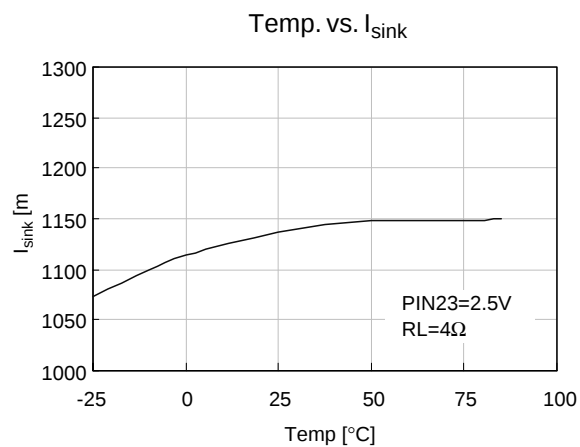
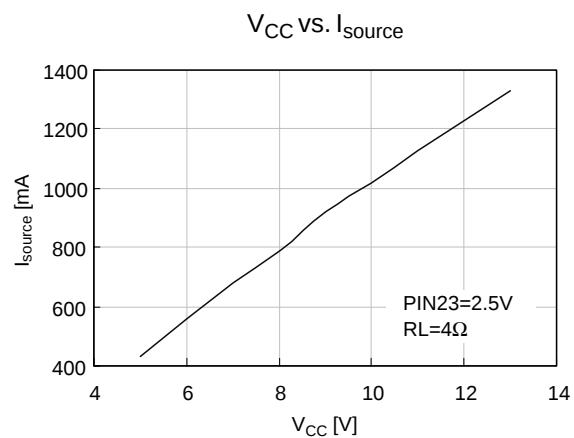
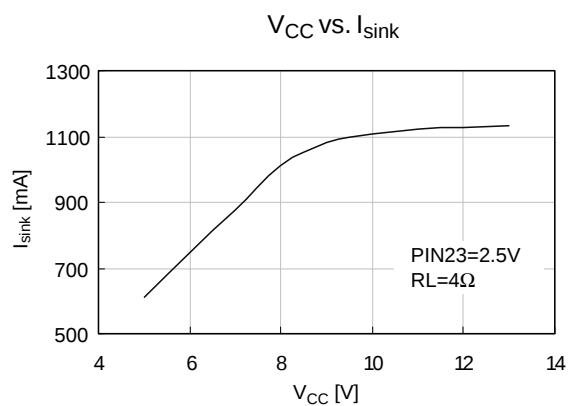
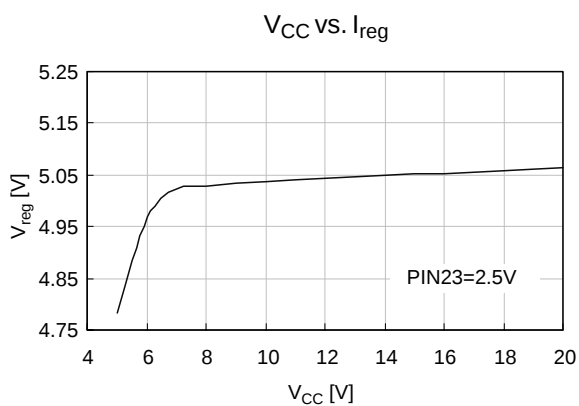
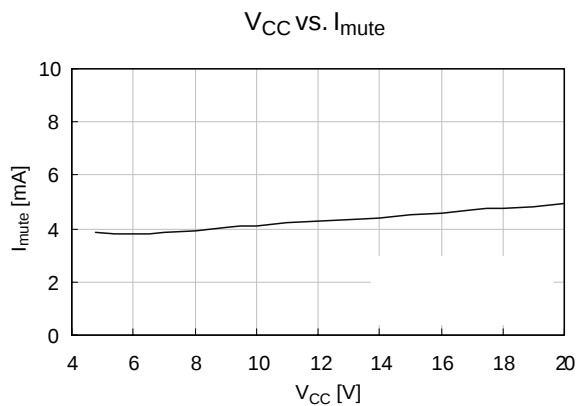
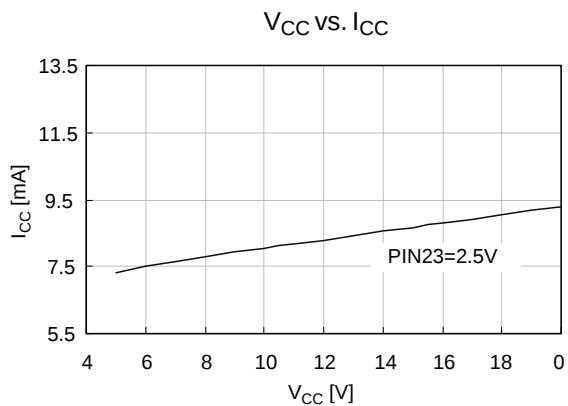
- The voltage, V_{REF} , is the reference voltage given by the bias voltage of the pin23.
- The input signal through the pin3 is amplified by 10k/10k times and then fed to the level shift.
- The level shift produces the current due to the difference between the input signal and the arbitrary reference signal. The current produced as $+\Delta I$ and $-\Delta I$ is fed into the driver buffer.
- Driver Buffer drives the power TR of the output stage according to the input signal.
- The output stage is the BTL driver and the motor is rotating in forward direction by operating TR Q1 and TR Q4. On the other hand, if TR Q2 and TR Q3 is operating, the motor is rotating in reverse direction.
- When the input voltage through the pin3 is below the V_{REF} , the motor rotates in forward direction.
- When the input voltage through the pin3 is above the V_{REF} , the motor rotates in reverse direction.
- To change the gain, pin4 or 24 can be used.

5. Connect a by-pass capacitor, 0.1 μ F between the supply voltage source.

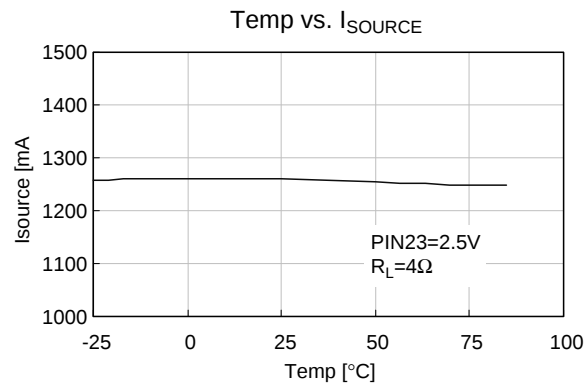
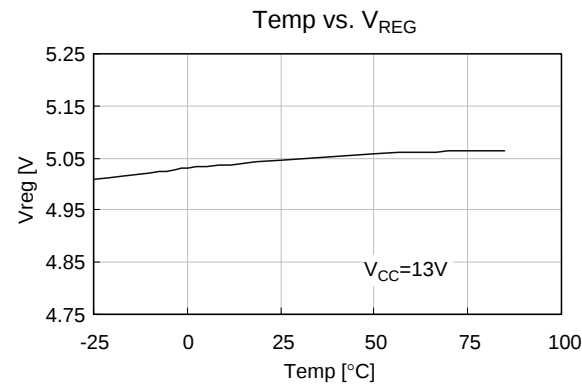
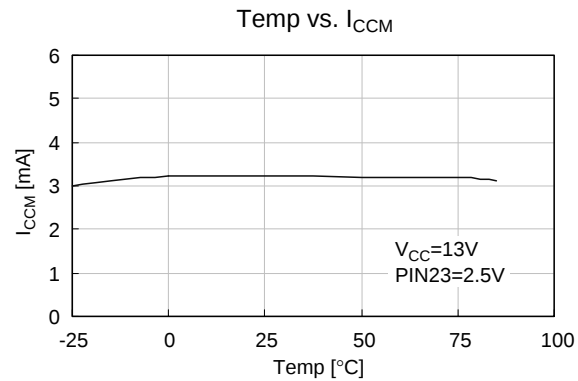
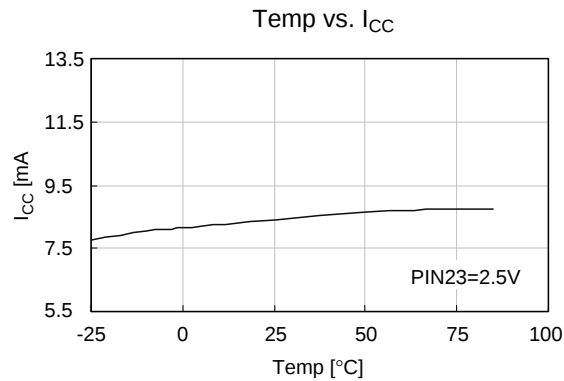


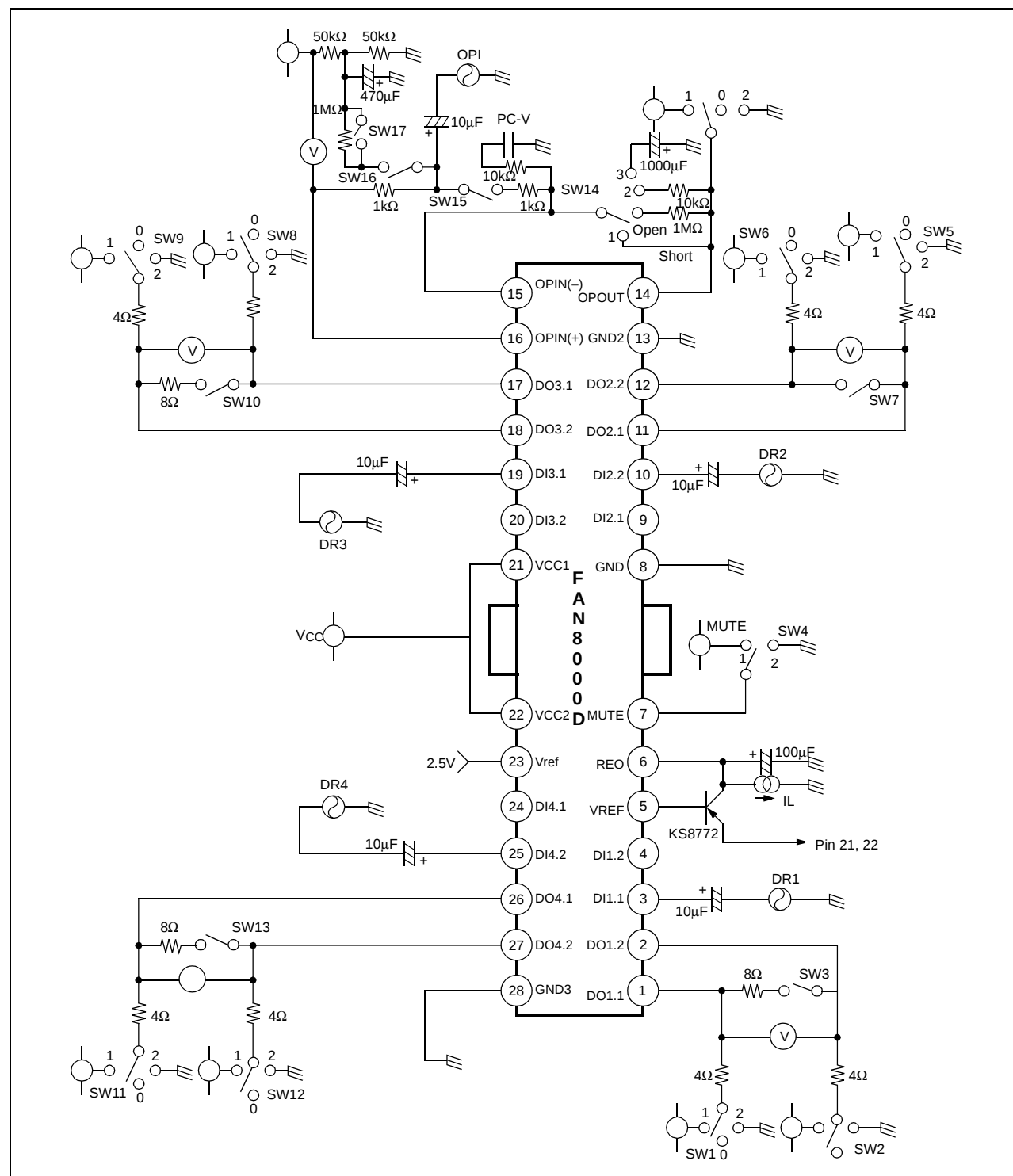
6. Radiation fin is connecting to the internal GND of the package.
Connect the fin to the external GND.

Typical Performance Characteristics

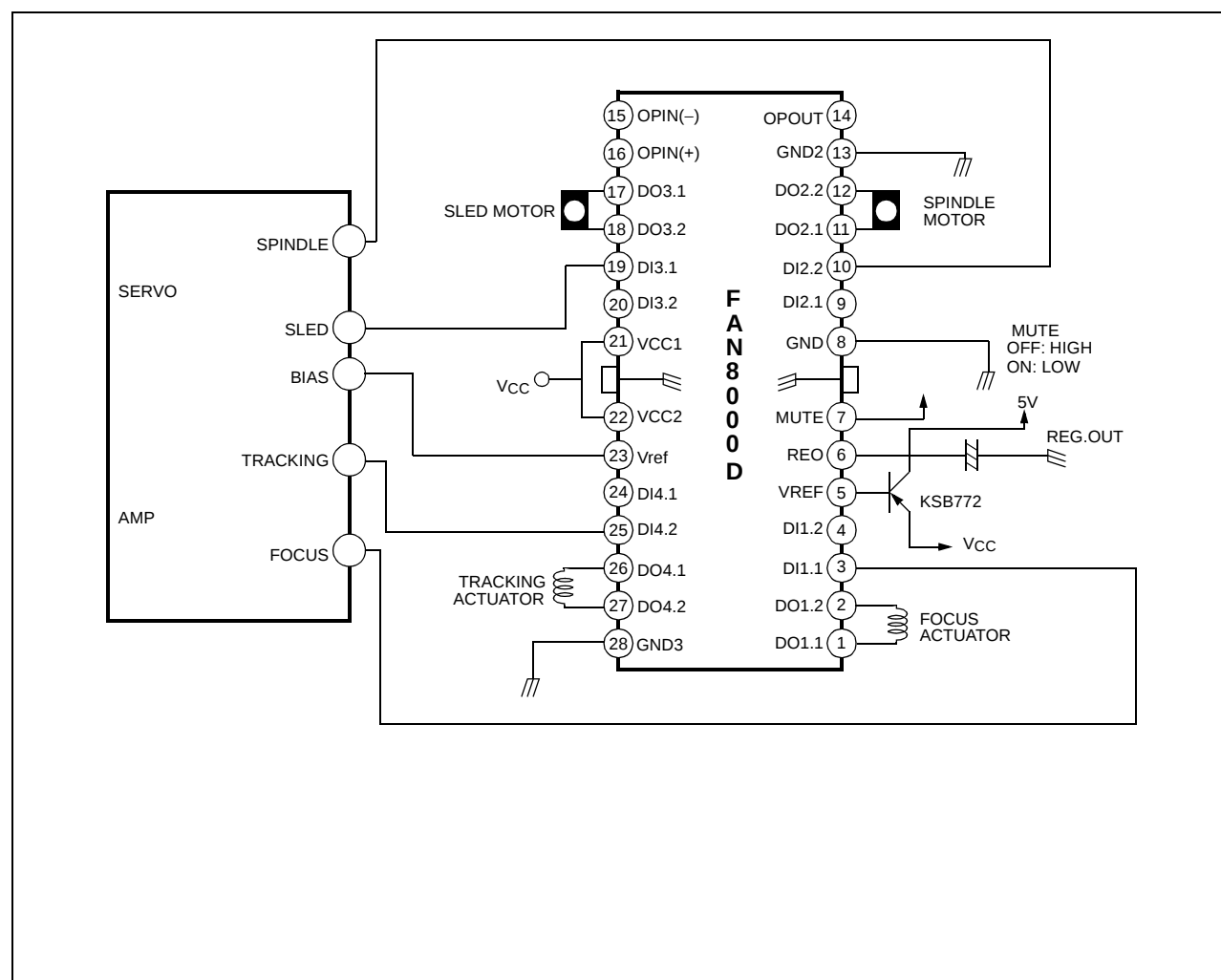


Typical Performance Characteristics (Continued)





Application Circuits



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.