19-3559; Rev 0; 1/05

EVALUATION KIT AVAILABLE

Integrated L1-Band GPS Receiver

MAX2741

General Description

The MAX2741 L1-band GPS receiver IC offers a high-performance, compact solution for mobile handsets, PDAs, and automotive applications. Total voltage gain of 80dB and a 4.7dB cascaded noise figure can provide receiver sensitivity for applications requiring -185dBW for indoor tracking solutions.

This dual-conversion receiver downconverts the 1575.42MHz GPS signal to a 37.38MHz first IF, and then a 3.78MHz second IF. An integrated 2- or 3-bit ADC (1-bit SIGN, 1- or 2-bit MAG selectable) samples the second IF and outputs the digitized signals to the baseband processor.

The integrated synthesizer offers the flexibility in frequency planning to allow a single board design to be employed for reference frequencies from 2MHz to 26MHz. The integrated reference oscillator allows either TCXO or crystal operation.

The receiver runs from a 2.7V to 3.0V supply, and draws only 30mA when active. It is offered in a 28-pin thin QFN package, and is specified for -40°C to +85°C at 3V.

28-PIN THIN QFN 5.0mm x 5.0mm

Applications

In-Vehicle Navigation Systems (IVNS)

Telematics (Vehicle and Asset Tracking, Inventory Management)

Automotive Security

Emergency Response Systems

Emergency Road-Side Assistance

Location-Based Services/Internet (PDAs)

Digital Cameras/Camcorders

Recreational Handhelds/Walkie-Talkies

Geographical Information Systems (GIS)

Consumer Electronics (Location-Based Games)

Precision Timing

Features

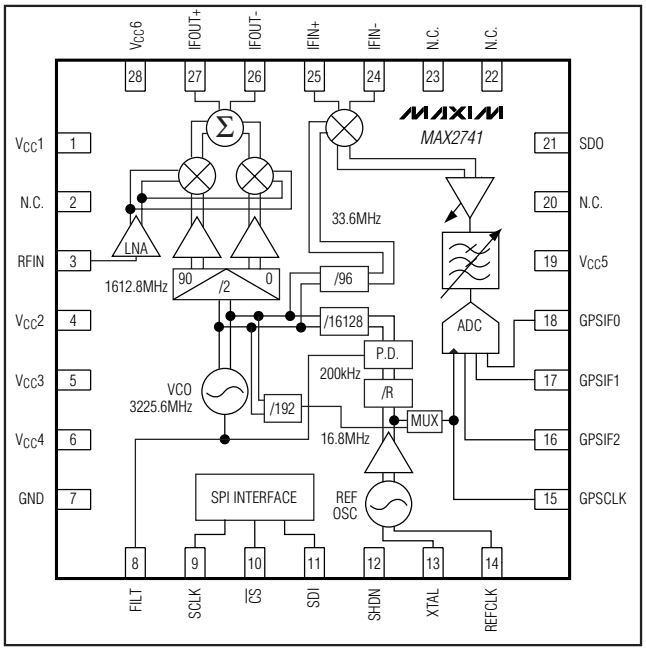
- ♦ **Supports All Popular Handset Reference Frequencies Up to 26MHz**
- ♦ **4.7dB Cascaded Noise Figure**
- ♦ **80dB Cascaded Gain**
- ♦ **Tolerates -90dBm In-Band Jammer**
- ♦ **Tolerates +13dBm CDMA Out-of-Band Jammer at Device Input**
- ♦ **Integrated Synthesizer and VCO**
- ♦ **Integrated 2- or 3-Bit ADC**
- ♦ **50dB IF AGC Range**
- ♦ **Small 28-Pin Thin QFN Package**
- ♦ **SPI™ Control Interface**
- ♦ **Clock Output for Baseband Processor**

SPI is a trademark of Motorola, Inc.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2741ETI	-40°C to +85°C	28 Thin QFN

Pin Configuration/ Functional Diagram



ABSOLUTE MAXIMUM RATINGS

V_{CC} Pins to GND .....-0.3V to +3.3V
V_{CC} Pins to Each Other .....-0.3V to +0.3V
FILT to GND.....-0.3V to (V_{CC} + 0.3V)
CMOS Inputs to GND (SHDN, SCLK, $\overline{CS}$, SDI).....+0.3V to (V_{CC} + 0.3V)
CMOS Outputs to GND (CLKOUT, GPSIF_, SDO).....-0.3V to (V_{CC} + 0.3V)
RFIN to GND.....-0.3V to (V_{CC} + 0.3V)
First IF Filter I/O to GND (IFOUT±, IFIN±).....-0.3V to (V_{CC} + 0.3V)
Crystal Inputs to GND (XTAL, REFCLK).....-0.3V to (V_{CC} + 0.3V)
Maximum RF Input Power.....0dBm
Continuous Power Dissipation (T_A = +85°C)
28-Pin Thin QFN (derate 20.8mW/°C above +70°C) .1000mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(Operating conditions (unless otherwise specified): V_{CC} = 2.7V to 3.0V; REFCLK driven with 10MHz sinusoid, 1.2V_{P-P}; registers set according to mode; no RF input signal; digital baseband outputs left open; T_A = -40°C to +85°C. Typical values are measured at V_{CC} = 2.75V, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.7		3.0	V
Supply Current	Normal operation (T_A = +25°C)		30	42	mA
	Standby (V_{SHDN} = V_{IL}, SYNTH:D8 = 0)		0.7		
Input-Logic High Threshold		V_{CC} - 0.1			V
Input-Logic Low Threshold				0.1	V
Input-Logic High/Low Current		-10		+10	µA
Output-Logic High	I_{LOAD} = 100µA	V_{CC} - 0.3			V
Output-Logic Low	I_{LOAD} = 100µA			0.3	V

AC ELECTRICAL CHARACTERISTICS

(Operating conditions (unless otherwise specified): V_{CC} = 2.7V to 3.0V for T_A = -40°C to +85°C; REFCLK driven at 10MHz sinusoid, 1.2V_{P-P}; registers set according to mode; using the *Typical Application Circuit*; CW RF signal at 1575.42MHz. Typical values are measured at V_{CC} = 2.75V, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1st CONVERSION STAGE (RF TO 1st IF)					
RF Frequency	L1-band		1575.42		MHz
RF Conversion Gain	(Note 1)	15	21	32	dB
Noise Figure	Mid-gain (CONFIG1:D4–D0 = 10000)		4.7		dB
Input IP3	(Note 2)		-30		dBm
RF Image Rejection	(Notes 3, 4)	20	35		dB
LO Leakage at RF	LO to RFIN pin		-90		dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(Operating conditions (unless otherwise specified): V_{CC} = 2.7V to 3.0V for T_A = -40°C to +85°C; REFCLK driven at 10MHz sinusoid, 1.2V_{P-P}; registers set according to mode; using the *Typical Application Circuit*; CW RF signal at 1575.42MHz. Typical values are measured at V_{CC} = 2.75V, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2nd CONVERSION STAGE (1st IF TO ADC INPUT)					
1st IF Frequency	At IFOUT		37.38		MHz
Conversion Gain	Max gain (CONFIG1:D4–D0 = 11111) (Note 1)	48	61	74	dB
	Min gain (CONFIG1:D4–D0 = 00000) (Note 1)		10		dB
Input IP3	1st conversion (Note 5)		-36		dBm
Noise Figure	Max gain (CONFIG1:D4–D0 = 11111)		12		dB
IF Output Port Admittance	Real		0.40		mS
	Imaginary		1.5		pF
IF Input Port Admittance	Real		0.40		mS
	Imaginary		0.15		pF
LPF -3dB Corner Frequency	(SYNTH:D13–D10 = 1111)		2.9		MHz
	(SYNTH:D13–D10 = 0000)		7.7		
SYNTHESIZER					
I_{CP_OH}	PLL charge-pump source current		75		µA
I_{CP_OL}	PLL charge-pump sink current		-100		µA
Closed-Loop Phase Noise	At 1kHz offset		-55		dBc/Hz
Comparison Spurs	At ±200kHz offset		-44		dBc/Hz
Reference Oscillator Frequency	Sinusoid (Note 1)	2	10	26	MHz
REF Input Voltage Level	Sinusoid (Note 1)	0.6		2.2	V_{P-P}
VCO Coarse Tune Range	Programmable (CONFIG1:D7 to D5 = 000 to 111) (Note 1)		240		MHz
DIGITAL I/O					
SPI Clock Frequency			1		MHz

Note 1: Production tested for +25°C and +85°C, guaranteed by design and characterization for -40°C.
Note 2: Test tones at 1575.8MHz and 1576.8MHz at -60dBm/tone.
Note 3: Guaranteed by design and characterization.
Note 4: Image frequency is 1575.42MHz + 2(f_{IF}) = 1650.18MHz
Note 5: Test tones at 37.38MHz and 36.88MHz at -50dBm/tone.

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Pin Description

PIN	NAME	FUNCTION
1	$V_{CC}1$	LNA Supply Connection. External RF bypass capacitor to ground required.
2, 20, 22, 23	N.C.	Reserved. Make no connections to this pin.
3	RFIN	LNA Input. Connect to GPS antenna through a bandpass filter. This input requires an external matching network to match to 50Ω. AC-couple to this pin.
4	$V_{CC}2$	VCO Supply Connection. External RF bypass capacitor to ground required.
5	$V_{CC}3$	CML Supply Connection. External RF bypass capacitor to ground required.
6	$V_{CC}4$	Digital Logic and PLL Supply Connection. External RF bypass capacitor to digital ground required.
7	GND	Ground. Connect to PC board digital ground plane.
8	FILT	PLL Loop Filter Connection. This is the output of the phase detector's charge pump. Use the recommended filter on EV kit for optimal phase noise and lock time.
9	SCLK	SPI Clock Input (CMOS)
10	$\overline{CS}$	SPI Chip-Select Input (CMOS, Active Low)
11	SDI	SPI Data Input (CMOS)
12	SHDN	Full IC Power-Down. This shutdown pin disables the on-chip oscillator and the rest of the IC. To keep the oscillator running, use the software shutdown (SYNTH:D8); (CMOS, active high).
13	XTAL	Crystal Oscillator Feedback Capacitor Connection
14	REFCLK	Reference Clock Input for PLL. Drive with $1.2V_{P-P}$ when using TCXO module.
15	GPSCLK	GPS Clock Output to Baseband. This is the clock used by the ADC to sample the GPS data (CMOS).
16	GPSIF2	Sampled IF Output, Bit 2 (CMOS). See Table 5.
17	GPSIF1	Sampled IF Output, Bit 1 (CMOS). See Table 5.
18	GPSIF0	Sampled IF Output, Bit 0 (CMOS). See Table 5.
19	$V_{CC}5$	IF Supply Connection. External RF bypass capacitor to ground required.
21	SDO	SPI Data Output (CMOS)
24	IFIN-	1st IF Input (Inverting). Connect this 2.5kΩ differentially terminated input to the 1st IF filter's (-) output.
25	IFIN+	1st IF Input (Noninverting). Connect this 2.5kΩ differentially terminated input to the 1st IF filter's (+) output.
26	IFOUT-	1st IF Output (Inverting). Connect this 2.4kΩ differential output to the 1st IF filter's (-) input.
27	IFOUT+	1st IF Output (Noninverting). Connect this 2.4kΩ differential output to the 1st IF filter's (+) input.
28	$V_{CC}6$	RF Image-Reject Mixer Supply. External RF bypass capacitor to ground required.
Exposed	GND	RF Ground. Ultra-low inductance connection to ground. Place several vias to PC board ground plane.

Detailed Description

The MAX2741 GPS offers a high-performance superheterodyne receiver solution for low-power mobile devices, with the benefit of using the system's existing clock reference. This receiver is ideal for integration into mobile phone handsets using common reference frequencies such as 10.0, 13.0, 14.4, 19.2, 20.0, and 26.0MHz. The only external components required are the GPS RF filter, an IF filter (typically designed from inexpensive discretes), a three-component PLL loop filter, and a few other resistors and capacitors. The MAX2741 integrates the reference oscillator core, the VCO and its tank, the synthesizer, a 1- to 3-bit ADC, and all signal path blocks except for the 1st IF filter. The typical application area for the receiver is less than $2cm^2$.

RF/1st Conversion Stage (Front-End)

The MAX2741 RF front-end LNA and mixer are the most important in the signal path. This stage sets the noise figure for the receiver, defining the sensitivity, and mixes the 1575.42MHz L1-band GPS signal down to a 1st IF of 37.38MHz. The LNA itself has an NF of approximately 1.5dB; the cascaded NF of the front-end (including the mixer) is approximately 4.7dB, and the cascaded gain is typically 21dB.

The image-reject mixer is set up for a high-side injected RFLO (1612.80MHz), and offers typically better than 30dB rejection of the image noise (1650.18MHz). The -30dBm input 3rd-order intercept (IIP3) of the RF strip, in conjunction with the GPS IF filter, provides excellent out-of-band interferer immunity.

The 1st IF outputs (IFOUT±) are internally biased to approximately 2V, and have a differential source impedance of approximately 2.5kΩ. The IF filter can be implemented as a discrete L/C filter, or as a monolithic SAW or ceramic if one is available.

IF/2nd Conversion Stage

The 2nd conversion stage consists of an active mixer, a variable-gain amplifier (VGA), and a tunable lowpass filter. The IF mixer is configured for low-side LO injection for a 2nd IF of 3.78MHz. Total gain in this stage is 62dB, and the VGA offers 51dB of gain adjustment. The VGA is typically controlled by the baseband IC through the SPI interface to optimize the signal swing for digitization by the ADC.

The on-chip lowpass filter has an adjustable cutoff frequency, programmable from 2.9MHz to 7.7MHz in 16 steps. This LPF further reduces out-of-band noise and band-limits the signal to the ADC, ensuring that the sampling process does not generate alias components.

DC offset compensation at the ADC input is performed by an on-chip 4-bit DAC. This compensates for any DC error introduced by transistor mismatch in the differential stage driving the ADC input, allowing the downconverted GPS signal's DC level to be centered within the threshold voltages of the ADC.

ADC

The on-chip ADC samples the down-converted GPS signal at the 2nd IF (3.78MHz). Sampled output is provided in either 2-bit (1-bit magnitude, 1-bit sign) or 3-bit (2-bit magnitude, 1-bit sign) formats, as determined by the ADC mode configuration bit (CONFIG1:D15); see Table 5 for details. The ADC sample clock (system GPS clock) is derived either directly from the reference clock (SYNTH:D9 = 1), or from an RFLO divide-by-96 block to provide a 16.8MHz sample clock (SYNTH:D9 = 0). The clock is available to the baseband processor at GPSCLK (pin 15). The sampled ADC data bits are available on pins 16, 17, and 18 (GPSIF2, GPSIF1, and GPSIF0). The functionality of the pins is different in each mode (2-bit vs. 3-bit)—see Table 5 in determining the interface connection for the application circuit.

Synthesizer

The MAX2741 integrates an integer-N synthesizer; all blocks except the loop filter are on-chip. The reference can be either a crystal (driven by the internal oscillator), or a TCXO module. The oscillator provides a 5pF load to the crystal. A TCXO module should provide a swing in the $0.6V_{P-P}$ to $2.2V_{P-P}$ range.

The reference divider (/R) is programmable (SYNTH: D7–D0), and can accommodate reference frequencies up to 26MHz. The reference divider needs to be set so the comparison frequency (f_{COMP}) at the frequency/phase detector is 200kHz. The VCO runs at twice the frequency of the RFLO; the RFLO is therefore generated from the VCO using a quadrature divide-by-2 block. The RF LO is f_{COMP} x 8064 (typically 1612.80MHz), and the 1st IF LO is f_{COMP} x 168 (typically 33.6MHz); the RF and IF LO division ratios are not adjustable. This configuration allows for the use of reference frequencies common to GSM, CDMA, TDMA, TD-SCDMA, and UMTS handsets: 9.6MHz (R = 48), 13.0MHz (R = 65), 14.4MHz (R = 72), 19.2MHz (R = 96), 26.0MHz (R = 130), etc.

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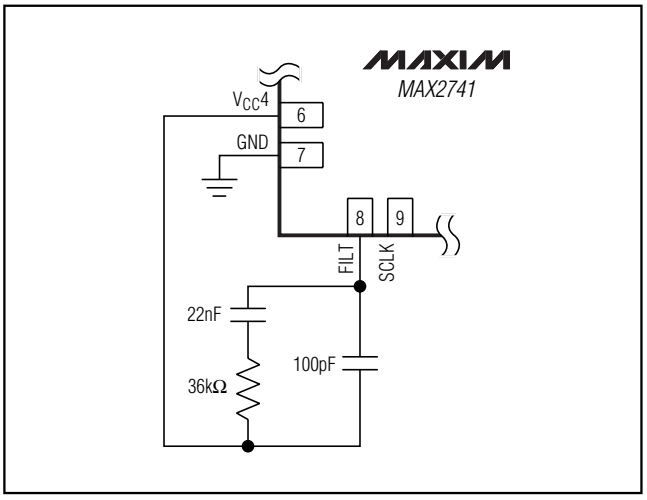

Figure 1. Recommended 3rd-Order PLL Filter

The VCO offers a bank of tuning capacitors that can be latched in/out to adjust the center frequency. Because the system does not require any RF LO frequency change (i.e., changing channels), the VCO varactor tuning gain is very low by design, which means the tuning range of the VCO is narrow. The coarse-tune capacitors in the tank circuit allow the system to adjust the VCO center frequency as needed to guarantee that the synthesizer can lock. In practice, process and temperature effects on VCO centering are negligible, and a coarse-tune setting of 110 (CONFIG:D7 to D5) will center the VCO tuning range correctly in virtually all cases. To aid in bench and prototype testing, the PFD offers out-of-lock-high and out-of-lock-low indicators, available in the SPI STATUS register (STATUS:D9 to D8). Use these flags to determine if the VCO tuning range needs to be adjusted higher or lower in the case where the PLL cannot lock.

The PLL filter is the only external block of the synthesizer. The typical filter is a classic C-R-C two-pole shunt network on the tune line. Low phase noise is preferred at the expense of longer PLL settling times, so a low 10kHz to 20kHz loop bandwidth is used. The recommended PLL 10kHz filter implementation, with charge pump set to 200µA (CONFIG1:D10 = 1), is shown in Figure 1.

The system/GPS clock is derived either directly from the reference oscillator, or synthesized from the RFLO (see the *ADC* section). This clock is used as the sampling clock for the on-chip ADC, and is seen at pin 15, GPSCLK.

SPI Bus, Address and Bit Assignments

An SPI-compatible serial interface is used to program the MAX2741 for configuring the different operating modes. In addition, data can be read out of the MAX2741 for status and diagnostic use. The serial interface is controlled by four signals: SCLK (serial clock), $\overline{CS}$ (chip-select), SDI (data input), and SDO (data output).

The control of the PLL, AGC, test, offset management, and block selection is performed through the SPI bus from the baseband controller. A 20-bit word, with the MSB (D15) being sent first, is clocked into a serial shift register when the chip-select signal is asserted low.

The SPI bus has four control lines: serial clock (SCLK), chip-select ($\overline{CS}$), data in (SDI), and data out (SDO). Enable SDO functionality by setting the digital test bus bits: CONFIG1:D9 to D8 = 01. The timing of the interface signals is shown in Figure 2 and Table 1 along with typical values for setup and hold time requirements.

For best performance, the SPI bus should be configured during the startup initialization and then left with the optimum values in the registers. Any changes to the ADC and VGA bits during GPS signal processing may cause glitches and corrupt the analog signal path. Reading from the SPI bus does not interrupt GPS operation.

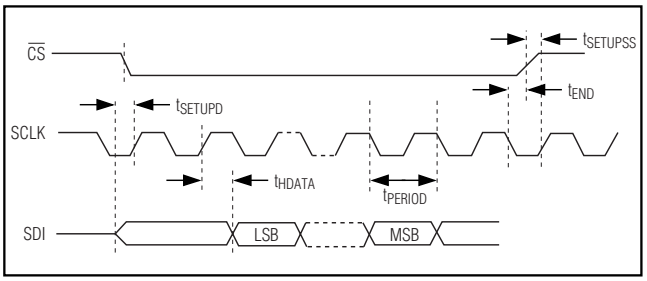

Figure 2. SPI Timing Diagram

Table 1. SPI Timing Requirements

SYMBOL	PARAMETER	TYP VALUE	UNITS
t_{SETUPD}	Data to SCLK setup	20	ns
t_{PERIOD}	SCLK period	100	ns
t_{HDATA}	Data hold to SCLK	20	ns
$t_{SETUPSS}$	$\overline{CS}$ to SCLK disable	20	ns
t_{END}	Falling SCLK to $\overline{CS}$ inactive	20	ns

Table 2. Register Address and Data Bit Assigments (Write)

REGISTER NAME	DATA																ADDRESS			
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
SYNTH	Reserved	LPF Autotune Initiate	LPF Tuning Word (MSB)	LPF Tuning Word	LPF Tuning Word	LPF Tuning Word (LSB)	XTAL Clock Select	Standby	PLL Ref Div Ratio (MSB)	PLL Ref Div Ratio	PLL Ref Div Ratio	PLL Ref Div Ratio	PLL Ref Div Ratio	PLL Ref Div Ratio	PLL Ref Div Ratio	PLL Ref Div Ratio (LSB)	0	1	0	0
CONFIG 1	ADC Mode	ADC Offset Control (LSB)	ADC Offset Control	ADC Offset Control (MSB)	ADC Offset Control (SIGN)	Double Charge-Pump Current	Digital Test Bus Mode Select (MSB)	Digital Test Bus Mode Select (LSB)	VCO Coarse Tuning Range (MSB)	VCO Coarse Tuning Range	VCO Coarse Tuning Range (LSB)	AGC Gain (MSB)	AGC Gain	AGC Gain	AGC Gain	AGC Gain (LSB)	0	1	0	1
CONFIG 2	Reset CMOS	Drive VCO Low	Drive VCO High	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Analog Test Mode Select	Analog Test Mode Select	Analog Test Mode Select	Analog Test Mode Select	Analog Test Mode Select	0	1	1	0

Table 3. Register Address and Data Bit Assigments (Read)

REGISTER NAME	DATA																ADDRESS			
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
STATUS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Out-of-Lock (High)	Out-of-Lock (Low)	XTAL Clock Selected	Parity	Reserved	LPF Auto-calibrate End	LPF Autotune (MSB)	LPF Autotune	LPF Autotune	LPF Autotune (LSB)	0	1	1	1

Detailed Register Definitions

Table 4. Detailed Register Definition for Write Address 0100: SYNTH

DATA BIT	DEFAULT	DESCRIPTION
D15	1	Reserved
D14	1	LPF Autotune Initiate: I = Initiate autotune, 0 = Manual tuning.
D13–D10	0100	LPF Tuning Word: 0000 ~ 7.7MHz, 1111 ~ 2.9MHz.
D9	1	XTAL Clock Select: 1 = External reference, 0 = Synthesized 16.8MHz.
D8	0	Standby: 0 = Normal operating mode, 1 = Standby (oscillator remains active), but only if D9 = 1.
D7–D0	01100000	Reference Division Ratio. Default 19.2MHz external reference (R = 96dec). R = f_{REF} / 200kHz.

Table 5. Detailed Register Definition for Write Address 0101: CONFIG 1

DATA BIT	DEFAULT	DESCRIPTION
D15	1	ADC Mode. Select 1 for 1-bit magnitude and sign, select 0 for 2-bit magnitude and sign. 1: GPSIF2 = sign, GPSIF1 = magnitude, GPSIF0 = X 0: GPSIF2 = MSB magnitude, GPSIF1 = LSB magnitude, GPSIF0 = sign
D14–D11	0000	ADC Offset Control (approx 4mV/step): D14 = LSB, D12 = MSB, D11 = sign.
D10	0	Double Charge-Pump Current: 0 = 100µA, 1 = 200µA.
D9 to D8	00	Digital Test Bus Mode Select. See Table 9 for test-mode descriptions.
D7 to D5	001	VCO Coarse Tuning Range. 000 = Lowest frequency, 111 = Highest frequency.
D4–D0	11111	AGC Gain. Digital control of the AGC amplifier in the 2nd IF section. 00000 => min gain, 11111 => max gain (linear gain ~2.5dB per unit SPI word).

Table 6. Detailed Register Definition for Write Address 0110: CONFIG 2

DATA BIT	DEFAULT	DESCRIPTION
D15	1	Reset CMOS: 0 = Hold CMOS dividers in reset and PFD is tri-stated, 1 = Inactive.
D14	1	Drive VCO Low: 0 = Active, forces VCO to lowest frequency. N.B. do not activate both D14 and D13 at the same time.
D13	1	Drive VCO High: <forces LCP low FET on, driving V_{TUNE} low, forcing VCO to highest extreme> 0 = Active, forces VCO to highest frequency. N.B. do not activate both D14 and D13 at the same time.
D12–D7	100000	Reserved
D6 to D5	11	Must be programmed to 11
D4–D0	11111	Analog Test Mode Select: Reserved

Table 7. Detailed Register Definition for Read Address 0111: STATUS

DATA BIT	DEFAULT	DESCRIPTION
D15–D10	XXXXXX	Reserved
D9	X	Out-of-Lock (High Frequency): 1 = PLL is out of lock, VCO free-running at its highest frequency, 0 = Locked.
D8	X	Out-of-Lock (Low Frequency): 1 = PLL is out of lock, VCO free-running at its lowest frequency, 0 = Locked high.
D7	1	XTAL Clock Selected: 1 = Synthesized 16.8MHz reference, 0 = External clock.
D6	X	Parity: 1 = Even, 0 = Odd.
D5	X	Reserved
D4	X	LPF Autotune End: 0 = Autotune run ended; 1 = Calibrating or manual tuning.
D3–D0	XXXX	LPF Autotune: 0000 ~ 7.7MHz; 1111 = 2.9MHz.

Applications Information

Fundamentally, the only application areas that require careful consideration are the LNA input match and the 1st IF filter. Of course, proper supply bypassing, grounding, and layout is required for reliable performance from any RF circuit.

LNA Input Matching

Input matching is critical for optimum noise figure and system sensitivity. Optimum source impedance (as seen from the LNA input) for lowest noise figure is 29Ω + j47Ω. Remember that optimum noise match and optimum gain match (return loss) do not occur simultaneously, so a good application circuit will sacrifice gain slightly in favor of reduced noise figure. Gain and noise circles are provided in Figure 3; S11 tabular data is provided in Table 8.

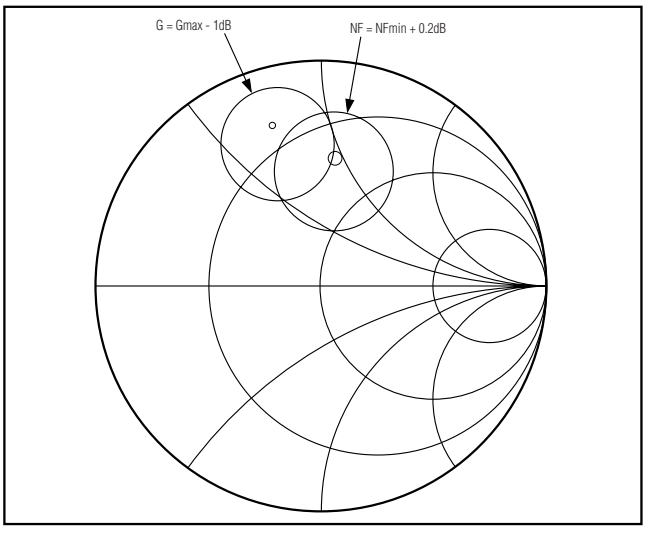

Figure 3. Gain and Noise Circles for MAX2741 LNA Input

Table 8. MAX2741 S11

FREQ (MHz)	S11 (MAG)	S11 (°)
1100	0.874	-50.9
1200	0.867	-56.1
1300	0.859	-61.5
1400	0.842	-66.9
1500	0.821	-72.3
1550	0.809	-74.9
1560	0.806	-75.4
1570	0.804	-75.9
1575	0.803	-76.2
1580	0.801	-76.4
1590	0.799	-77.0
1600	0.796	-77.5
1650	0.783	-80.0
1700	0.768	-82.5
1800	0.739	-87.4
1900	0.708	-92.3
2000	0.677	-96.8

1st IF Interface and Filtering

The typical application uses a 37.38MHz 1st IF, and employs an IF filter. The order of the filter should be tailored to suit the application—stand-alone GPS receivers will not require the channel-selection and stopband attenuation of GPS receivers that are integrated into other wireless handsets. Be sure that the filter topology provides DC-blocking for the IF I/O ports.

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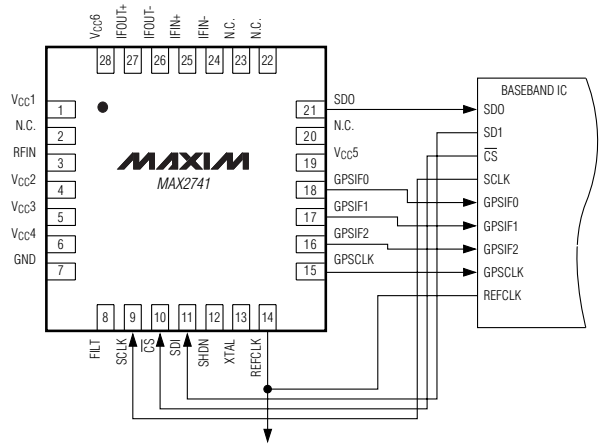
Typical Interface Diagram



Interface Summary

All I/O connections are DC-coupled. Supply voltages as specified in the electrical specifications.

RF		
I/O CONNECTION	**RECEIVER**	**RF BPF**
RFIN	LNA Input	RF BPF Output
IF		
I/O CONNECTION	**RECEIVER**	**IF FILTER**
IFOUT+	1st IF Output from Mixer (+)	IF BPF Input, 2.5kΩ Differential
IFOUT-	1st IF Output from Mixer (-)	IF BPF Input, 2.5kΩ Differential
IFIN+	1st IF Input (+)	IF BPF Input, 2.5kΩ Differential
IFIN-	1st IF Input (-)	IF BPF Input, 2.5kΩ Differential
BASEBAND		
I/O CONNECTION	**RECEIVER**	**BB IC/MAC**
SCLK	CMOS Input	CMOS Output
$\overline{CS}$	CMOS Input	CMOS Output
SDI	CMOS Input	CMOS Output
SDO	CMOS Output	CMOS Input
SHDN	CMOS Input	CMOS Output
GPSCLK	CMOS Output	CMOS Input
GPSIF0	CMOS Output	CMOS Input
GPSIF1	CMOS Output	CMOS Input
GPSIF2	CMOS Output	CMOS Input
SYNTHESIZER		
I/O CONNECTION	**RECEIVER**	**EXTERNAL COMPONENTS**
FILT	PLL Phase-Detector Charge-Pump	PLL Loop Filter
XTAL	Crystal Oscillator Feedback	Feedback Capacitors
REFCLK	External TCXO or Crystal	Analog (also connected to REFCLK input to MAC)

Typical Application Circuit

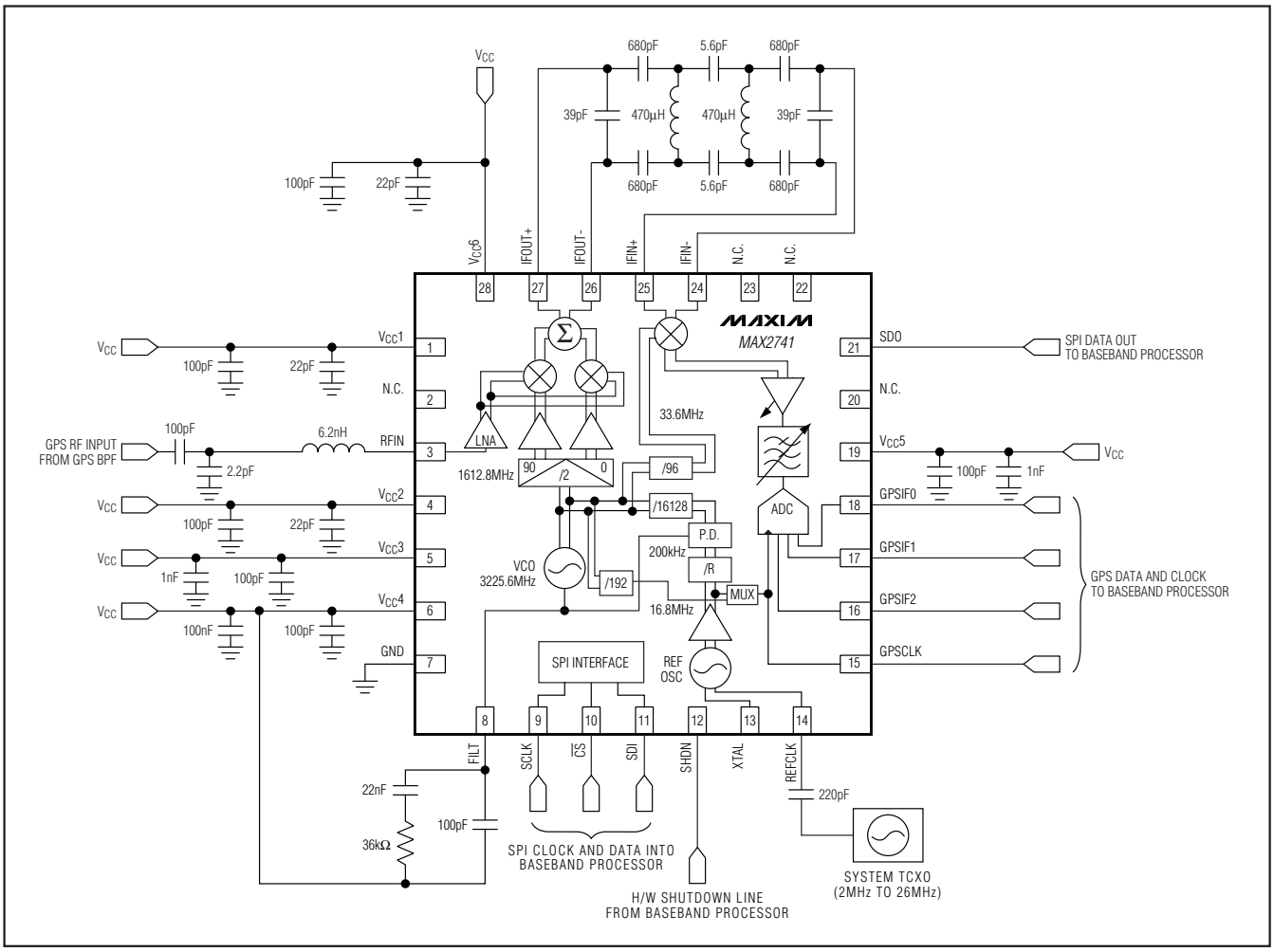


Table 9. Digital Test-Mode-Select Description

MODE	REGISTER SETTING CONFIG1:D9 to D8	DIGITAL OUTPUT FUNCTION		
		GPSIF2	GPSIF1	GPSIF0
3	11	SIGN	LSB	MSB
2	10	M COUNTER	R COUNTER	HANDSHAKE STATUS
1	01	CHARGE PUMP UP	CHARGE PUMP DOWN	SDO
0	00	CML CLOCK	CALIBRATE LPF END	XTL CLOCK SELECTED

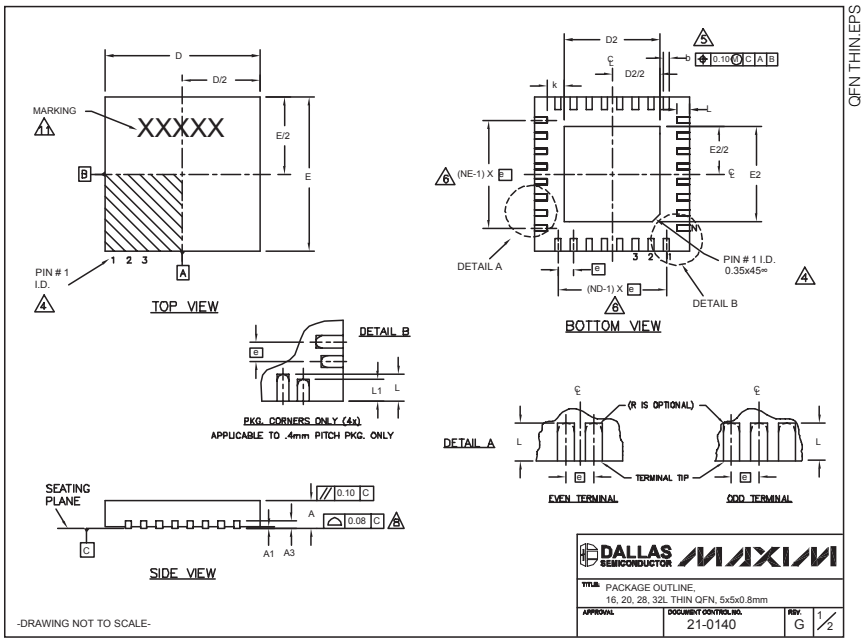
Digital Test Bus

The digital test bus (DTB) is provided to allow for easy bench analysis of the digital workings of the receiver.

Integrated L1-Band GPS Receiver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
L1	-	-	-	-	-	-	-	-	-	-	-	-
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	N
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 16, 20, 28, 32L THIN QFN, 5x5x0.8mm
21-0140
G
2/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.