



T-75-11-21

# MV8804

## 8 x 4 BIDIRECTIONAL ANALOG SWITCH ARRAY

The MV8804 is a CMOS/LSI 8 x 4 Analog Switch Array incorporating control memory (32 bits), decoder and digital logic level converters. The circuit has digitally-controlled analog switches having very low 'ON' resistance and very low 'OFF' leakage current. The switches will operate with analog signals at frequencies up to 40MHz and up to 13.0V peak-to-peak. A 'HIGH' on the Master Reset input switches all channels 'OFF' and clears the memory. The MV8804 is ideal for crosspoint switching applications.

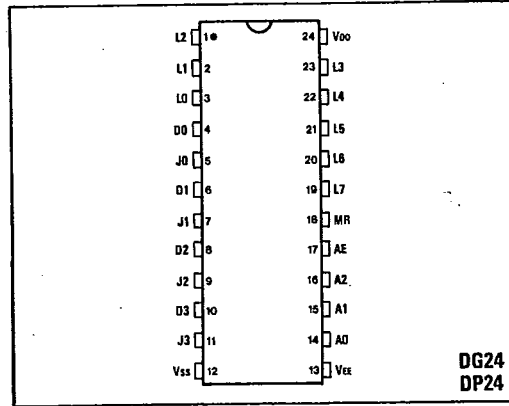


Fig.1 Pin connections - top view

### FEATURES

- Microprocessor Compatible Control Inputs
- On-Chip Control Memory And Address Decoding
- Row Addressing
- Master Reset
- 32 Crosspoint Switches in 8 x 4 Array
- 5.0V to 13.0V Operation
- Low Crosstalk Between Switches
- Low On Resistance: 90Ω (typ.) At 10V
- Matched Switch Characteristics
- Switches Frequencies Up To 40MHz

### APPLICATIONS

- PABX And Key Systems
- Data Acquisition Systems
- Test Equipment/Instrumentation
- Analog/Digital Multiplexers

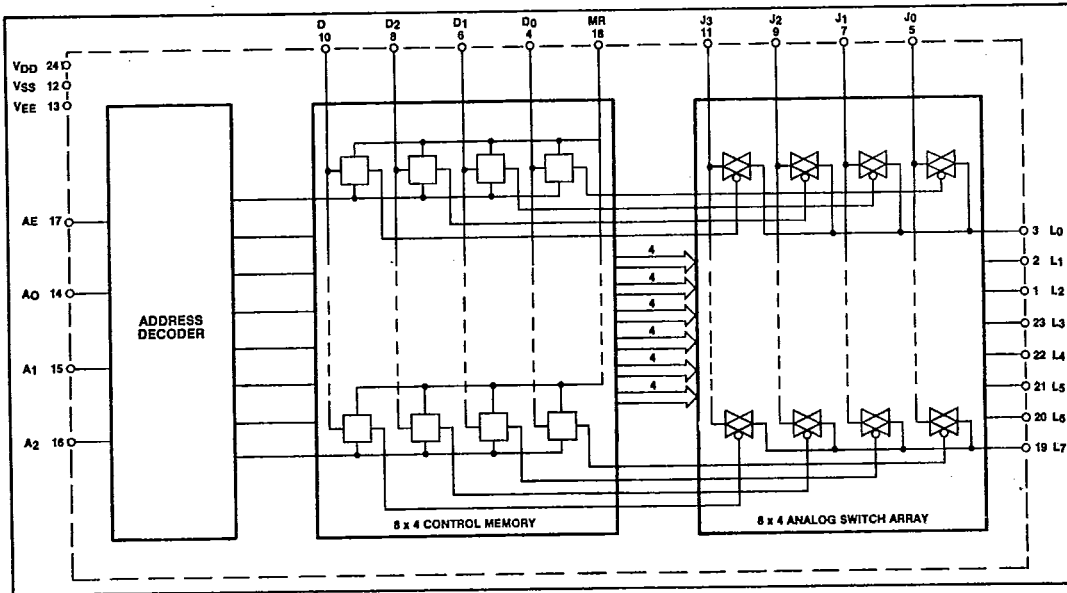


Fig.2 MV8804 functional block diagram

MV8804

PLESSEY SEMICONDUCTORS T-75-11-21

**ABSOLUTE MAXIMUM RATINGS**

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

	Min.	Max.		Min.	Max.
V <sub>DD</sub> - V <sub>SS</sub>	-0.3V	16V	Storage temperature (DP package)	-65°C	+125°C
V <sub>DD</sub> - V <sub>EE</sub>	-0.3V	16V	Power dissipation (DG package)		1200mW*
V <sub>SS</sub> - V <sub>EE</sub>	-0.3V	16V	Power dissipation (DP package)		600mW**
Voltage on any logic pin	V <sub>SS</sub> - 0.3V	V <sub>DD</sub> + 0.3V			
Voltage on any line (V <sub>I</sub> ) or junctor (V <sub>J</sub> )	V <sub>EE</sub> - 0.3V	V <sub>DD</sub> + 0.3V			
Current at any logic pin		10mA			
Operating temperature (all packages)	-40°C	+85°C			
Storage temperature (DG package)	-65°C	+150°C			

\* Derate 16mW/°C above 75°C. All leads soldered to PC board.

\*\* Derate 6.3mW/°C above 25°C. All leads soldered to PC board.

**AC ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated):

T<sub>amb</sub> = +25°C, V<sub>SS</sub> - V<sub>EE</sub> = 0V, V<sub>IS</sub> = 5V p-p, C<sub>L</sub> = 50pF, R<sub>L</sub> = 10kΩ, t<sub>r</sub> = t<sub>f</sub> = 20ns (input signal)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Sine wave response (distortion)			0.1		%	V <sub>DD</sub> = 13V } V <sub>DD</sub> = 10V } V <sub>DD</sub> = 5V } f <sub>in</sub> = 1kHz
			0.2		%	
			1.0		%	
Frequency response channel 'ON' (sine wave input)			40	MHz	V <sub>C</sub> = V <sub>DD</sub> = 10V, $\frac{V_o}{V_i} = -3dB$	
Feedthrough channel 'OFF'			-40	dB	V <sub>DD</sub> = 10V, V <sub>C</sub> = V <sub>EE</sub> , R <sub>L</sub> = 1kΩ, f <sub>in</sub> = 1MHz	
Crosstalk between any two channels			-40	dB	f <sub>in</sub> = 1.0MHz, V <sub>DD</sub> = 10V, Switch A 'ON', Switch B 'OFF'	
			-90	dB	f <sub>in</sub> = 3.4kHz, V <sub>DD</sub> = 10V, Switch A 'ON', Switch B 'OFF'	
Propagation delay Signal input to signal output	t <sub>PS</sub>		10	ns	V <sub>DD</sub> = 10V, Switch 'ON'	
Turn 'ON' propagation delay Data input to signal output	t <sub>PLH</sub>		200	ns	V <sub>DD</sub> = 10V	
	t <sub>PHL</sub>		400	ns	V <sub>DD</sub> = 5V	
Address enable to signal output	t <sub>PAE</sub>		300	ns	V <sub>DD</sub> = 10V	
			600	ns	V <sub>DD</sub> = 5V	
Minimum address enable (AE) Pulse width	t <sub>AE</sub>		90	ns	V <sub>DD</sub> = 10V	
			225	ns	V <sub>DD</sub> = 5V	
Minimum set-up time Address to AE	t <sub>s</sub>	0	50	ns	V <sub>DD</sub> = 10V	
		0	90	ns	V <sub>DD</sub> = 5V	
Data in to AE	t <sub>s</sub>		50	ns	V <sub>DD</sub> = 10V	
			90	ns	V <sub>DD</sub> = 5V	
Minimum Hold Time Address or data in to address enable	t <sub>h</sub>		50	ns	V <sub>DD</sub> = 10V	
			90	ns	V <sub>DD</sub> = 5V	
Memory reset time	t <sub>MR</sub>		175	ns	V <sub>DD</sub> = 10V, R <sub>L</sub> = 1kΩ	
Memory reset recovery time	T <sub>MRR</sub>		150	ns	V <sub>DD</sub> = 10V } V <sub>DD</sub> = 5V } R <sub>L</sub> = 1kΩ	
			250	ns		

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**DC ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated):  
 Tamb = +25°C, VSS = VEE = 0V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range						
Digital	V <sub>DD</sub> - V <sub>SS</sub>	5	5	13	V	
Analog	V <sub>DD</sub> - V <sub>EE</sub>	5	10	13	V	
Logic level converter	V <sub>SS</sub> - V <sub>EE</sub>	0	5	12	V	
On state resistance	R <sub>ON</sub>		75	108	Ω	V <sub>DD</sub> = 13V } V <sub>DD</sub> = 10V } V <sub>J</sub> = V <sub>L</sub> = 0.6V V <sub>DD</sub> = 5V }
			90		Ω	
			240		Ω	
Difference in On state Resistance between any switches	R <sub>ON</sub>		20		Ω	V <sub>DD</sub> = 13V
			30		Ω	V <sub>DD</sub> = 10V
Off state leakage current (any I <sub>JNE</sub> to any junctor)	I <sub>OFF</sub>		±0.01	±500	nA	V <sub>DD</sub> = 13V, selected crosspoint in Off state
Input logic '0' level	V <sub>IL</sub>		4.5		V	V <sub>DD</sub> = 10V } V <sub>DD</sub> = 5V } V <sub>IS</sub> = V <sub>DD</sub> through 1kΩ
			2.25	1.5	V	
Input logic '1' level	V <sub>IH</sub>		5.5		V	V <sub>DD</sub> = 10V } V <sub>DD</sub> = 5V } V <sub>IS</sub> = V <sub>DD</sub> through 1kΩ
		3.5	2.75		V	
Quiescent device current (per package)	I <sub>Q</sub>		0.1	500	μA	V <sub>DD</sub> = 13V
Maximum current through crosspoint switch	I <sub>MAX</sub>		±8.0		mA	V <sub>DD</sub> = 13V
Switch input capacitance	C <sub>IS</sub>		5		pF	V <sub>DD</sub> = 10V, V <sub>IN</sub> = 0V
Switch output capacitance	C <sub>OS</sub>		20		pF	V <sub>DD</sub> = 10V, V <sub>IN</sub> = 0V
Feedthrough capacitance	C <sub>IOS</sub>		0.2		pF	V <sub>DD</sub> = 10V, V <sub>IN</sub> = 0V
Digital input capacitance	C <sub>IN</sub>		5		pF	V <sub>DD</sub> = 10V, V <sub>IN</sub> = 0V

**NOTES**

1. Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing.
2. V<sub>IS</sub> is the analog switch input voltage, V<sub>IN</sub> is digital input voltage.

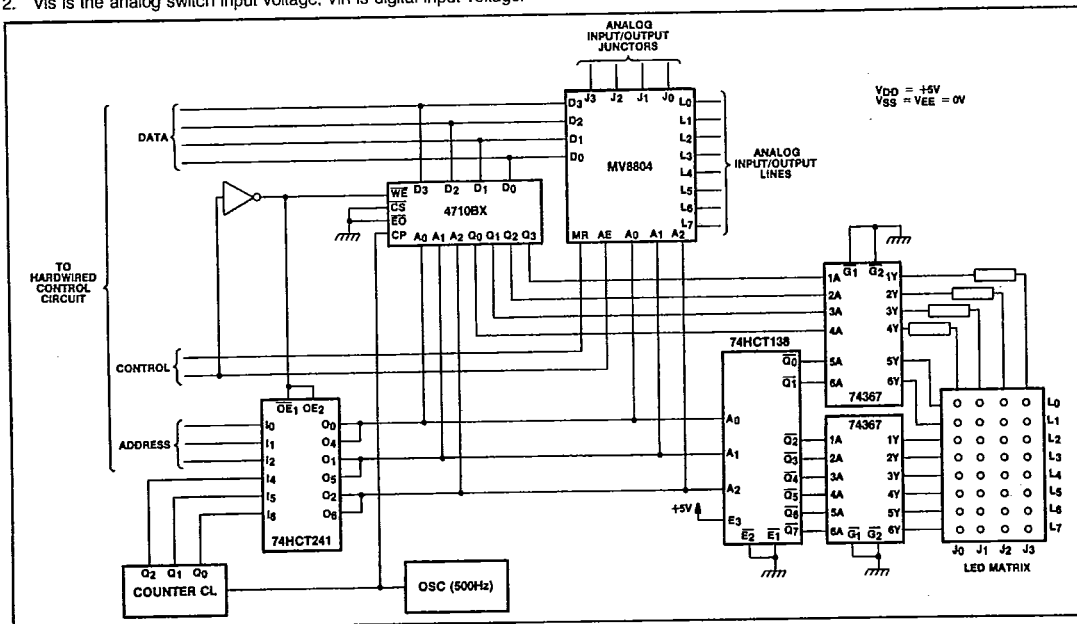


Fig.3 Visual indication of MV8804 control memory status

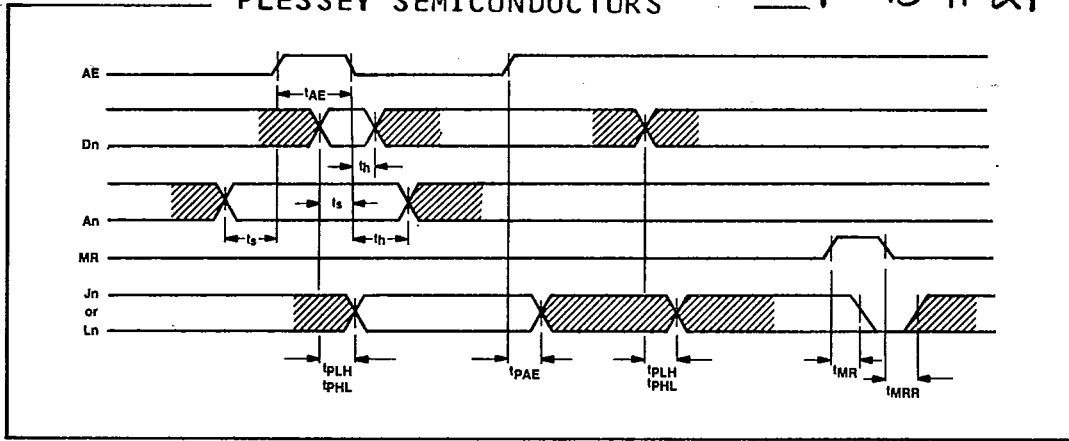


Fig.4 Timing waveforms

**PIN DESCRIPTION**

Pin	Name	Description
1	L <sub>2</sub>	Analog Switch Array Input/Output Line
2	L <sub>1</sub>	Analog Switch Array Input/Output Line
3	L <sub>0</sub>	Analog Switch Array Input/Output Line
4	D <sub>0</sub>	Control Memory Data Line Input
5	J <sub>0</sub>	Analog Switch Array Input/Output Junctor
6	D <sub>1</sub>	Control Memory Data Line Input
7	J <sub>1</sub>	Analog Switch Array Input/Output Junctor
8	D <sub>2</sub>	Control Memory Data Line Input
9	J <sub>2</sub>	Analog Switch Array Input/Output Junctor
10	D <sub>3</sub>	Control Memory Data Line Input
11	J <sub>3</sub>	Analog Switch Input/Output Junctor
12	V <sub>SS</sub>	Negative Digital Power Supply
13	V <sub>EE</sub>	Negative Analog Power Supply
14	A <sub>0</sub>	Control Memory Address Input
15	A <sub>1</sub>	Control Memory Address Input
16	A <sub>2</sub>	Control Memory Address Input
17	AE	Control Memory Address Enable Input (Strobe)
18	MR	Master Reset
19	L <sub>7</sub>	Analog Switch Array Input/Output Line
20	L <sub>6</sub>	Analog Switch Array Input/Output Line
21	L <sub>5</sub>	Analog Switch Array Input/Output Line
22	L <sub>4</sub>	Analog Switch Array Input/Output Line
23	L <sub>3</sub>	Analog Switch Array Input/Output Line
24	V <sub>DD</sub>	Positive Analog/Digital Power Supply

**FUNCTIONAL DESCRIPTION**

The analog switch array is arranged in 8 rows and 4 columns. The row input/outputs are referred to as LINES (L<sub>0</sub>-L<sub>7</sub>) and the column input/outputs as JUNCTORS (J<sub>0</sub>-J<sub>3</sub>). The crosspoint analog switches interconnect the lines and junctors when turned 'ON' and provide a high degree of isolation when turned 'OFF'. Interchannel crosstalk is minimal despite the high density of the analog switch array.

The control memory of the MV8804 can be treated as an 8-word by 4-bit random access memory. The 8 words are selected by the ADDRESS (A<sub>0</sub>-A<sub>2</sub>) inputs through the on-chip address decoder. Data is presented to the memory via the 4 DATA inputs (D<sub>0</sub>-D<sub>3</sub>). This data is asynchronously written into the control memory whenever the ADDRESS ENABLE (AE) input is high. A high level written into a memory cell turns the corresponding crosspoint switch 'ON'

while a low level causes the crosspoint to turn 'OFF'.

Only the crosspoint switches corresponding to the addressed memory word are affected when data is written into the memory. The remaining switches retain their previous states. By establishing appropriate patterns in the control memory, any combination of lines and junctors may be interconnected. A high level on the MASTER RESET (MR) input returns all memory locations to a low level and turns all crosspoint switches 'OFF', effectively isolating the lines from the junctors. The digital logic level converters allow the digital input levels to differ from limits of the analog levels switched through the array. For example, with V<sub>DD</sub> = 5V, V<sub>SS</sub> = 0V and V<sub>EE</sub> = -6V, the control inputs can be driven by a 5V system while the analog voltages through the crosspoint switches can swing from +5V to -6V.

LOGIC TRUTH TABLE

PLESSEY SEMICONDUCTORS

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Master Reset	Address enable	Address			Addressed line	Input data to control memory				Junctors connected to addressed line			
		A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	J <sub>3</sub>	J <sub>2</sub>	J <sub>1</sub>	J <sub>0</sub>
H	X	X	X	X	All	X	X	X	X	All switches 'Off'			
L	L	X	X	X	None	X	X	X	X	No change of state			
L	H	L	L	L	L0	L	L	L	L	•	•	•	•
L	H	L	L	L	L0	L	L	L	H	•	•	+	•
L	H	L	L	L	L0	L	L	H	L	•	•	+	•
L	H	L	L	L	L0	L	L	H	H	•	•	+	•
L	H	L	L	L	L0	L	H	L	L	•	+	•	•
L	H	L	L	L	L0	L	H	H	L	•	+	+	•
L	H	L	L	L	L0	L	H	H	H	•	+	+	•
L	H	L	L	L	L0	H	L	L	L	+	•	•	•
L	H	L	L	L	L0	H	L	L	H	+	•	•	•
L	H	L	L	L	L0	H	L	H	L	+	•	+	•
L	H	L	L	L	L0	H	L	H	H	+	•	+	•
L	H	L	L	L	L0	H	H	L	L	+	+	•	•
L	H	L	L	L	L0	H	H	H	L	+	+	+	•
L	H	L	L	L	L0	H	H	H	H	+	+	+	•
L	H	L	L	L	L0	H	H	H	H	+	+	+	+
L	H	L	L	H	L1	Each addressed line may have 16 different combinations of junctors connected to it by inputing data to the control memory as shown for L0.							
L	H	L	H	L	L2								
L	H	L	H	H	L3								
L	H	H	L	L	L4								
L	H	H	L	H	L5								
L	H	H	H	L	L6								
L	H	H	H	H	L7								

NOTES

- L = Low Logic Level
- H = High Logic Level
- X = Don't Care Condition
- + = Indicates Connection Between Junctor and Addressed Line
- = Indicates No Connection Between Junctor and Addressed Line

8 x 8 ANALOG/DIGITAL SWITCH

Two MV8804s configured as shown in Fig.7, implement an 8 x 8 analog/digital switch. The switch capacity can be expanded to an M x N array of inputs/outputs. Expansion in the N dimension is as shown and connecting the lines (L0-L7) from the MV8804s in common.

Expansion in the N dimension is accomplished by replicating the circuit shown and connecting the MV8804 junctors (J0-J3) in common. The address and data control inputs of the MV8804s can be connected in common for any size and switch provided that the address enable (AE) inputs are driven individually, for example by a 74HCT515 programmable AND gate.

A particular signal path is connected by setting up the appropriate signals or the address and data lines and taking the corresponding address enable input high. The master reset (MR), when taken high, disconnects all signal paths.

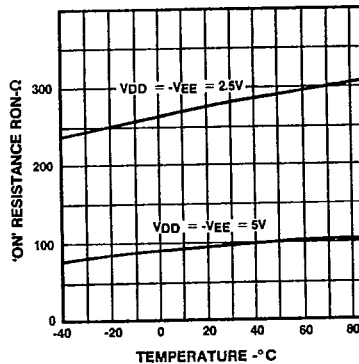


Fig.5 ON resistance vs temperature (input signal voltage = supply voltage/2)

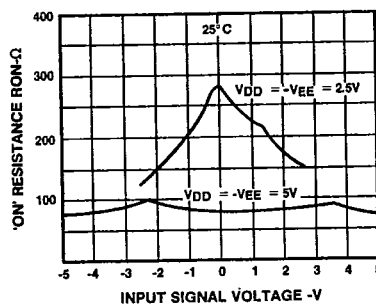


Fig.6 ON resistance vs input signal voltage

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PLESSEY SEMICONDUCTORS

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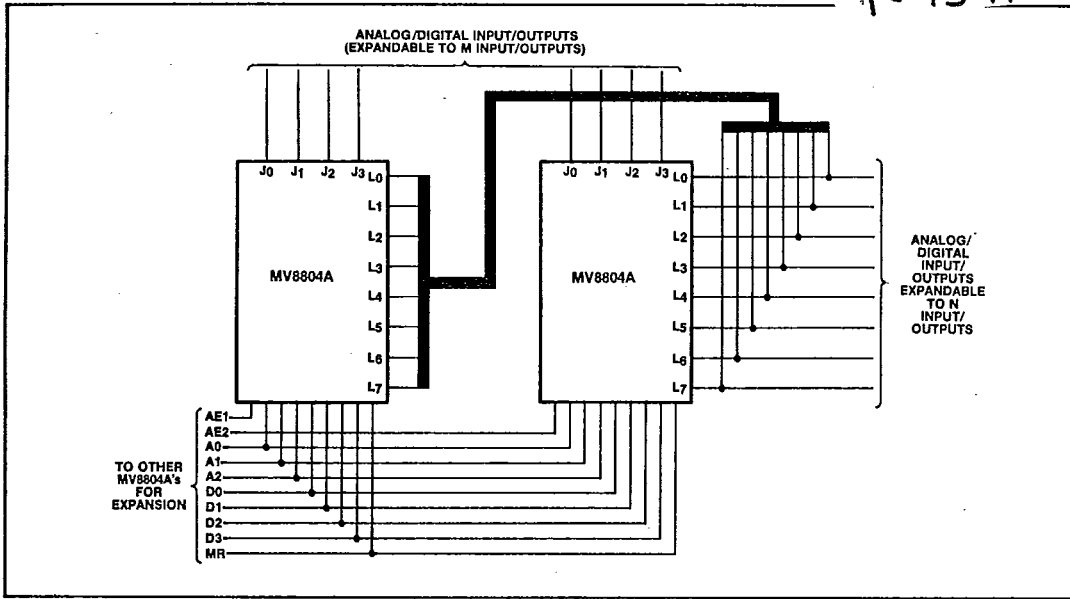


Fig.7 Expanding MV8804s