



**V53C104B**  
**HIGH PERFORMANCE, LOW POWER**  
**256K X 4 BIT FAST PAGE MODE**  
**CMOS DYNAMIC RAM**

**PRELIMINARY**

| <b>HIGH PERFORMANCE V53C104B</b>               | <b>60/60L</b> | <b>70/70L</b> | <b>80/80L</b> |
|------------------------------------------------|---------------|---------------|---------------|
| Max. RAS Access Time, ( $t_{RAC}$ )            | 60 ns         | 70 ns         | 80 ns         |
| Max. Column Address Access Time, ( $t_{CAA}$ ) | 30 ns         | 35 ns         | 40 ns         |
| Min. Fast Page Mode Cycle Time, ( $t_{PC}$ )   | 40 ns         | 45 ns         | 50 ns         |
| Min. Read/Write Cycle Time, ( $t_{RC}$ )       | 120 ns        | 130 ns        | 150 ns        |

| <b>LOW POWER V53C104BL</b>               | <b>60L</b>  | <b>70L</b>  | <b>80L</b>  |
|------------------------------------------|-------------|-------------|-------------|
| Max. CMOS Standby Current, ( $I_{DD6}$ ) | 200 $\mu$ A | 200 $\mu$ A | 200 $\mu$ A |

### Features

- 256K x 4 Organization
- RAS access time: 60,70,80 ns
- Low power dissipation for V53C104B-80
  - Operating Current – 70 mA max.
  - TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C104B – 1.0 mA max.
  - V53C104BL – 0.2 mA max.
- Read-Modify-Write, RAS-Only Refresh, CAS-Before-RAS Refresh capability.
- Common I/O capability
- Refresh Interval
  - V53C104B – 512 cycles/8ms
  - V53C104BL – 512 cycles/64ms
- On-chip substrate bias generator
- Fast Page Mode for a sustained data rate greater than 25 MHz
- Standard packages are 20 pin Plastic DIP and 26/20 pin SOJ
- Low Battery Back-up Current
  - V53C104BL – 300  $\mu$ A max.
  - 200  $\mu$ A max. available on request

### Description

The Vitelic V53C104B is a high speed 262,144 x 4 bit CMOS dynamic random access memory. Fabricated with Vitelic's VICMOS IV technology, the V53C104B offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C104BL).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x4) bits within a row with cycle times as short as 40 ns. Because of static circuitry, the  $\overline{CAS}$  clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C104B ideally suited for graphics, digital signal processing and high performance computing systems.

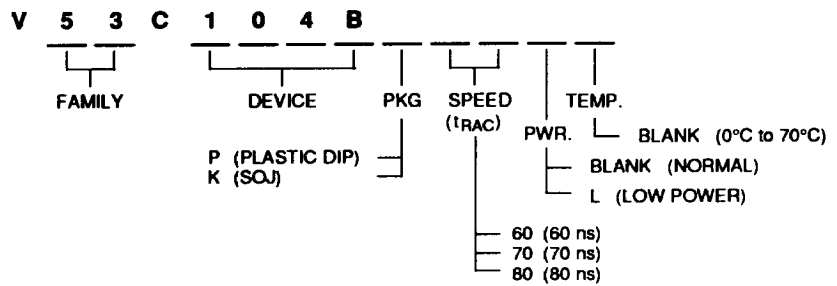
The V53C104BL offers a maximum data retention power of 1.65 mW when operating in CMOS standby mode and performing CAS-before-RAS refresh cycles.

### Device Usage Chart

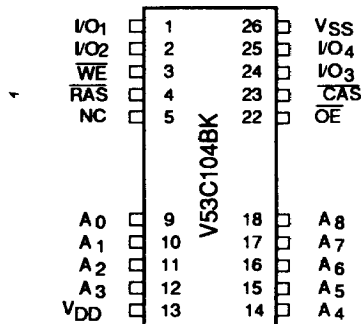
| Operating Temperature Range | Package Outline |   | Access Time (ns) |    |    | Power |      | Temperature Mark |
|-----------------------------|-----------------|---|------------------|----|----|-------|------|------------------|
|                             | P               | K | 60               | 70 | 80 | Low   | Std. |                  |
| 0°C to 70 °C                | •               | • | •                | •  | •  | •     | •    | Blank            |

V53C104B Rev. 01 September 1991

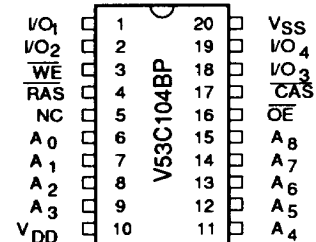
| Description | Pkg. | Pin Count |
|-------------|------|-----------|
| Plastic DIP | P    | 20        |
| SOJ         | K    | 26/20     |



**26/20 Lead SOJ Package  
PIN CONFIGURATION  
Top View**



**20 Lead Plastic DIP  
PIN CONFIGURATION  
Top View**



**Pin Names**

|                                    |                       |
|------------------------------------|-----------------------|
| A <sub>0</sub> –A <sub>8</sub>     | Address Inputs        |
| RAS                                | Row Address Strobe    |
| CAS                                | Column Address Strobe |
| WE                                 | Write Enable          |
| OE                                 | Output Enable         |
| I/O <sub>1</sub> –I/O <sub>4</sub> | Data Input, Output    |
| V <sub>DD</sub>                    | +5V Supply            |
| V <sub>SS</sub>                    | 0V Supply             |
| NC                                 | No Connect            |

**Absolute Maximum Ratings\***

**Ambient Temperature**

Under Bias .....–10°C to +80°C

Storage Temperature (plastic) ....–55°C to +125°C

Voltage Relative to V<sub>SS</sub> .....–1.0 V to +7.0 V

Voltage on V<sub>DD</sub> relative to V<sub>SS</sub> .....–1.0 V to +7.0 V

Data Output Current .....50 mA

Power Dissipation .....1.0 W

\*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

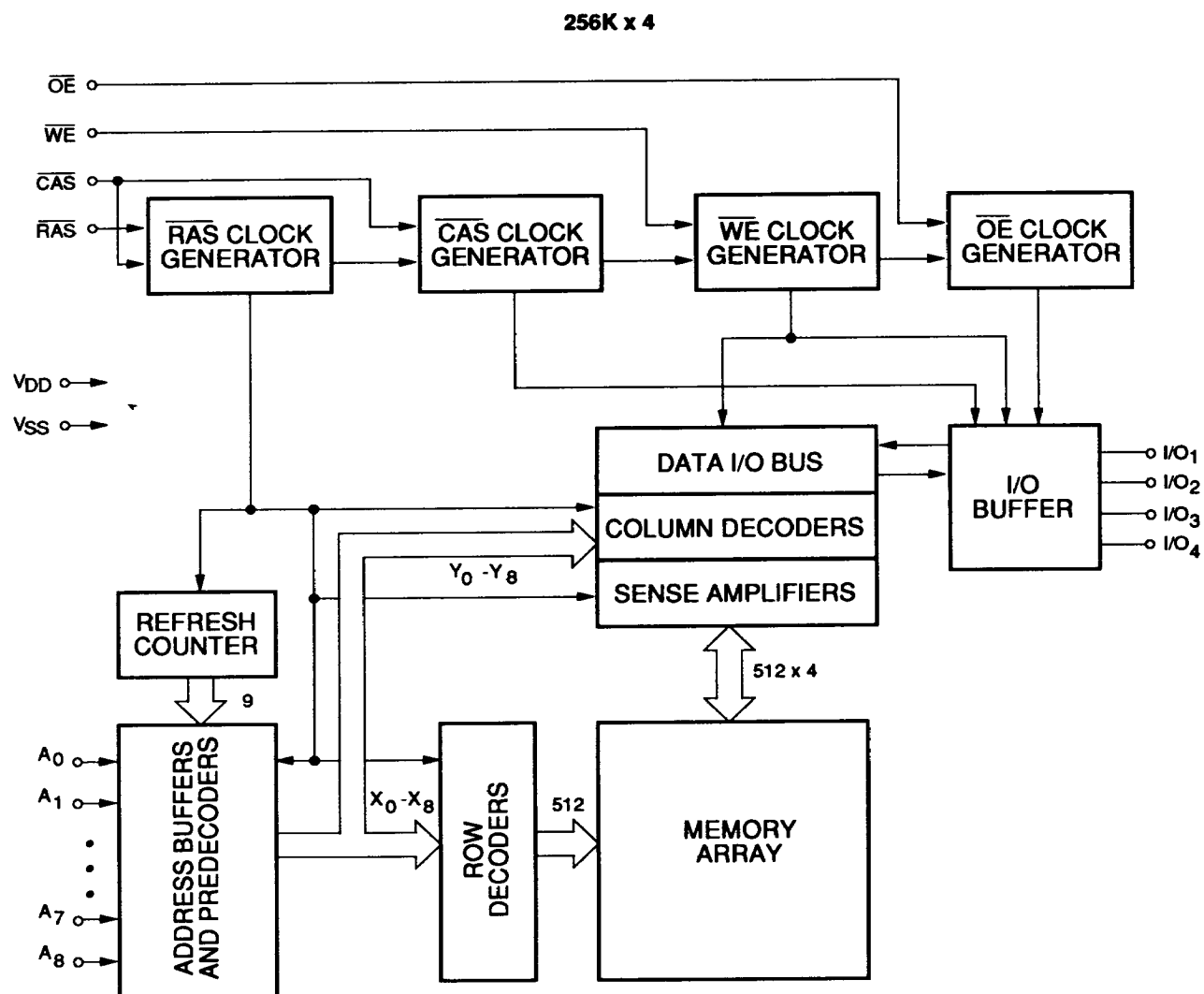
**Capacitance\***

T<sub>A</sub> = 25°C, V<sub>DD</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V

| Symbol           | Parameter         | Typ. | Max. | Unit |
|------------------|-------------------|------|------|------|
| C <sub>IN1</sub> | Address Input     | —    | 6    | pF   |
| C <sub>IN2</sub> | RAS, CAS, WE, OE  | —    | 7    | pF   |
| C <sub>OUT</sub> | Data Input/Output | —    | 7    | pF   |

\* Note: Capacitance is sampled and not 100% tested

### Block Diagram



**DC and Operating Characteristics (1-2)**
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ , unless otherwise specified.

| Symbol      | Parameter                                                     | Access Time | V53C104 |            | V53C104L |            | Unit          | Test Conditions                                                                                     | Notes |
|-------------|---------------------------------------------------------------|-------------|---------|------------|----------|------------|---------------|-----------------------------------------------------------------------------------------------------|-------|
|             |                                                               |             | Min.    | Max.       | Min.     | Max.       |               |                                                                                                     |       |
| $I_{LI}$    | Input Leakage Current<br>(any input pin)                      |             | -10     | 10         | -10      | 10         | $\mu\text{A}$ | $V_{SS} \leq V_{IN} \leq V_{DD}$                                                                    |       |
| $I_{LO}$    | Output Leakage Current<br>(for High-Z State)                  |             | -10     | 10         | -10      | 10         | $\mu\text{A}$ | $V_{SS} \leq V_{OUT} \leq V_{DD}$<br>RAS, CAS at $V_{IH}$                                           |       |
| $I_{DD1}$   | $V_{DD}$ Supply Current,<br>Operating                         | 60          |         | 90         |          | 90         | mA            | $t_{RC} = t_{RC}(\text{min.})$                                                                      | 1, 2  |
|             |                                                               | 70          |         | 80         |          | 80         |               |                                                                                                     |       |
|             |                                                               | 80          |         | 70         |          | 70         |               |                                                                                                     |       |
| $I_{DD2}$   | $V_{DD}$ Supply Current,<br>TTL Standby                       |             |         | 2.0        |          | 2.0        | mA            | RAS, CAS at $V_{IH}$<br>other inputs $\geq V_{SS}$                                                  |       |
| $I_{DD3}$   | $V_{DD}$ Supply Current,<br>RAS-Only Refresh                  | 60          |         | 90         |          | 90         | mA            | $t_{RC} = t_{RC}(\text{min.})$                                                                      | 2     |
|             |                                                               | 70          |         | 80         |          | 80         |               |                                                                                                     |       |
|             |                                                               | 80          |         | 70         |          | 70         |               |                                                                                                     |       |
| $I_{DD4}$   | $V_{DD}$ Supply Current,<br>Fast Page Mode<br>Operation       | 60          |         | 80         |          | 80         | mA            | Minimum Cycle                                                                                       | 1, 2  |
|             |                                                               | 70          |         | 70         |          | 70         |               |                                                                                                     |       |
|             |                                                               | 80          |         | 60         |          | 60         |               |                                                                                                     |       |
| $I_{DD5}$   | Standby, Output Enabled                                       |             |         | 3.0        |          | 2.0        | mA            | RAS= $V_{IH}$ , CAS= $V_{IL}$<br>other inputs $\geq V_{SS}$                                         | 1     |
| $I_{DD6}$   | $V_{DD}$ Supply Current<br>CMOS Standby                       |             |         | 1.0        |          | 0.2        | mA            | RAS $\geq V_{DD} - 0.2\text{ V}$ ,<br>CAS $\geq V_{DD} - 0.2\text{ V}$<br>other input $\geq V_{SS}$ |       |
| $I_{DD7}^*$ | Battery Back-up<br>Data Retention Current<br>(V53C104BL only) |             |         | N.A.       |          | 0.3*       | mA            | CAS-Before-RAS<br>Refresh Cycle<br>$t_{RC} = 125\text{ }\mu\text{s}$<br>CMOS Clock Levels           | 1, 18 |
| $V_{IL}$    | Input Low Voltage                                             |             | -1.0    | 0.8        | -1.0     | 0.8        | V             |                                                                                                     | 3     |
| $V_{IH}$    | Input High Voltage                                            |             | 2.4     | $V_{DD}+1$ | 2.4      | $V_{DD}+1$ | V             |                                                                                                     | 3     |
| $V_{OL}$    | Output Low Voltage                                            |             |         | 0.4        |          | 0.4        | V             | $I_{OL} = 4.2\text{ mA}$                                                                            |       |
| $V_{OH}$    | Output High Voltage                                           |             | 2.4     |            | 2.4      |            |               | $I_{OH} = -5\text{ mA}$                                                                             |       |

\* $I_{DD7} = 0.2\text{ mA}$  max. available on request.

**AC Characteristics**
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$  unless otherwise noted

AC Test conditions, input pulse levels 0 to 3V

| #  | JEDEC Symbol    | Symbol       | Parameter                                                | 60/L |      | 70/L |      | 80/L |      | Unit | Notes   |
|----|-----------------|--------------|----------------------------------------------------------|------|------|------|------|------|------|------|---------|
|    |                 |              |                                                          | Min. | Max. | Min. | Max. | Min. | Max. |      |         |
| 1  | $t_{RL1RH1}$    | $t_{RAS}$    | $\overline{RAS}$ Pulse Width                             | 60   | 75K  | 70   | 75K  | 80   | 75K  | ns   |         |
| 2  | $t_{RL2RL2}$    | $t_{RC}$     | Read or Write Cycle Time                                 | 120  |      | 130  |      | 150  |      | ns   |         |
| 3  | $t_{RH2RL2}$    | $t_{RP}$     | $\overline{RAS}$ Precharge Time                          | 50   |      | 50   |      | 60   |      | ns   |         |
| 4  | $t_{RL1CH1}$    | $t_{CSH}$    | $\overline{CAS}$ Hold Time                               | 60   |      | 70   |      | 80   |      | ns   |         |
| 5  | $t_{CL1CH1}$    | $t_{CAS}$    | $\overline{CAS}$ Pulse Width                             | 15   |      | 20   |      | 20   |      | ns   |         |
| 6  | $t_{RL1CL1}$    | $t_{RCD}$    | $\overline{RAS}$ to $\overline{CAS}$ Delay               | 20   | 45   | 20   | 50   | 20   | 60   | ns   | 4       |
| 7  | $t_{WH2CL2}$    | $t_{RCS}$    | Read Command Setup Time                                  | 0    |      | 0    |      | 0    |      | ns   |         |
| 8  | $t_{AVRL2}$     | $t_{ASR}$    | Row Address Setup Time                                   | 0    |      | 0    |      | 0    |      | ns   |         |
| 9  | $t_{RL1AX}$     | $t_{RAH}$    | Row Address Hold Time                                    | 10   |      | 10   |      | 10   |      | ns   |         |
| 10 | $t_{AVCL2}$     | $t_{ASC}$    | Column Address Setup Time                                | 0    |      | 0    |      | 0    |      | ns   |         |
| 11 | $t_{CL1AX}$     | $t_{CAH}$    | Column Address Hold Time                                 | 15   |      | 15   |      | 15   |      | ns   |         |
| 12 | $t_{CL1RH1(R)}$ | $t_{RSH(R)}$ | $\overline{RAS}$ Hold Time (Read Cycle)                  | 15   |      | 20   |      | 20   |      | ns   |         |
| 13 | $t_{CH2RL2}$    | $t_{CRP}$    | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time      | 5    |      | 5    |      | 5    |      | ns   |         |
| 14 | $t_{CH2WX}$     | $t_{RCH}$    | Read Command Hold Time Referenced to $\overline{CAS}$    | 0    |      | 0    |      | 0    |      | ns   | 5       |
| 15 | $t_{RH2WX}$     | $t_{RRH}$    | Read Command Hold Time Referenced to $\overline{RAS}$    | 0    |      | 0    |      | 0    |      | ns   | 5       |
| 16 | $t_{OEL1RH2}$   | $t_{ROH}$    | $\overline{RAS}$ Hold Time Referenced to $\overline{OE}$ | 10   |      | 10   |      | 10   |      | ns   |         |
| 17 | $t_{GL1QV}$     | $t_{OAC}$    | Access Time from $\overline{OE}$                         |      | 15   |      | 20   |      | 20   | ns   |         |
| 18 | $t_{CL1QV}$     | $t_{CAC}$    | Access Time from $\overline{CAS}$                        |      | 15   |      | 20   |      | 20   | ns   | 6,7     |
| 19 | $t_{RL1QV}$     | $t_{RAC}$    | Access Time from $\overline{RAS}$                        |      | 60   |      | 70   |      | 80   | ns   | 6,8,9   |
| 20 | $t_{AVQV}$      | $t_{CAA}$    | Access Time from Column Address                          |      | 30   |      | 35   |      | 40   | ns   | 6,7, 10 |

**AC Characteristics (Cont'd.)**

| #  | JEDEC Symbol      | Symbol       | Parameter                                                     | 60/L |      | 70/L |      | 80/L |      | Unit | Notes |
|----|-------------------|--------------|---------------------------------------------------------------|------|------|------|------|------|------|------|-------|
|    |                   |              |                                                               | Min. | Max. | Min. | Max. | Min. | Max. |      |       |
| 21 | $t_{CL1QX}$       | $t_{LZ}$     | $\overline{OE}$ or $\overline{CAS}$ to Low-Z Output           | 0    |      | 0    |      | 0    |      | ns   | 16    |
| 22 | $t_{CH2QZ}$       | $t_{HZ}$     | $\overline{OE}$ or $\overline{CAS}$ to High-Z Output          | 0    | 20   | 0    | 20   | 0    | 20   | ns   | 16    |
| 23 | $t_{RL1AX}$       | $t_{AR}$     | Column Address Hold Time from $\overline{RAS}$                | 50   |      | 55   |      | 60   |      | ns   |       |
| 24 | $t_{RL1AV}$       | $t_{RAD}$    | $\overline{RAS}$ to Column Address Delay Time                 | 15   | 30   | 15   | 35   | 15   | 40   | ns   | 11    |
| 25 | $t_{CL1RH1(W)}$   | $t_{RSH(W)}$ | $\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle | 15   |      | 20   |      | 20   |      | ns   |       |
| 26 | $t_{WL1CH1}$      | $t_{CWL}$    | Write Command to $\overline{CAS}$ Lead Time                   | 15   |      | 20   |      | 20   |      | ns   |       |
| 27 | $t_{WL1GL2}$      | $t_{WCS}$    | Write Command Setup Time                                      | 0    |      | 0    |      | 0    |      | ns   | 12,13 |
| 28 | $t_{CL1WH1}$      | $t_{WCH}$    | Write Command Hold Time                                       | 10   |      | 15   |      | 15   |      | ns   |       |
| 29 | $t_{WL1WH1}$      | $t_{WP}$     | Write Pulse Width                                             | 10   |      | 15   |      | 15   |      | ns   |       |
| 30 | $t_{RL1WH1}$      | $t_{WCR}$    | Write Command Hold Time from $\overline{RAS}$                 | 50   |      | 55   |      | 60   |      | ns   |       |
| 31 | $t_{WL1RH1}$      | $t_{RWL}$    | Write Command to $\overline{RAS}$ Lead Time                   | 15   |      | 20   |      | 20   |      | ns   |       |
| 32 | $t_{DVWL2}$       | $t_{DS}$     | Data in Setup Time                                            | 0    |      | 0    |      | 0    |      | ns   | 14    |
| 33 | $t_{WL1DX}$       | $t_{DH}$     | Data in Hold Time                                             | 15   |      | 15   |      | 15   |      | ns   | 14    |
| 34 | $t_{WL1GL2}$      | $t_{WOH}$    | Write to $\overline{OE}$ Hold Time                            | 15   |      | 20   |      | 20   |      | ns   | 14    |
| 35 | $t_{GH2DX}$       | $t_{OED}$    | $\overline{OE}$ to Data Delay Time                            | 15   |      | 20   |      | 20   |      | ns   | 14    |
| 36 | $t_{RL2RL2(RMW)}$ | $t_{RWC}$    | Read-Modify-Write Cycle Time                                  | 170  |      | 185  |      | 205  |      | ns   |       |
| 37 | $t_{RL1RH1(RMW)}$ | $t_{RRW}$    | Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width          | 105  |      | 125  |      | 135  |      | ns   |       |
| 38 | $t_{CL1WL2}$      | $t_{CWD}$    | $\overline{CAS}$ to $\overline{WE}$ Delay                     | 40   |      | 50   |      | 50   |      | ns   | 12    |

**AC Characteristics (Cont'd.)**

| #  | JEDEC Symbol          | Symbol    | Parameter                                                                         | 60/L |      | 70/L |      | 80/L |      | Unit | Notes |
|----|-----------------------|-----------|-----------------------------------------------------------------------------------|------|------|------|------|------|------|------|-------|
|    |                       |           |                                                                                   | Min. | Max. | Min. | Max. | Min. | Max. |      |       |
| 39 | $t_{RL1WL2}$          | $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle              | 85   |      | 100  |      | 110  |      | ns   | 12    |
| 40 | $t_{CL1CH1}$          | $t_{CRW}$ | $\overline{CAS}$ Pulse Width (RMW)                                                | 65   |      | 75   |      | 75   |      | ns   |       |
| 41 | $t_{AVWL2}$           | $t_{AWD}$ | Col. Address to $\overline{WE}$ Delay                                             | 60   |      | 65   |      | 70   |      | ns   | 12    |
| 42 | $t_{CL2CL2}$          | $t_{PC}$  | Fast Page Mode Read or Write Cycle Time                                           | 40   |      | 45   |      | 50   |      | ns   |       |
| 43 | $t_{CH2CL2}$          | $t_{CP}$  | $\overline{CAS}$ Precharge Time                                                   | 10   |      | 10   |      | 10   |      | ns   |       |
| 44 | $t_{AVRH1}$           | $t_{CAR}$ | Column Address to $\overline{RAS}$ Setup Time                                     | 30   |      | 35   |      | 45   |      | ns   |       |
| 45 | $t_{CH2OV}$           | $t_{CAP}$ | Access Time from Column Precharge                                                 |      | 35   |      | 40   |      | 45   | ns   | 7     |
| 46 | $t_{RL1DX}$           | $t_{DHR}$ | Data in Hold Time Referenced to $\overline{RAS}$                                  | 50   |      | 55   |      | 60   |      | ns   |       |
| 47 | $t_{CL1RL2}$          | $t_{CSR}$ | $\overline{CAS}$ Setup Time<br>$\overline{CAS}$ -before- $\overline{RAS}$ Refresh | 10   |      | 10   |      | 10   |      | ns   |       |
| 48 | $t_{RH2CL2}$          | $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time                               | 10   |      | 10   |      | 10   |      | ns   |       |
| 49 | $t_{RL1CH1}$          | $t_{CHR}$ | $\overline{CAS}$ Hold Time<br>$\overline{CAS}$ -before- $\overline{RAS}$ Refresh  | 30   |      | 30   |      | 30   |      | ns   |       |
| 50 | $t_{CL2CL2}$<br>(RMW) | $t_{PCM}$ | Fast Page Mode Read-Modify-Write Cycle Time                                       | 85   |      | 95   |      | 100  |      | ns   |       |
|    | $t_T$                 | $t_T$     | Transition Time (Rise and Fall)                                                   | 3    | 50   | 3    | 50   | 3    | 50   | ns   | 15    |
|    |                       | $t_{REF}$ | Refresh Interval (512 Cycles)                                                     |      | 8    |      | 8    |      | 8    | ms   | 17    |
|    |                       | $t_{REF}$ | Refresh Interval<br>V53C104BL Only<br>(512 Refresh cycles, $t_{RC}=125\mu s$ )    |      | 64   |      | 64   |      | 64   | ms   | 17,18 |

1.  $I_{DD}$  is dependent on output loading when the device output is selected. Specified  $I_{DD}$  (max.) is measured with the output open.
2.  $I_{DD}$  is dependent upon the number of address transitions. Specified  $I_{DD}$  (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified  $V_{IL}$  (min.) is steady state operating. During transitions,  $V_{IL}$  (min.) may undershoot to  $-1.0$  V for a period not to exceed 20 ns. All AC parameters are measured with  $V_{IL}$  (min.)  $\geq V_{SS}$  and  $V_{IH}$  (max.)  $\leq V_{DD}$ .
4.  $t_{RCD}$  (max.) is specified for reference only. Operation within  $t_{RCD}$  (max.) limits insures that  $t_{RAC}$  (max.) and  $t_{CAA}$  (max.) can be met. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max.), the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
5. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of  $t_{CAA}$ ,  $t_{CAC}$  and  $t_{CAP}$ .
8. Assumes that  $t_{RAD} \leq t_{RAD}$  (max.). If  $t_{RAD}$  is greater than  $t_{RAD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RAD}$  exceeds  $t_{RAD}$  (max.).
9. Assumes that  $t_{RCD} \leq t_{RCD}$  (max.). If  $t_{RCD}$  is greater than  $t_{RCD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds  $t_{RCD}$  (max.).
10. Assumes that  $t_{RAD} \geq t_{RAD}$  (max.).
11. Operation within the  $t_{RAD}$  (max.) limit ensures that  $t_{RAC}$  (max.) can be met.  $t_{RAD}$  (max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max.) limit, the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
12.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are not restrictive operating parameters.
13.  $t_{WCS}$  (min.) must be satisfied in an Early Write Cycle.
14.  $t_{DS}$  and  $t_{DH}$  are referenced to the latter occurrence of  $\overline{CAS}$  or  $\overline{WE}$ .
15.  $t_T$  is measured between  $V_{IH}$  (min.) and  $V_{IL}$  (max.). AC-measurements assume  $t_T = 5$  ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200  $\mu$ s pause and 8  $\overline{RAS}$ -containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycles.

$$t_{RC} = 125 \mu s (125 \mu s \times 512 = 64 \text{ ms})$$

$$t_{RAS} = t_{RAS} \text{ (min) to } 1 \mu s$$

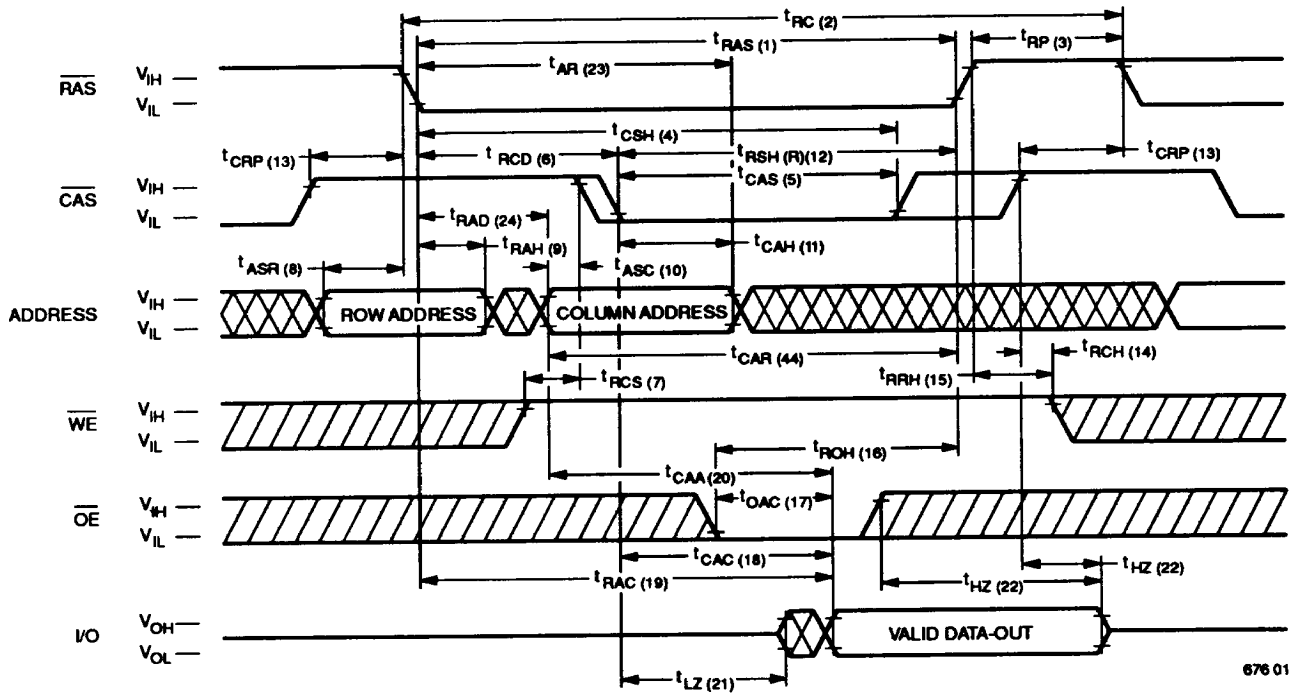
$$\text{Input voltages : } \overline{RAS} \text{ and } \overline{CAS} \quad V_{IH} > V_{DD} - 0.2 \text{ V}$$

$$V_{IL} < 0.2 \text{ V}$$

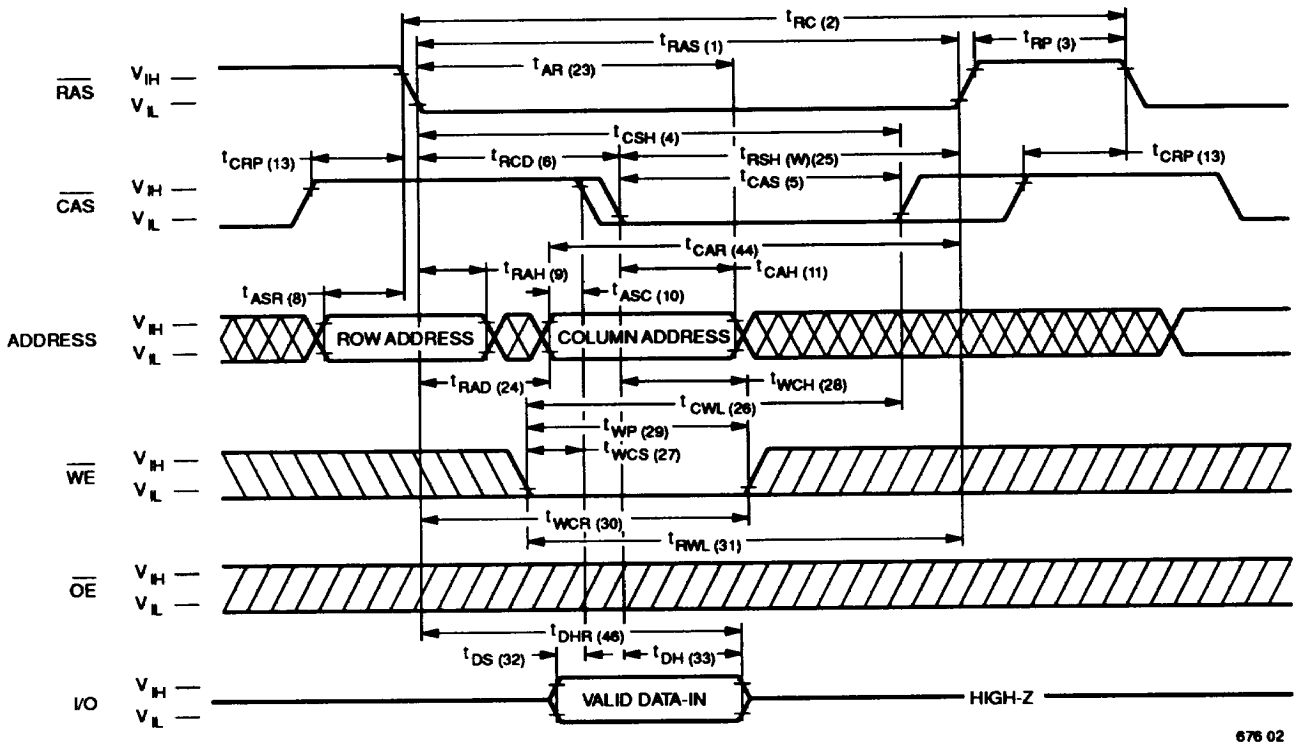
$$\overline{WE} \text{ and } \overline{OE} \quad V_{IH} > V_{DD} - 0.2 \text{ V}$$

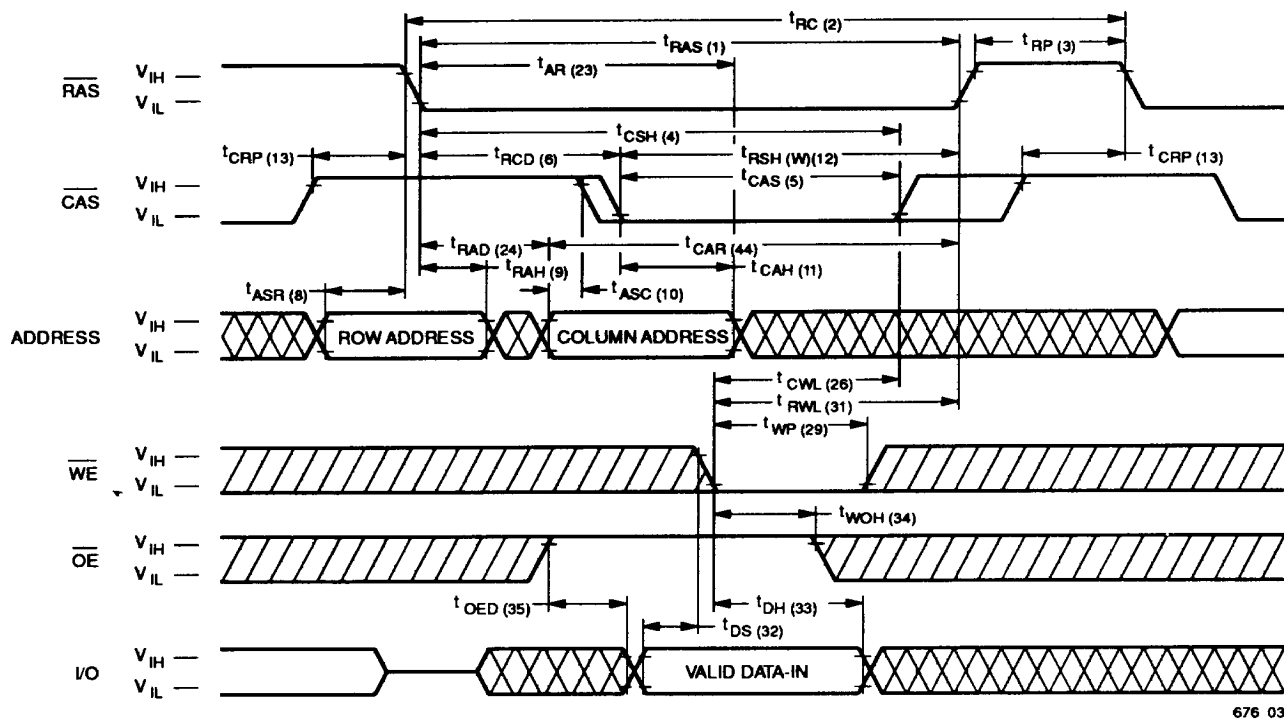
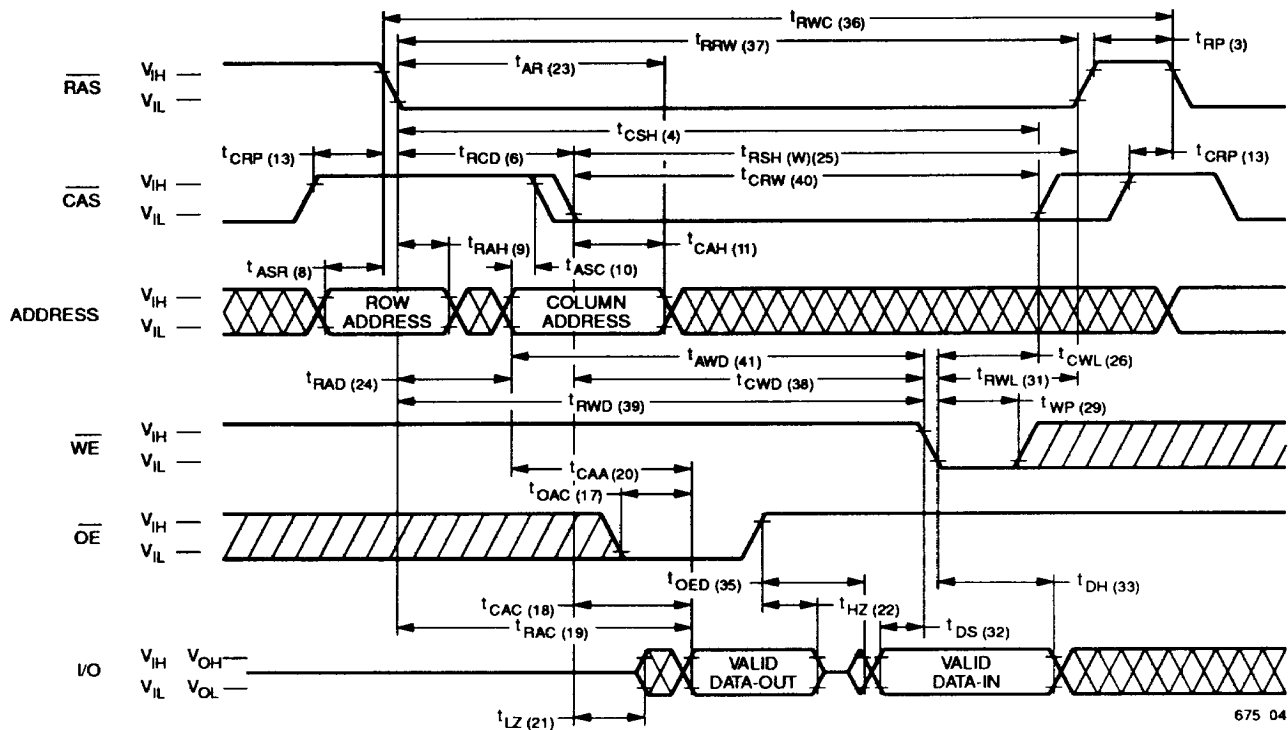
$$\text{All other inputs at stable } V_{IH} \text{ or } V_{IL}$$

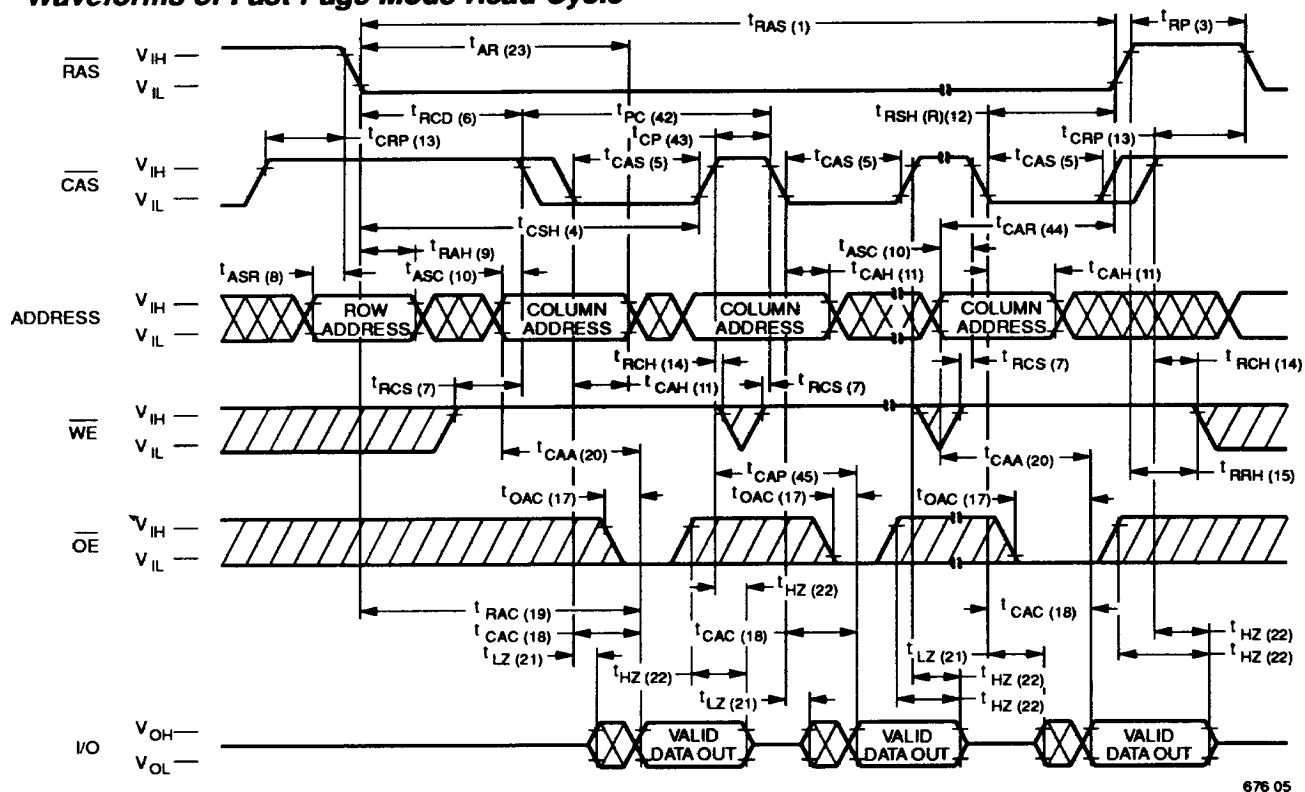
### Waveforms of Read Cycle



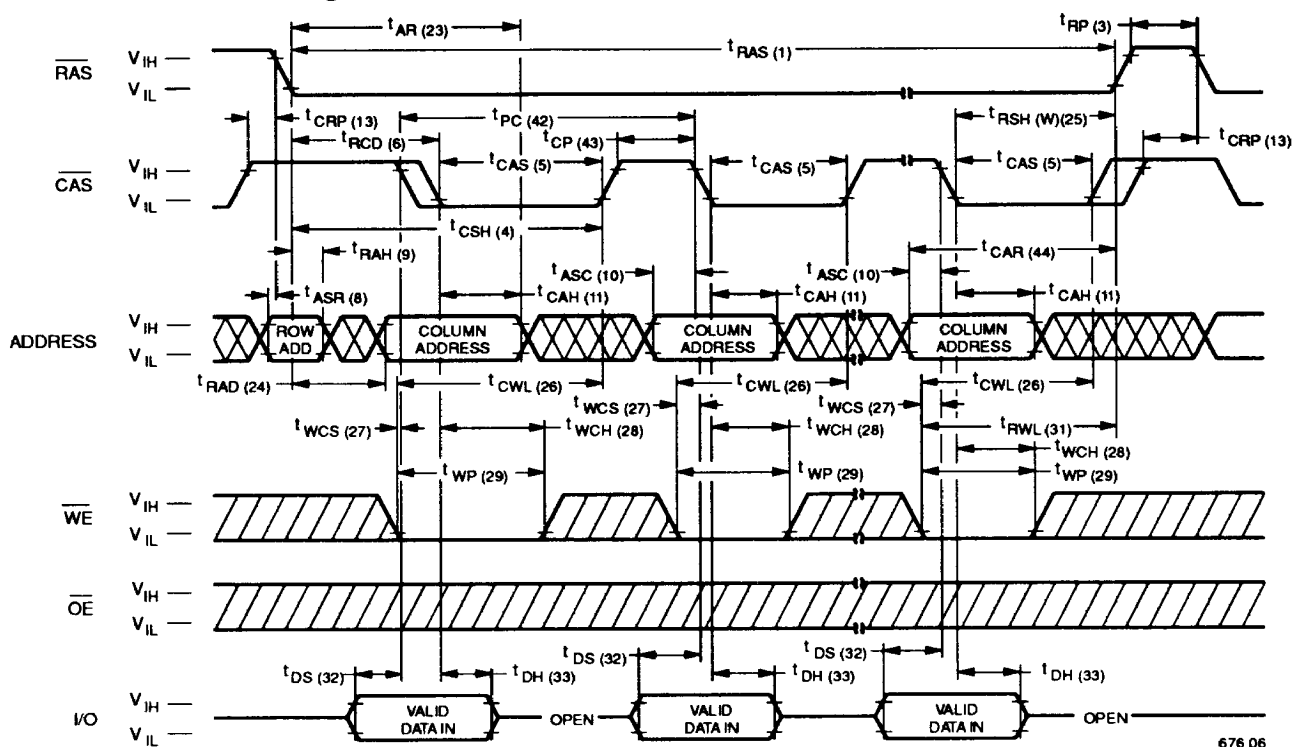
### Waveforms of Early Write Cycle



**Waveforms of  $\overline{\text{OE}}$ -Controlled Write Cycle**

**Waveforms of Read-Modify-Write Cycle**


**Waveforms of Fast Page Mode Read Cycle**


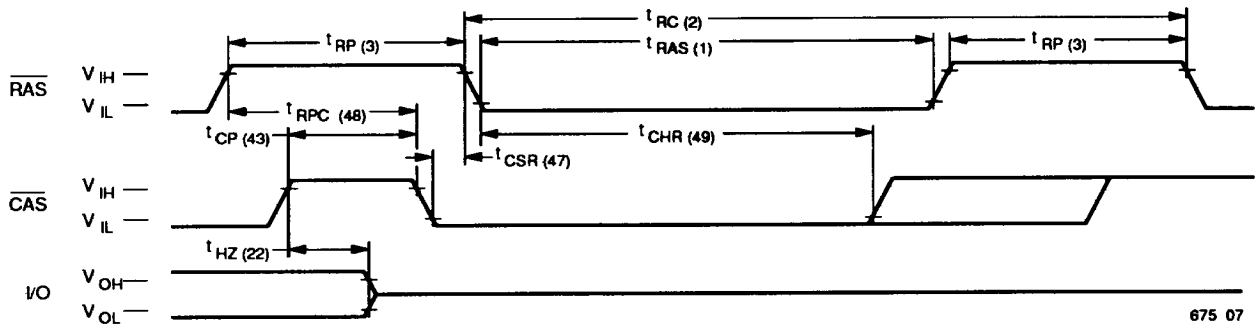
676 05

**Waveforms of Fast Page Mode Write Cycle**


676 06

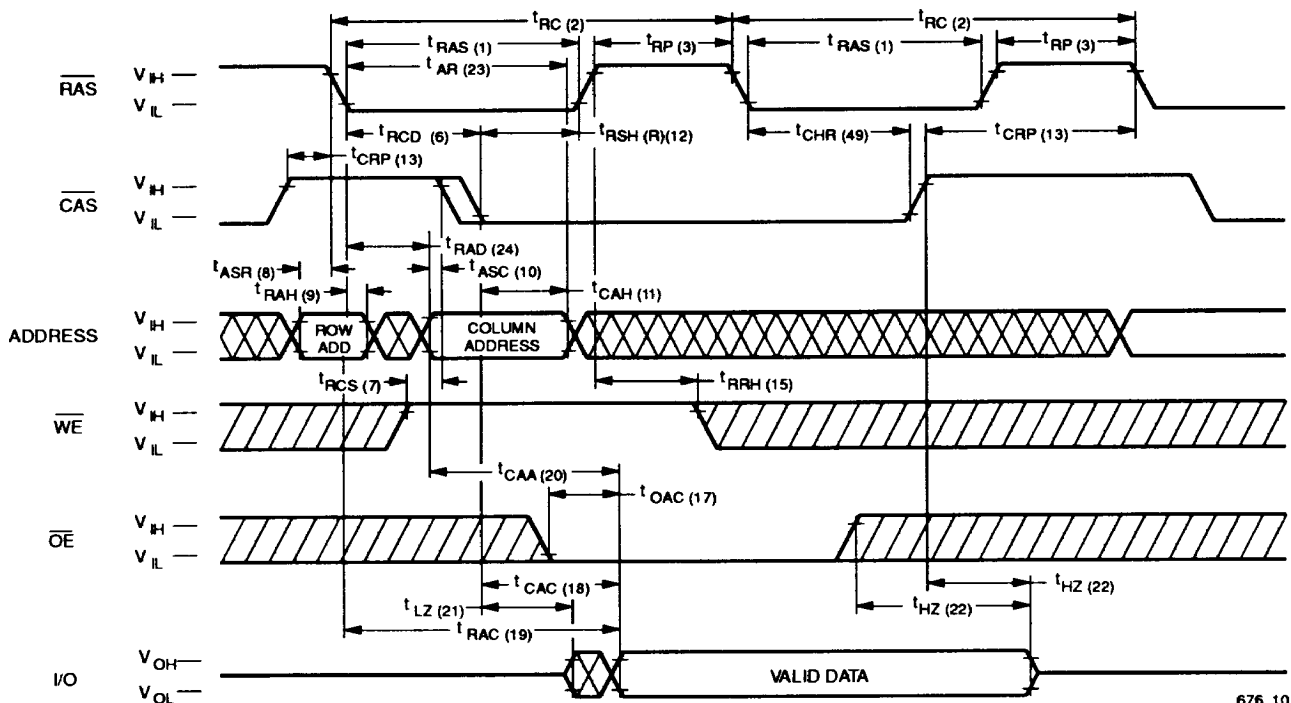
[illegible]

NOTE:  $\overline{WE}, \overline{OE}$  = Don't care

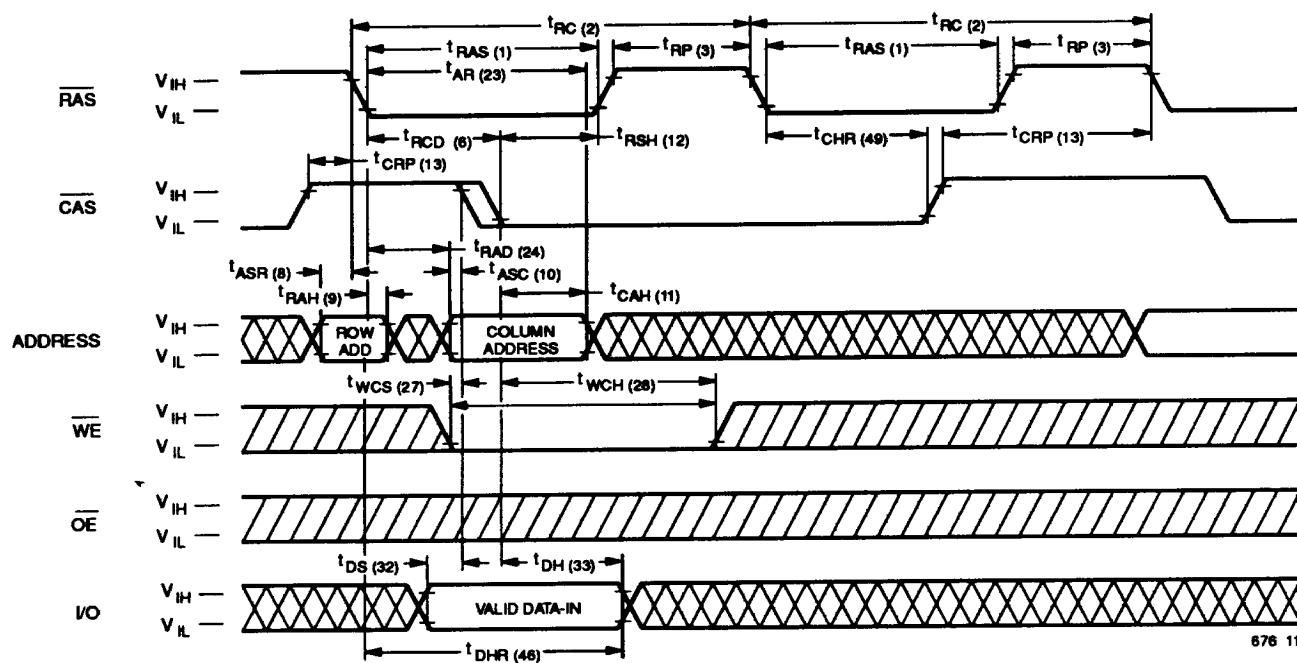
**Waveforms of CAS-before-RAS Refresh Cycle**


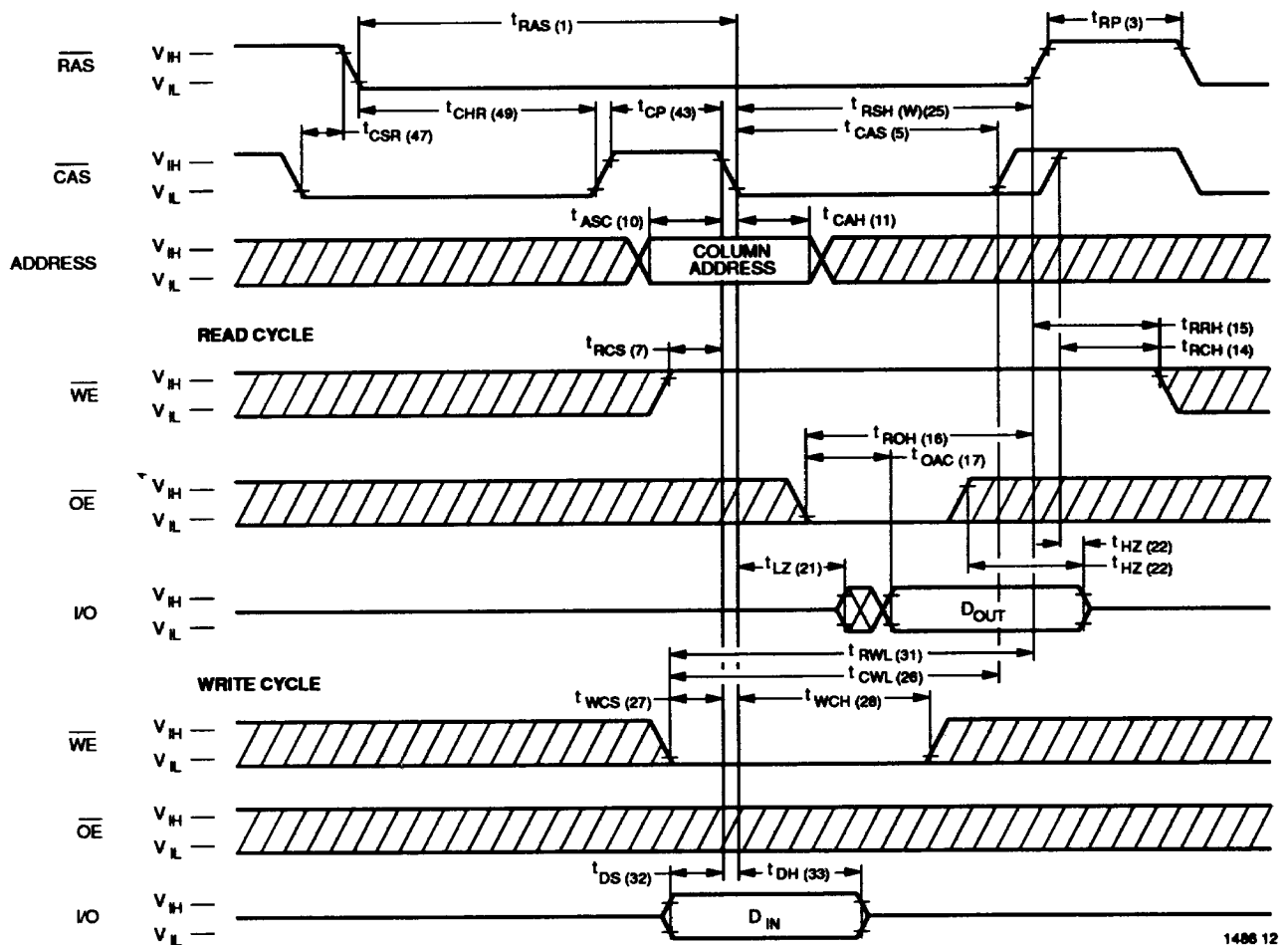
675 07

NOTE:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $A_0-A_7$  = Don't care

**Waveforms of Hidden Refresh Cycle (Read)**


676 10

**Waveforms of Hidden Refresh Cycle (Write)**


**Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Counter Test Cycle**


1486 12

## Functional Description

The V53C104B is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C104B reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ( $\overline{\text{RAS}}$ ). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ( $\overline{\text{CAS}}$ ). Because access time is primarily dependent on a valid column address rather than the precise time that the  $\overline{\text{CAS}}$  edge occurs, the delay time from  $\overline{\text{RAS}}$  to  $\overline{\text{CAS}}$  has little effect on the access time.

## Memory Cycle

A memory cycle is initiated by bringing  $\overline{\text{RAS}}$  low. Any memory cycle, once initiated, must not be ended or aborted before the minimum  $t_{\text{RAS}}$  time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time  $t_{\text{RP}}/t_{\text{CP}}$  has elapsed.

## Read Cycle

A Read cycle is performed by holding the Write Enable ( $\overline{\text{WE}}$ ) signal High during a  $\overline{\text{RAS}}/\overline{\text{CAS}}$  operation. The column address must be held for a minimum specified by  $t_{\text{AR}}$ . Data Out becomes valid only when  $t_{\text{OAC}}$ ,  $t_{\text{RAC}}$ ,  $t_{\text{CAA}}$  and  $t_{\text{CAC}}$  are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by  $t_{\text{CAA}}$  when  $t_{\text{RAC}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{OAC}}$  are all satisfied.

## Write Cycle

A Write Cycle is performed by taking  $\overline{\text{WE}}$  and  $\overline{\text{CAS}}$  low during a  $\overline{\text{RAS}}$  operation. The column address is latched by  $\overline{\text{CAS}}$ . The Write Cycle can be  $\overline{\text{WE}}$  controlled or  $\overline{\text{CAS}}$  controlled depending on whether  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$  falls later. Consequently, the input data must be valid at or before the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. In the  $\overline{\text{CAS}}$ -controlled Write Cycle, when the leading edge of  $\overline{\text{WE}}$  occurs prior to the  $\overline{\text{CAS}}$  low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function.

Ending the Write with  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  will maintain the output in the High-Z state.

In the  $\overline{\text{WE}}$  controlled Write Cycle,  $\overline{\text{OE}}$  must be in the high state and  $t_{\text{OED}}$  must be satisfied.

## Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses ( $A_0$  through  $A_9$ ) with  $\overline{\text{RAS}}$  at least once every 8 ms. Any Read, Write, Read-Modify-Write or  $\overline{\text{RAS}}$ -only cycle refreshes the addressed row.
2. Using a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Cycle. If  $\overline{\text{CAS}}$  makes a transition from low to high to low after the previous cycle and before  $\overline{\text{RAS}}$  falls,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is activated. The V53C104B uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  counter test mode is provided to ensure reliable operation of the internal refresh counter.

## Data Retention Mode

The V53C104B offers a CMOS standby mode that is entered by causing the  $\overline{\text{RAS}}$  clock to swing between a valid  $V_{\text{L}}$  and an "extra high"  $V_{\text{IH}}$  within 0.2 V of  $V_{\text{DD}}$ . While the  $\overline{\text{RAS}}$  clock is at the "extra high" level, the V53C104B power consumption is reduced to the low  $I_{\text{DD6}}$  level. Overall  $I_{\text{DD}}$  consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{\text{RC}}) \times (I_{\text{DD1}}) + (t_{\text{RX}} - t_{\text{RC}}) \times (I_{\text{DD6}})}{t_{\text{RX}}}$$

Where:  $t_{\text{RC}}$  = Refresh Cycle Time  
 $t_{\text{RX}}$  = Refresh Interval / 512

### Fast Page Mode Operation

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining  $\overline{\text{RAS}}$  low while performing successive  $\overline{\text{CAS}}$  cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while  $\overline{\text{CAS}}$  is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of  $\overline{\text{CAS}}$ , eliminating  $t_{\text{ASC}}$  and  $t_{\text{T}}$  from the critical timing path.  $\overline{\text{CAS}}$  latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is  $t_{\text{CAA}}$  or  $t_{\text{CAP}}$  controlled. If the column address is valid prior to the rising edge of  $\overline{\text{CAS}}$ , the access time is referenced to the  $\overline{\text{CAS}}$  rising edge and is specified by  $t_{\text{CAP}}$ . If the column address is valid after the rising  $\overline{\text{CAS}}$  edge, access is timed from the occurrence of a valid address and is specified by  $t_{\text{CAA}}$ . In both cases, the falling edge of  $\overline{\text{CAS}}$  latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 25 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{\text{RC}} + 511 \times t_{\text{PC}}}$$

### Data Output Operation

The V53C104B Input/Output is controlled by  $\overline{\text{OE}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{RAS}}$ . A  $\overline{\text{RAS}}$  low transition enables the transfer of data to and from the selected row address in the Memory Array. A  $\overline{\text{RAS}}$  high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a  $\overline{\text{RAS}}$  low transition, a  $\overline{\text{CAS}}$  low transition or  $\overline{\text{CAS}}$  low level enables the internal I/O path. A  $\overline{\text{CAS}}$  high transition or a  $\overline{\text{CAS}}$  high level disables the I/O path and the output driver if it is enabled. A  $\overline{\text{CAS}}$  low transition while  $\overline{\text{RAS}}$  is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding

$\overline{\text{OE}}$  high. The  $\overline{\text{OE}}$  signal has no effect on any data stored in the output latches. A  $\overline{\text{WE}}$  low level can also disable the output drivers when  $\overline{\text{CAS}}$  is low. During a Write cycle, if  $\overline{\text{WE}}$  goes low at a time in relationship to  $\overline{\text{CAS}}$  that would normally cause the outputs to be active, it is necessary to use  $\overline{\text{OE}}$  to disable the output drivers prior to the  $\overline{\text{WE}}$  low transition to allow Data In Setup Time ( $t_{\text{DS}}$ ) to be satisfied.

### Power-On

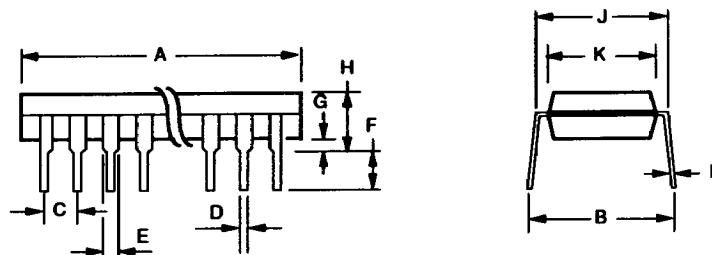
After application of the  $V_{\text{DD}}$  supply, an initial pause of 200  $\mu\text{s}$  is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the  $V_{\text{DD}}$  current requirement of the V53C104B is dependent on the input levels of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . If  $\overline{\text{RAS}}$  is low during Power-On, the device will go into an active cycle and  $I_{\text{DD}}$  will exhibit current transients. It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with  $V_{\text{DD}}$  or be held at a valid  $V_{\text{IH}}$  during Power-On to avoid current surges.

**Table 1. Vitellic V53C104B Data Output Operation for Various Cycle Types**

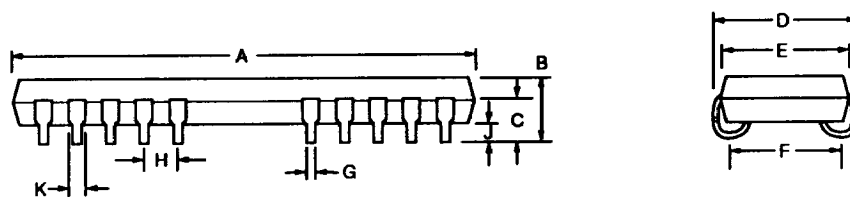
| Cycle Type                                                             | I/O State                                                                       |
|------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| Read Cycles                                                            | Data from Addressed Memory Cell                                                 |
| $\overline{\text{CAS}}$ -Controlled Write Cycle (Early Write)          | High-Z                                                                          |
| $\overline{\text{WE}}$ -Controlled Write Cycle (Late Write)            | $\overline{\text{OE}}$ Controlled. High<br>$\overline{\text{OE}}$ = High-Z I/Os |
| Read-Modify-Write Cycles                                               | Data from Addressed Memory Cell                                                 |
| Fast Page Mode Read                                                    | Data from Addressed Memory Cell                                                 |
| Fast Page Mode Write Cycle (Early Write)                               | High-Z                                                                          |
| Fast Page Mode Read-Modify-Write Cycle                                 | Data from Addressed Memory Cell                                                 |
| $\overline{\text{RAS}}$ -only Refresh                                  | High-Z                                                                          |
| $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle | Data remains as in previous cycle                                               |
| $\overline{\text{CAS}}$ -only Cycles                                   | High-Z                                                                          |

### Package Outlines



### 20-pin 300 mil Plastic DIP

| Dimension | Inches      | Millimeters |
|-----------|-------------|-------------|
| A         | 0.980 Max.  | 24.892 Max. |
| B         | 0.320/0.370 | 8.128/9.398 |
| C         | .100 Typ.   | 2.54 Typ.   |
| D         | 0.018/0.024 | 0.457/0.610 |
| E         | 0.048/0.054 | 1.219/1.372 |
| F         | 0.110/0.140 | 2.794/3.556 |
| G         | 0.005/0.050 | 0.127/1.270 |
| H         | .180 Max.   | 4.572 Max.  |
| J         | 0.300/0.330 | 7.62/8.382  |
| K         | 0.280/0.300 | 7.112/7.620 |
| L         | 0.008/0.013 | 0.20/0.33   |

**26/20-pin SOJ**

| Dimension | Inches      | Millimeters   |
|-----------|-------------|---------------|
| A         | 0.672/0.684 | 17.069/17.374 |
| B         | 0.125/0.135 | 3.175/3.429   |
| C         | 0.082/0.093 | 2.083/2.362   |
| D         | 0.332/0.342 | 8.433/8.687   |
| E         | 0.296/0.304 | 7.518/7.722   |
| F         | 0.255/0.275 | 6.477/6.985   |
| G         | 0.018 Typ.  | 0.457 Typ.    |
| H         | 0.05 Typ.   | 1.270 Typ.    |
| J         | 0.026 Min.  | 0.660 Min.    |
| K         | 0.028 Typ.  | 0.711 Typ.    |

**VITELIC****WORLDWIDE VITELIC OFFICES****V53C104B****U.S.A.**

VITELIC SEMICONDUCTOR  
3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0185

**TAIWAN**

VITELIC CORP.  
133, MINSHENG E. RD.,  
SECTION III, 7B  
TAIPEI, TAIWAN, R.O.C.  
PHONE: 011-886-2-718-1369  
FAX: 011-886-2-718-1362

VITELIC TAIWAN CORP.  
1 R&D ROAD I  
SCIENCE BASED IND. PARK  
HSIN CHU, TAIWAN, R.O.C.  
PHONE: 011-886-35-770055  
FAX: 011-886-35-776520

**JAPAN**

VITELIC JAPAN CORP.  
NIHON SEIMEI KAWASAKI  
BLDG., 8TH FL.  
1-1 MINAMI-CHO KAWASAKI-KU  
KAWASAKI-SHI KANAGAWA 210  
JAPAN  
PHONE: 011-04-4-246-3021  
FAX: 011-04-4-246-3029

**HONG KONG**

VITELIC (HONG KONG) LIMITED  
19 DAI FU STREET  
TAIPO INDUSTRIAL ESTATE  
TAIPO, NT, HONG KONG  
PHONE: 011-852-665-4883  
FAX: 011-852-664-7535

**KOREA**

VITELIC CORP.  
RM. 309, BEUK-EUN BLDG.  
1339-1 SEOCHO-DONG,  
SEOCHO-KU  
SEOUL, KOREA  
PHONE: 011-82-2-553-3385  
FAX: 011-82-2-553-3675

**VITELIC U.S. SALES OFFICES****NORTHWESTERN**

VITELIC SEMICONDUCTOR  
3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0185

**SOUTHWESTERN**

VITELIC SEMICONDUCTOR  
SUITE 200  
5150 E. PACIFIC COAST HWY.  
LONG BEACH, CA 90804  
PHONE: 213-498-3314  
FAX: 213-597-2174

**EASTERN/MIDWESTERN**

VITELIC SEMICONDUCTOR  
SUITE 203  
619 SEVERN AVENUE  
ANNAPOLIS, MD 21403  
PHONE: 301-267-9616  
FAX: 301-267-7411  
or: 301-268-9081

VICMOS is a trademark of VITELIC  
© Copyright 1991, Vitelic Corporation

9/91  
Printed in U.S.A.

The information in this document is subject to change without notice.

VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of VITELIC.

VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.

**VITELIC**

3910 N. First Street, San Jose, CA 95134-1501 Ph: (408) 433-6000 Fax: (408) 433-0952 Tlx: 371-9461

20

032161 ✓